A Wide-Range Highly Power Efficient RF-to-DC Rectifier for RF Energy Harvesting Systems

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***Abstract*—In this paper, a wide input range, 4-stage threshold voltage compensated RF-DC power converter is introduced. A novel threshold voltage compensation scheme is proposed that can be applied to a rectifier chain with a relatively low number of stages. This proposed structure is shown to provide a high power conversion efficiency (PCE) over a wide input power range that increases the coverage area of wireless powering. Designed and simulated in IBM 130-nm CMOS technology, the proposed 915-MHz rectifier exhibits a PCE of above 20% over the 20-dB input power range while driving a 1-MΩ load resistor. For the same load, utilizing a minimal number of compensated rectifier stages, the proposed circuit exhibits a record maximum PCE of 52% at -10 dBm for single-ended Dickson-based CMOS rectifiers. The proposed circuit demonstrates a -22.3 dBm sensitivity for 1 V output across a 1-MΩ resistive load.**

***Keywords*—RF energy harvesting, Rectifier, Power conversion efficiency.**

I. INTRODUCTION

Progress of energy harvesting systems has opened a new era of charging a battery remotely or powering a batteryless system without costly wiring and bulk head connections. A radio frequency (RF) energy harvester produces a DC supply source by scavenging the electromagnetic energy transmitted by a dedicated transmitting antenna. The received RF signal is rectified and provides a promising solution for powering up a variety of low-power wireless portable electronic devices. The amount of harvested energy depends on the strength of received RF signals determined by the distance from the transmitter and the power conversion efficiency (PCE) of the RF energy harvesters. To increase the range of the operation and the range of wireless powering, it is imperative to enhance the PCE of RF rectifiers for the widest possible input power range especially at low input power levels.

CMOS rectifiers in most cases are based on the Dickson's charge pump, which relies on the use of cascaded diode connected transistors as rectifying devices [1]. The performance parameters of Dickson's topology such as PCE are substantially affected by the threshold voltage of the diode-connected transistors. Several works have been reported on the compensation of threshold voltages of the rectifying devices [2]-[8]. Work in [2] utilizes an internal V_{TH} cancellation circuit. In this method, a capacitor holds the threshold voltage of a diode connected transistor and applies this stored threshold voltage at the gate-source of the MOS transistors for compensation. This technique uses large resistance values for decreasing the leakage current that leads to large silicon area for multi-stage implementations. Large resistors in [2], apart from the occupation of large silicon area, suffers from substantial parasitic capacitance to the substrate that leads to high leakage currents and hence reduced output power and PCE. A self-compensation technique based on the Dickson's topology is introduced in [3]. In this work, later stages are providing the compensating voltage for former stages. In this work to be able to connect the bulk of NMOS transistors to their sources, triple well NMOS transistors are used. To eliminate the need for triple-well NMOS transistors and to be able to compensate all stages, authors in [4] used PMOS transistors as rectifying device for all stages except for first few stages. Gate of PMOS transistors is connected to former stages for compensation and gate of first few NMOS transistors are connected to their following stages. A minimal additional circuitry is used in [5] to adaptively decrease the reverse leakage current during the reverse-biased region. In [3]-[5], a large number of stages are needed to generate the appropriate compensation voltage for each individual transistor from the later or former stages. The RF-DC power converters constructed of a large number of stages inherently have lower PCE. Because the PCE of cascaded stages is equal to the product of all PCEs of each individual stages. Therefore even if the threshold voltage compensation techniques are effective in increasing the overall PCE of multistage rectifier it will increase a significantly degraded PCE resulted from cascading a large number of stages. Only a narrow high PCE range can be achieved in [3]-[5] as appropriate compensation voltages from the later or former stages for each transistor can be created for limited input power range. Wide input range, differential drive rectifiers are introduced in [6]-[8]. The differential circuit requires a balun or differential antenna and triple-well NMOS transistors.

In this paper, we propose an area efficient, wide input range, 4-stage, single ended, threshold voltage compensated RF-DC power converter. In this design, the drain voltage of each transistor is connected to a voltage divider to provide the appropriate compensation voltage for each gate. As the proposed threshold voltage compensation can be applied to rectifiers with relatively low number of stages and provide the appropriate compensation voltage for each gate for the wide

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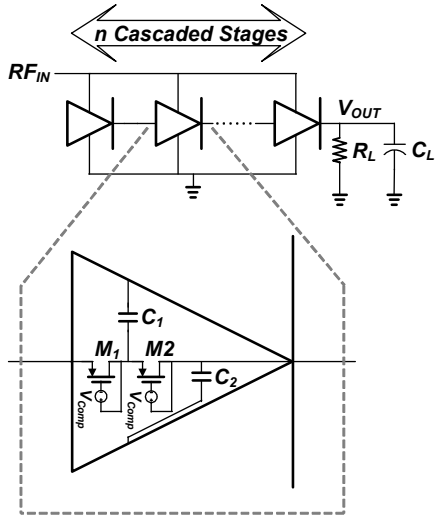
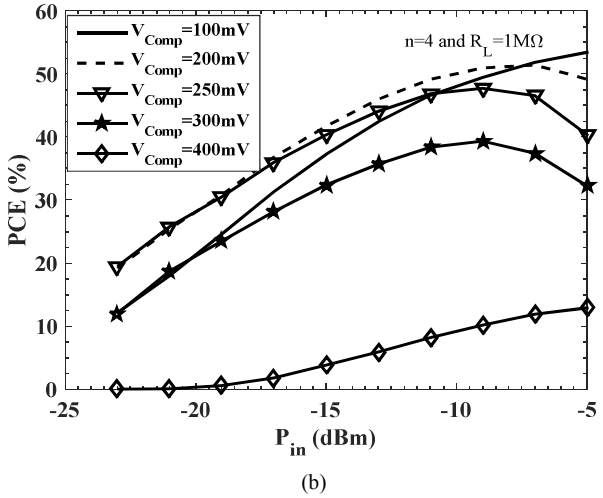
input power range, this design can provide higher PCE and output power for the wider input power range in comparison to previously reported structures. The RF-DC power converter presented in this paper is designed and simulated in a standard 130-nm CMOS technology.

II. Operating Principle of the Proposed Rectifier

In this work we first explore what would be an optimum compensation level to produce the highest possible PCE over the largest input power range. For this propose, an ideal compensation voltage source is applied between the gate and drain of the transistors of the main rectifier chain of a 4-stage Dickson based rectifier as shown in Fig 1 (a). The simulation results as shown in Fig 1 (b), indicate that an optimum compensation voltage for a 4-stage RF-DC converter is around $\frac{V_{TH}}{2}$ (200 mV for a CMOS process with V_{TH} of 424 mV) over the input power range of -23 to -5 dBm.



(a)



(b)

Fig. 1. (a)Simulated circuit for finding the optimum compensation voltage. (b) RF rectifier's power conversion efficiency as a function of input power for different compensation voltages.

The proposed RF-DC converter structure that produces the desired compensation voltage is shown in Fig. 2. In this design, minimal number of rectifier stages are used. To reduce ON resistance, the source-gate voltage of each PMOS transistor in the rectification chain is increased by connecting the gate voltage of each transistor to a voltage lower than its drain voltage. A lower voltage for each gate in the main rectification chain is locally created by a voltage divider at the drain of each transistor which aims to turn the drain voltage into smaller portions. In Fig. 2, transistors M_1 to M_8 and coupling capacitors C_1 to C_7 are constructing the main rectification chain. For eliminating the need for triple-well NMOS transistors, PMOS transistors are chosen as the rectifying devices in all stages except for the first transistor in the first stage. Transistors $MA_{0\text{-}7}$, $MB_{0\text{-}11}$, $MC_{0\text{-}11}$, $MD_{0\text{-}14}$, and $ME_{0\text{-}14}$ are the voltage dividers providing the compensation voltage for the gates of $M_{1\text{-}6}$ from the drain voltages of $M_{2\text{-}6}$. The source-drain voltage drop of MA_0, MB_0, MC_0 and ME_0 for the wide range of input powers is about half of the threshold voltage creating the good compensation voltage for the gates of $M_{2\text{-}6}$. For the gates of M_2, M_4, and M_6 that their drain voltage is DC (not connected to RF_{IN}), the compensated voltage is simply provided by connecting them to drains of MA_0, MC_0, and ME_0 respectively. $CB_{1\text{-}4}$ connected to gates/drains of MA_0, MA_7, MC_0 and ME_0 suppresses the high-frequency noise at the gates of M_1, M_2, M_4 and M_6 respectively. For providing the compensation voltage for the gates of M_3 and M_5 that their drain voltage is AC (connected to RF_{IN} via the decoupling capacitors), the DC level of the drain voltages of M_3 and M_5 is shifted to lower voltages without attenuation of their AC component by passively delivering the AC component to the DC-shifted drains of MB_0 and MD_0 through the small DC block capacitors of CD_1 and CD_2 respectively. In this design, the first transistor of the main rectification chain is an NMOS. For the compensation of this transistor, its gate is connected to a higher voltage with respect to its drain (GND). The compensation voltage for this transistor is provided through connecting the gate of this NMOS to the last transistor (MA_0) of the voltage divider connected to its adjacent PMOS transistor (M_2). The last stage of this designed rectifier (transistors M_7 and M_8) is left uncompensated to decrease the leakage.

As the voltage dividers connected to the drain of PMOS transistors in the main rectification chain are working in the subthreshold region, the compensation voltage created by this scheme can be calculated by writing the transistor's current in the subthreshold region as:

$$I_{Leakage} \approx 2n\mu C_{ox}\frac{W}{L}\left(\frac{kT}{q}\right)^2 \exp\left(\frac{|V_{GS}| - V_{TH}}{\frac{nkT}{q}}\right), \qquad (1)$$

where $I_{Leakage}$ is the current flowing through the each voltage divider chain, n is the subthreshold slope factor, μ is the effective mobility, k is the Boltzmann constant and $|V_{GS}|$ is the generated compensation voltage for each PMOS transistor in the main rectification chain. To enhance the performance of the rectifier, the leakage current flowing through the voltage dividers should

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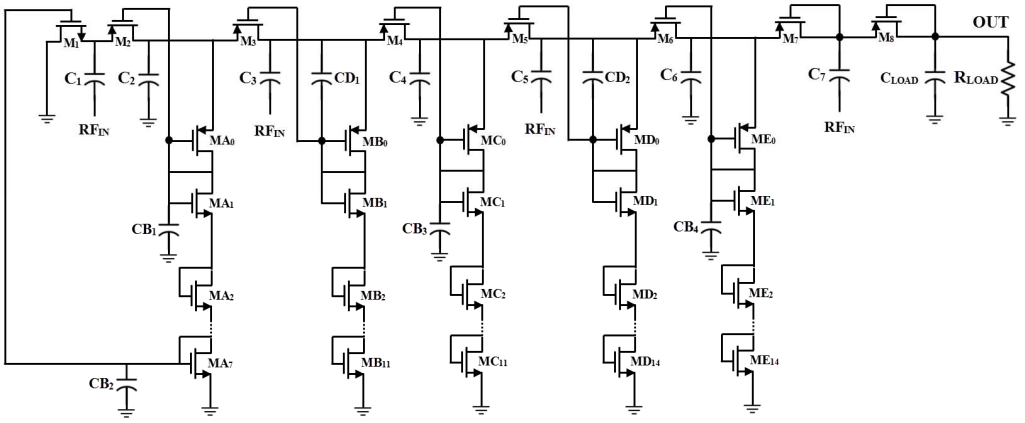

Fig. 2. Schematic of the proposed compensation scheme

be minimized. Leakage current is proportional to the number of diode connected transistors in the voltage divider. Therefore, the number of diode connected transistors should be chosen in a way to guarantee the satisfactory performance for the rectifier in the desired range of input power. *W/L* is the size of auxiliary transistors of MA_0, MB_0, MC_0, MD_0 and ME_0. By choosing the proper size for the auxiliary transistors of MA_0, MB_0, MC_0, MD_0 and ME_0 the compensation voltage around $V_{TH}/2$ can be produced.

III. Simulation Results

In order to find the performance of the proposed RF-DC power converter, the proposed structure with a proper L-section matching network is simulated in a standard IBM 0.13-µm metal CMOS process with eight layers of metallization. The simulation is performed at the frequency of 915MHz which is the center frequency for the industrial, scientific and material (ISM) band bounded by 902 and 928 MHz.

Targeting the maximum PCE, four-stage of voltage doubler equivalent to eight-stage rectifier is selected. Width of PMOS transistors ($M_{2\text{-}8}$) is chosen 10 um. Width of NMOS transistor (M_1) is selected to be 4.5um. Coupling capacitor value of 4pF is selected. The number and size of diode connected transistors in the voltage dividers are chosen to minimize the power consumption of the voltage dividers up to -7dBm input power for a 1 MΩ load and provide the appropriate compensation voltage. Fig 3 depicts the compensation voltage created for each transistor at different input power levels for the proposed design. It can be seen that by applying this technique for each power level almost constant compensation voltage is created for all transistors. The compensation voltage only changes by 50 mV as the input power level increase from -23 to -2 dBm. Fig. 4 shows the post layout simulation of the PCE of the proposed rectifier as the function of input power for different load resistance. As seen in Fig. 4, the proposed rectifier obtains a maximum PCE of 52.27% at an input power of -10 dBm (100 µW) with an output DC voltage of 7.23V for a 1MΩ load. As the load resistance decreases, the peak conversion efficiency shifts to the right. The maximum PCE for load impedances of 500 kΩ and 300 kΩ is 62.24% and 53.8% at input powers of -7 dBm and -4dBm respectively. Simulation demonstrates a -22.3 dBm sensitivity for obtaining an output voltage of 1V with a 1

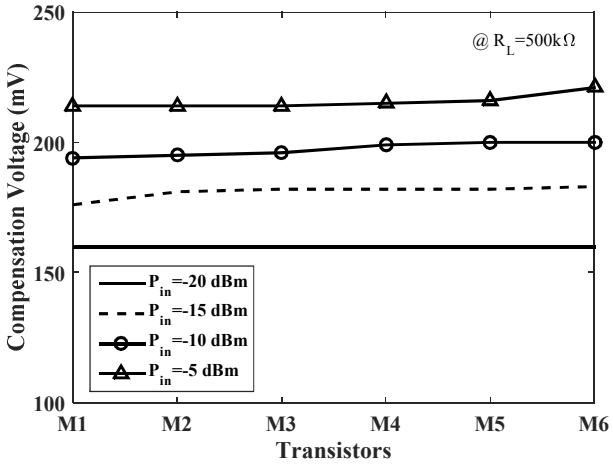

Fig. 3. Generated compensation voltage at different input power levels for each transistor.

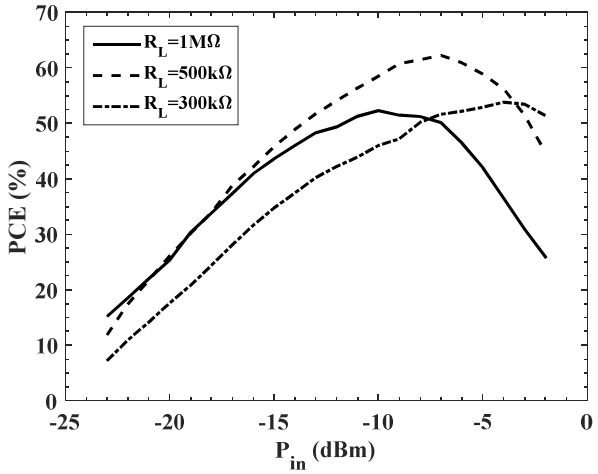

Fig. 4. Simulated PCE versus input power for different loads.

MΩ load. This work demonstrates a PCE of above 20% for high input power range of more than 20 dB for all 1 MΩ, 500 kΩ, and 300 kΩ load resistances. The active area of the proposed circuit

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TABLE I. PERFORMANCE SUMMARY AND COMPARISON

	This work*	**TCAS I '15** [5]	**JSSC '14** [8]	**JSSC '11** [3]	**TCAS II '17** [7]
Technology	130 nm	130 nm	90 nm	90 nm	65 nm
Frequency	915 MHz	915 MHz	868 MHz	915 MHz	900 MHz
Effective area	0.053 mm^2	0.25 mm^2	0.029 mm^2	0.19 mm^2	0.048 mm^2
No. of stages	4	12	5	17	5
Peak PCE & PCE at different input powers	Peak: 52% @-10 dBm	Peak: 32% @-15dBm	Peak: 24% @-21dBm	Peak: 11% @ -18.83dBm	Peak:36.5% @ -10dBm
	43.6%@-15dBm	18%@-10dBm**	10%@-11dBm**	3.5%@-10dBm**	20%@-5dBm
	25.3%@-20dBm	17%@-20dBm**	18%@-15dBm**	9%@-15dBm**	20%@-16dBm
Voltage Sensitivity: 1 V for R_L	-22.3 dBm	-20.5 dBm	-23 dBm	-17.5 dBm**	-16 dBm
High-PCE Range***	20 dB	7.5 dB	12 dB**	N.A.	11 dB
Load	R_L = 1 MΩ	R_L = 1 MΩ	R_L = 1 MΩ	R_L = 1 MΩ	R_L = 147 kΩ

* Post-layout simulation results, ** Estimated from the figure, *** PCE above 20%.

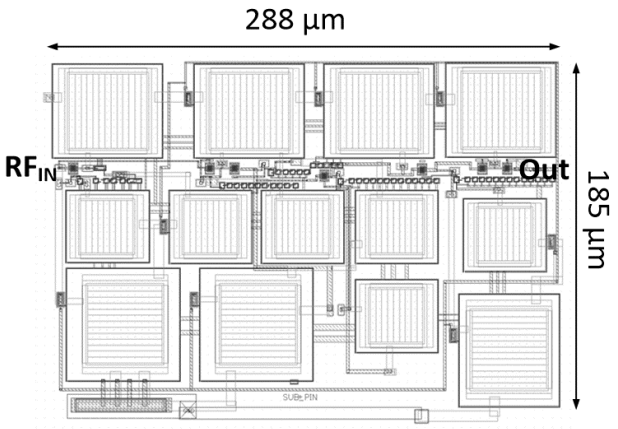

Fig. 5. Layout of the proposed structure.

excluding the L-section impedance matching network is 288 µm × 185 µm, as shown in Fig. 5.

IV. DISCUSSION AND PERFORMANCE COMPARISON

Table I summarizes the proposed RF-DC converter and compares it with other works. Apart from the occupying small silicon area, not requiring PCB balun or differential antenna or special transistors in CMOS process, proposed technique offers a higher PCE for a wider range of input powers in comparison to other structures because it uses the minimal number of stages and creates a relatively constant gate voltage drop for a wide range of input powers while the amount of the compensation in other circuitry are highly dependent on the input power. The peak PCE of 52.27% and PCE of greater than 20% for an input power range of more than 20 dB for a load resistance of 1 MΩ is among the highest reported in the literature.

V. CONCLUSION

A highly power efficient RF-to-DC power converter for energy harvesting systems has been presented, and the proposed design is simulated in 130 nm CMOS technology to verify the performance. The proposed rectifier achieves the maximum PCE of 52.27% at -10 dBm of input power when driving a 1MΩ load. The simulated PCE maintains above 20% for an input power of -21.5 dBm to -2 dBm. The proposed circuit exhibits the sensitivity of -22.3 dBm to generate 1V across a 1MΩ load.

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