Power Management Design for Lab-on-chip Biosensors

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***Abstract*— Over the past decades, we have witnessed the growth demands of portable lab-on-chip biosensors. These lab-on-chip devices are mostly powered by battery, and intelligent power management systems are required to provide supply voltage for different functional units on biosensors (e.g. a microfluidic control system might require higher voltage than the rest working units of biosensors). In this paper, a fully integrated multiple-stage voltage multiplier is proposed to provide high-voltage power needs. The proposed design was implemented with the IBM's 0.13um CMOS process with a maximum power efficiency of 81.02% and maximum voltage conversion efficiency of 99.8% under a supply voltage of 1.2 V.**

I. Introduction

With the increase of integration of different modules on the system-on-chip (SoC), the demand for integrated power management with multiple output voltages is increasing. Using off-chip power supplies increases the volume and cost of the system, and decreases the performance of the system due to the separation of package powers planes [1]. Therefore, fully integrated voltage converters are strongly recommended. In the previous research [1] [2], fully integrated step-down DC-DC converters have been reported in low-power applications. For applications such as lab-on-chip devices, higher voltage is required to provide enough driving capability. With the development of CMOS process and the decrease of the transistor sizes, the nominal voltage supply has reduced to around 1V. As a result, step-up DC-DC converters are needed to provide enough driving voltage that is larger than the nominal supply voltage of CMOS technology for these applications. In our research, we will present a step-up switched-capacitor DC-DC converter dedicated for lab-on-chip biosensors.

In general, there are two types of step-up DC-DC converters, switching mode converters and switched-capacitor (SC) converters. Conventional switching mode converters can achieve high efficiency, but require bulky and low-loss inductor, and are difficult to integrate on a single chip. In addition, the switching mode converters also suffer from EMI noise introduced by inductors [3], which makes them not suitable for deployment in noise-sensitive environments. In contrast to switching mode converters, SC converters only require capacitors to boost up output voltage. Current commercial CMOS process provides high-quality on-chip capacitors, which make it much easier to design a fully integrated SC converter than a switching converter. In addition, SC converter has a lower intrinsic conductive loss for a given rating of switch volt-ampere product compared to its inductive counterpart [4] [5].

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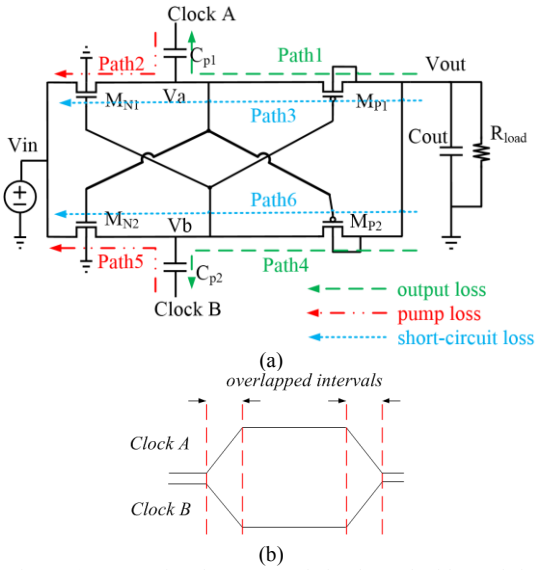


Fig. 1 (a) Conventional cross-coupled voltage doubler and six reversion loss paths.
(b) The overlapped intervals existing at clock transitions in conventional CCVD.

The most commonly used step-up SC converters are Dickson charge pump [6] and the Cross-coupled voltage doubler (CCVD) [7] as shown in Fig. 1. Compared to conventional charge pump, CCVD has several advantages. First, CCVD reduces the output voltage ripples and output voltage drop if the output buffer capacitors have the same capacitance. Second, in Dickson's charge pump, diodes or diode-connected MOSFETs are used as switches. As a result, the voltage drop across each switch is the threshold voltage V_{th}. In CCVD topology, the voltage drop is equal to the drain to source voltage V_{ds}, which is much less than V_{th}. However, the reversion loss during the clock transition time in this topology severely reduces the power efficiency [7]. The reversion losses mainly consist of three types of losses including the output loss, pump loss and short circuit loss, and six power-loss paths (refer to Fig. 1a). All these power losses appear at the clock transitions due to the overlapped clock signals or the timing mismatch [8], as shown in Fig. 1b. The output loss is caused by the reverse charge flow from the output capacitor to the flying capacitor during the falling transition of *Clock A* and rising transition of *Clock B*, and vise

versa, which illustrated as *Path 1* and *Path 4* in Fig.1. Similarly, the pump loss appears when the boosting node V_a and V_b transfer charges back to the input source during the rising clock transition intervals of *Clock A* or *Clock B*, which is labeled as *Path 2* and *Path 5* in Fig.1. The short-circuit power loss is induced by reverse charge from the output capacitor to the input source, because the M_{P1} and M_{N1} will be both turned on for a short time at the clock falling and rising transitions. The short-circuit loss is labeled as *Path 3* and *Path 6* in Fig.1.

Several techniques have been reported previously to reduce or eliminate the reversion power losses [7-10]. However, in these designs, either extra blocking transistors and level shifters are used, or potential voltage overstress exists. As a result, extra power is consumed and the power efficiency drops, or the stability of the circuit will decrease. Moreover, most of the previous designs cannot be scaled to multiple stages because either level shifter is used or some transistors suffer from voltage overstress. In this paper, an improved circuit design and the control scheme are proposed to eliminate the reversion power losses. Furthermore, the gate-to-source and source-to-drain voltages of each transistor are limited within the nominal supply voltage. As a result, such a design can be easily scaled to multiple stages without the voltage overstress issues.

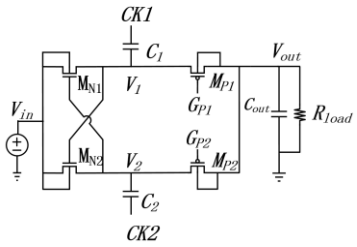
II. Proposed Circuit and Control Scheme

A. Single-Stage CCVD Topology

In order to improve the efficiency of CCVD, all of the 6 reversion loss paths in Fig.1 must be removed. In order to remove power loss along *Path 1*, M_{P1} must be turned off before *Clock A* goes low. Similarly, M_{N1} must be turned off before *Clock A* goes high to remove power loss along *Path 2*. To remove power loss in *Path 3*, M_{P1} and M_{N1} cannot be turned on at the same time during the clock transition. Since the structure of CCVD is symmetric, the other three loss paths can be removed in the same way.

The two charge-transfer transistors M_{N1} and M_{P1} must be driven separately to avoid simultaneous conduction at the clock transition to eliminate the short-circuit power loss, producing a circuit shown Fig. 2(a). The gate-drive signals at nodes V_1, V_2, G_{P1} and G_{P2} should be non-overlapping as shown in Fig. 2b to eliminate pump loss and output loss. Based on this control scheme, V_2 turns off M_{N1} before *CK1* goes high, and the transistor M_{P1} will be turned off by G_{P1} before *CK1* becomes low. Therefore, the reversion loss *Path 1* and *Path 2* are eliminated. Since M_{N1} and M_{P1} are never turned on at the same time according to the waveforms of node G_{P1} and V_2, the reversion loss along *Path 3* is also removed. *Path 4 – Path 6* will also be removed due to the symmetry of the circuit.

Based on above analysis, an improved design and its clock scheme are presented that satisfy the gate drive signals in Fig. 2b, respectively. The schematic and the clock scheme are shown in Fig. 3a and Fig. 3b. In this design, the bulk of NMOS and PMOS transistors are all connected to their sources. Since the bulk of NMOS transistors are biased at different voltages, the triple-well NMOS transistors are used in this design. The four non-overlapping clocks, *CK1, CK2,*



(a) Charge-transferring NMOS and PMOS must be driven separated to eliminate reversion loss.

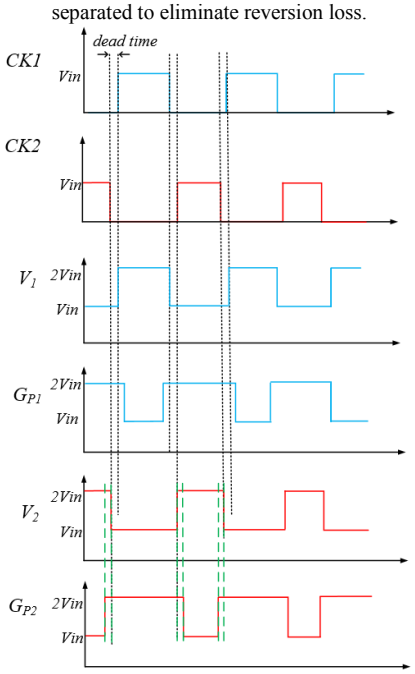


Fig.2 (b) Control scheme of non-overlapping gate-drive signals.

CKA and *CKB* are applied to generate the four gate-drive signals (refers to V_1, V_2, G_{P1}, and G_{P2}) shown in Fig. 2b.

In order to avoid any breakdown issues, the V_{gs}, V_{gd} and V_{ds} voltage of the transistors must not exceed V_{dd}. In the worst case that V_{in} is equal to V_{dd} and the output is unloaded, the two gate drive signals G_{P1} and G_{P2} must swing within a range from V_{dd} *to* $2V_{dd}$ (note: the maximum ideal voltage of V_{out} in Fig. 2b is $2V_{dd}$) to turn on or turn off M_{P1} and M_{P2}. If the CCVD converters are cascaded to make *N* stages of CCVD, the drive signals G_{P1} *and* G_{P2} in the *nth* stages should swing within the range from nV_{dd} *to* $(n+1)V_{dd}$. Consequently, the level shifters in [7] and [9] are not applicable to drive M_{P1} and M_{P2} because the level shifters in these designs can only provide a voltage swing from $0 \sim NV_{dd}$. It may cause oxide breakdown issues if the level shifters are used to drive the PMOS transistors M_{P1} and M_{P2} in Fig.3a. In the proposed design, two auxiliary clock signals *CK A* and *CK B* are connected to two small auxiliary capacitors C_A and C_B to achieve driving signals G_{P1} *and* G_{P2} swinging from V_{dd} *to* $2V_{dd}$. Likewise, in a multiple-stage CCVD, the driving singals G_{P1} and G_{P2} in *nth* stage swing from nV_{dd} *to* $(n+1)V_{dd}$, eliminating the overstress of the gate-to-source/drain voltage across the transistors.

In order to generate the four non-overlapping clock signals that satisfies the control scheme in Fig.3(b), an on-chip clock circuit is presented in Fig.4. The structure of the clock circuit is very simple. It consists of a voltage-controlled ring oscillator, four delay cells, and several logic gates. The

delaytime of the first two delay cells and the second two delay cells are 1 ns and 0.5 ns, respectively. In the first stage, two NOR gates and two delay cells are used to generate two non-overlapping clock signals V_{d1} and V_{d2}. The dead time of these two signals are 1 ns. In the second stage, another two delay cells are applied to produce four non-overlapping signals, and the dead time between CK1 and CK2, CK1 and CKA, CK2 and CKB are all 0.5 ns, producing waveforms depicted in Fig.3(b).

B. Multistage CCVD Topology

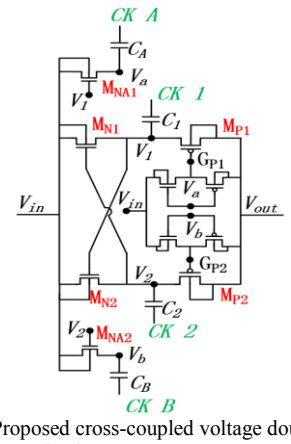
The single-stage CCVD can be cascaded to obtain higher output voltage. As a result, N stages of CCVDs can provide an output voltage of $(N+1)*V_{dd}$ if no load is applied at the output. Fig.6 demonstrates a three-stage CCVD design based on the proposed single-stage CCVD, in which three CCVDs are cascaded. Since the reversion loss in every stage has been removed, this design has a higher power efficiency and voltage conversion efficiency than conventional design.

Similar cascaded multiple-stage CCVD was proposed by Ker [11], as shown in Fig.5. However, the reversion losses are not eliminated in this design because overlapped clock signals are applied. As a result, in Ker's design, the output voltage drop is larger than our design, and the power efficiency is also lower. In addition, even though the gate-to-source voltage or the gate-to-drain/source voltage of each transistor does not exceed V_{dd} in Ker's design, the source-to-drain (V_{ds}) voltage may still exceed V_{dd} during the clock transitions or slight timing mismatch. For example, in Fig.5, when CLK becomes low and CLKB goes high, the transistor M_{P1} in the first stage and the transistor M_{N2} in the second stage may not be turned off at the same time. If M_{N2} is turned off before M_{P1}, the source-to-drain voltage across the M_{N1} may exceed V_{dd}, which may cause reliability issues. However, in the proposed design and control scheme shown in Fig.5 and Fig.3, the transistor M_{P1} in the first stage and transistor M_{N2} in the second stage are both turned off before CK2 goes high and CK1 goes low. As a result, the source-to-drain voltage drop across both M_{P1} and M_{N1} does not exceed V_{dd}. Therefore, the proposed design is more robust than Ker's design by taking the gate-oxide and source-to-drain reliabilities into consideration. In addition, an output capacitor (i.e., C_{out1} and C_{out2} in Fig. 6) can be added at the end of each stage to obtain multiple outputs with different voltage levels.

III. Simulation Results

As shown in Fig.7, the proposed single-stage and three-stage CCVD structure have been implemented using IBM's 0.13um process with active area of 0.37 mm^2 and 1.07 mm^2, respectively. Each stage operates with two main flying capacitors of 100 pF, two auxiliary flying capacitors of 5pF and the output capacitor is 200 pF. All of the capacitors are on-chip capacitors. The CCVDs work at a frequency of 50MHz and the input voltage supply is 1.2V. Two three-stage voltage doublers based on the design in [11] [12] with the same size of transistors and capacitors are also simulated and compared with the proposed design.

The maximum unloaded output voltage of the proposed design is 4.79 V, which is 99.8% of the ideal output voltage (i.e., 4.8 V). The maximum unloaded output voltage of the design in [11] is 4.67 V, with a ratio of 97.3%. The quiescent



(a) Proposed cross-coupled voltage doubler.

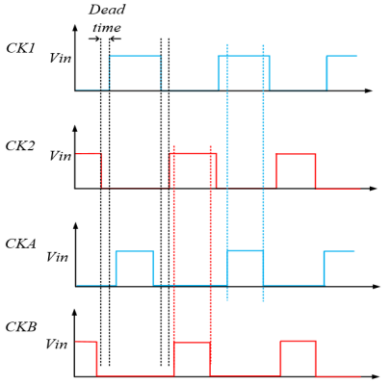


Fig.3 (b) Control scheme for the proposed voltage doubler.

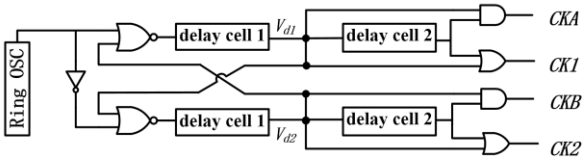


Fig.4 Clock generation circuit

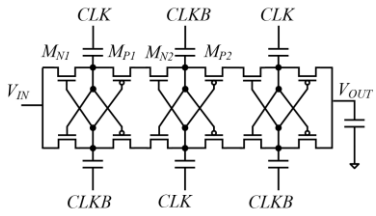


Fig. 5 Three-stage voltage multiplier based on design in [11]

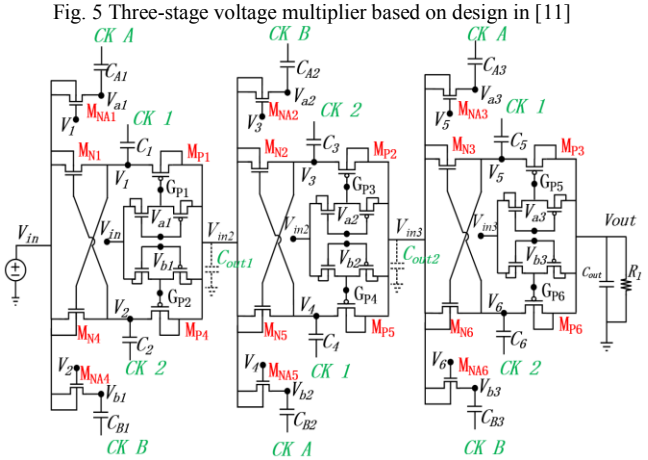


Fig. 6 Proposed three-stage CCVD topology.

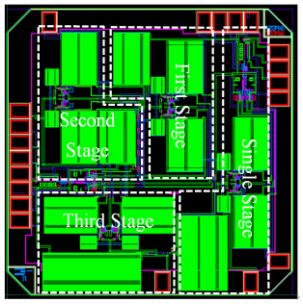


Fig.7 Layout of three-stage and single-stage CCVD.

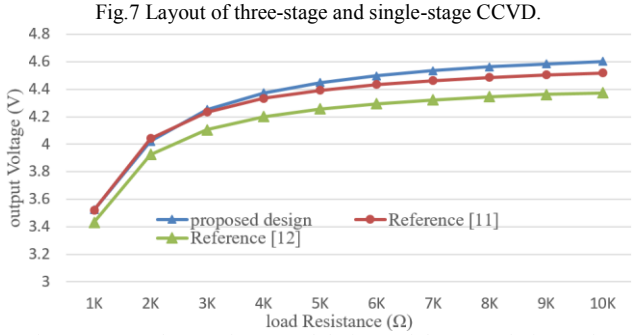


Fig.8 Output voltages of proposed design and the Ker's design under different load resistance

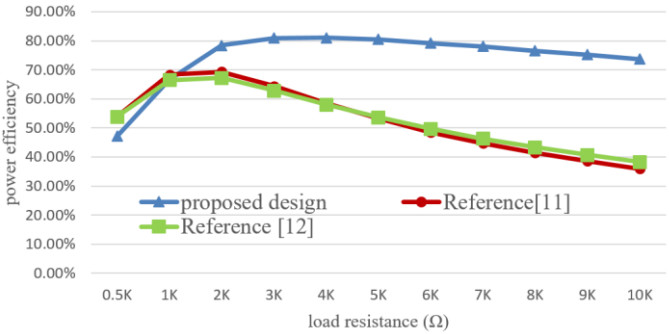


Fig.9 Power efficiency of proposed design and Ker's design under different load resistances

power consumption in the proposed design and [11] are 479 *uW* and 3.792 *mW*, respectively. Fig.8 compares the simulated output voltages of the proposed design and the designs of [11] and [12] under different load. The output voltages of the proposed design are 120 mV higher than that in [11] at most. As shown in Fig.9, the power efficiency of the proposed design is also much higher than the designs in [11] and [12]. The simulation results show that the proposed design improves the power efficiency significantly by eliminating the reversion loss. The maximum power efficiency of the proposed design, [11] and [12] are 81.02%, 69.29% and 67.18%, respectively. In addition, the power efficiency of the proposed design is around 80% with a large range of load resistance. However, the design based on [11] and [12] has efficiency lower than 50% in a wide range of load resistance, especially in larger load resistance. Under a heavy load, both designs have a low output voltage due to the relatively small on-chip capacitors. The power efficiency also drops at heavy load, because the low output voltage in each stage makes the transistors unable to be completely turned on or turned off. As a result, the on-resistance and leakage current of the transistors increase, and thus significantly decrease the power efficiency. However, the proposed design can achieve high power efficiency than other designs when the load is higher than 1 KΩ.

IV. Conclusion

In this paper, a new fully integrated three-stage cross-coupled voltage multiplier and control scheme are proposed. The presented structure eliminates all of the reversion power loss by using four non-overlapping clock signals. We implemented the design in 0.13um IBM CMOS process. The simulation results show a higher output voltage and power efficiency with a large range of load. The maximum output voltage and power efficiency of the proposed design is 4.79 V and 81.02%, respectively. Since this design does not require any extra level shifter circuit and both of the gate-to-source/drain voltage and drain-to-source voltage do not exceed the nominal supply voltage, this design is scalable to even more stages to obtain higher output voltages.

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