A NOVEL MATRIX-BASED LUMPED-ELEMENT ANALYSIS METHOD FOR CMOS DISTRIBUTED AMPLIFIERS

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ABSTRACT

This paper presents a novel matrix-based lumped-element theoretical analysis of CMOS distributed amplifiers that employ the image impedance technique for the input/output terminating networks. The design of distributed amplifiers can be more efficient in CMOS technology by using lumped-element modeling of the distributed amplifiers rather than the one commonly used for microwave distributed amplifiers that is based on transmission line parameters. The simulation results clearly indicate an improved voltage gain and a better gain uniformity over the bandwidth of the proposed amplifier design. Moreover, this matrix-based lumped-element method is suitable for analysis of any distributed amplifier with an arbitrary terminating network.

1. INTRODUCTION

A distributed integrated circuit design is one of the effective approaches for the design of optical communication ultra-wideband circuits, particularly in CMOS technology [1]. Wide-band preamplifiers and gain-controlled amplifiers (or limiting amplifiers) are the key building blocks of optical receivers [2]. Since distributed amplifiers (DAs) have no gain-bandwidth trade-off, unlike other amplifier configurations, they can offer wide-band amplification for fiber-optic receivers. As a candidate technology for implementation, CMOS continues to be used at higher frequencies for optical communication applications [3]. Implementation of the analog and digital building blocks of a receiver on a single CMOS chip leads to an integrated solution for optical receivers. Several successful implementations of DAs in CMOS technology have been reported in 0[6][7][8]. Bringing the distributed amplification technique to CMOS technology necessitates some essential changes both in analysis and design, since CMOS interconnects with lengths up to 100μm are not considered to be distributed elements, even at frequencies of tens of gigahertz. This paper presents a new matrix-based lumped-element analysis that is more intuitive for analog circuit designers than the transmission line analysis adapted from microwave amplifiers analysis. The analysis results in a closed-form equation for the amplifier transfer function which can be used for optimization or customization of the amplifier's specifications.

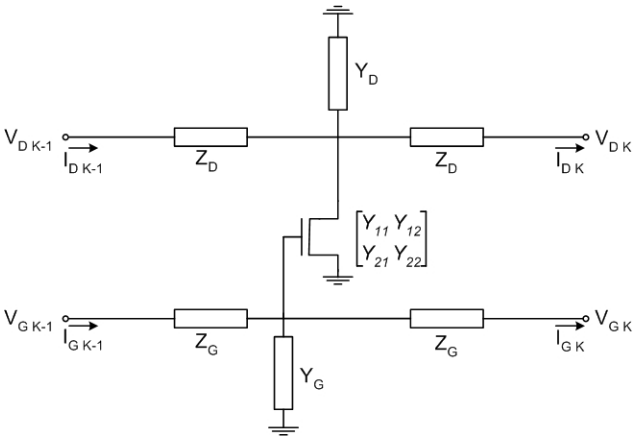

Figure 1. Stage K of a symmetrical N-stage distributed amplifier.

2. DA ABCD TRANSMISSION MATRIX

Figure 1 illustrates a stage (stage K) of a symmetrical N-stage DA. An ABCD Transmission matrix is an effective representation for the analysis of cascaded networks, since the overall ABCD matrix of the network can be simply computed by multiplying the ABCD matrices of the cascaded stage. Starting at the same point as the analysis reported in [4], an ABCD transmission matrix for each stage of amplifier is defined as follows:

$$\begin{bmatrix} V_{Dk-1} \\ I_{Dk-1} \\ V_{Gk-1} \\ I_{Gk-1} \end{bmatrix} = \begin{bmatrix} D_{11} & D_{12} & D_{13} & D_{14} \\ D_{21} & D_{22} & D_{23} & D_{24} \\ D_{31} & D_{32} & D_{33} & D_{34} \\ D_{41} & D_{42} & D_{43} & D_{44} \end{bmatrix} \begin{bmatrix} V_{Dk} \\ I_{Dk} \\ V_{Gk} \\ I_{Gk} \end{bmatrix}, \qquad (1)$$

where the voltages and currents are denoted in Figure 1. The DA ABCD matrix can be rewritten as a product of the transmission matrices of the transmission lines and

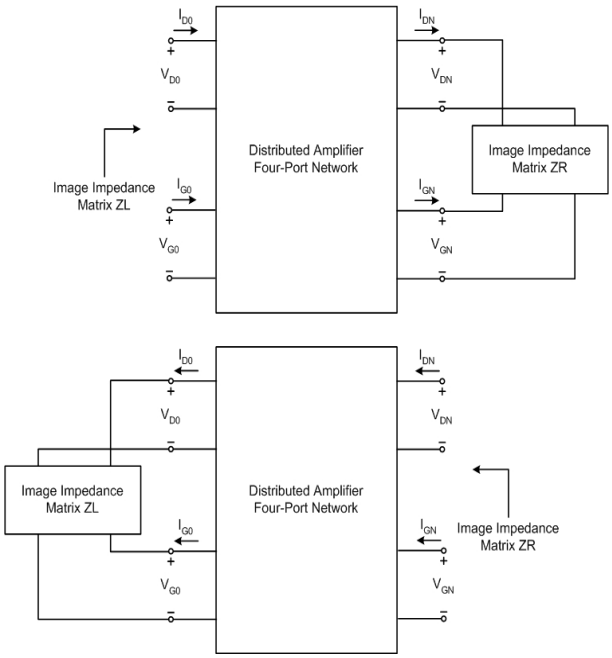

Figure 2. Right and left image impedance matrices of a distributed amplifier.

transistors as

$$D = A_1 A_2 A_1 , \tag{2}$$

where the transmission matrix of the artificial transmission lines is given by

$$A_1 = \begin{bmatrix} 1 & Z_D & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & Z_G \\ 0 & 0 & 0 & 1 \end{bmatrix}, \tag{3}$$

and the transmission matrix of a MOS transistor, including the admittances of gate and drain transmission lines, is:

$$A_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ Y_{22} + Y_D & 1 & Y_{21} & 0 \\ 0 & 0 & 1 & 0 \\ Y_{12} & 0 & Y_{11} + Y_G & 1 \end{bmatrix}, \tag{4}$$

where Z_D, Z_G, Y_D, Y_G are the impedances and admittances of the drain and gain transmission lines, and Y_{11}, Y_{12}, Y_{21}, Y_{22} are the transistor's admittance matrix parameters. The most important properties of the ABCD matrix stem from the fact that the amplifier network is reciprocal. If the directions of the currents are modified toward the network, the inverse of the resulting ABCD matrix should be equal to itself ($\boldsymbol{D'^{-1} = D'}$), where

$$D' = \begin{bmatrix} D_{11} & -D_{12} & D_{13} & -D_{14} \\ D_{21} & -D_{22} & D_{23} & -D_{24} \\ D_{31} & -D_{32} & D_{33} & -D_{34} \\ D_{41} & -D_{42} & D_{43} & -D_{44} \end{bmatrix}. \tag{5}$$

Also, the reciprocity condition also implies that amplifier's impedance, admittance, and scattering matrices are symmetric (i.e. $Z_{ij} = Z_{ji}, Y_{ij} = Y_{ji}, S_{ij} = S_{ji}$).

If the transistor is assumed to be unilateral, i.e. $Y_{21} = 0$, the following conditions must be met in order to have the above matrix equal to its reverse:

$$\begin{aligned} &D_{31} = D_{32} = D_{41} = D_{42} = 0, \\ &D_{11} = D_{22}, D_{33} = D_{44}, \\ &D_{21} = (D_{11}^2 - 1)/D_{12}, \\ &D_{34} = (D_{33}^2 - 1)/D_{34}, \\ &D_{13} = (-D_{11}D_{14} + D_{12}D_{24} + D_{14}D_{33})/D_{34}, \\ &D_{23} = (D_{14} - D_{11}^2 D_{14} + D_{12}D_{24}D_{33} + D_{11}D_{12}D_{24})/D_{12}D_{34}. \end{aligned} \tag{6}$$

It is evident that the elements of the DA ABCD matrix are not independent. In the derivation of the previous conditions, D_{11}, D_{12}, D_{14}, D_{24}, D_{33}, and D_{34} are considered to be independent variables, and the other matrix elements are calculated as the functions of these independent variables.

3. IMAGE IMPEDANCE MATRIX

The image impedance method is employed for the analysis and design of the periodical structure filters in [10]. This method can be applied to DAs because of their periodical structure. If the gate and drain lines are terminated at the scalar impedance Z_{IG} and Z_{ID} at the right ports, respectively, the equations can be written to obtain the impedance seen at the left ports, which must also be equal to Z_{IG} and Z_{ID} to satisfy the image impedance condition for DA network. It can be shown that this equation results in a none-zero mutual impedance between the gate and drain lines. This proves that there is no scalar image impedance for the DA structure; therefore, an image impedance matrix (IIM) is defined instead. As shown in Figure 2, the IIM ZL is the input impedance matrix of the left ports when the right ports are terminated in their IIM ZR and vice versa. Because of the reciprocity of the network, the two image impedance matrices are equal (***ZR = ZL = Z***). It is evident that the IIM of the one-stage amplifier is equal to that of the N-stage amplifier.

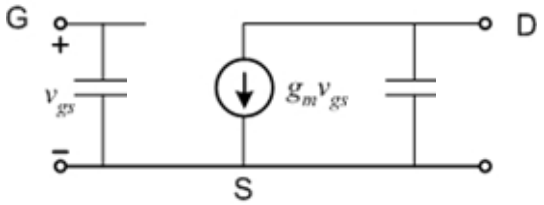

Figure 3. Basic NMOS transistor model combined with the gate and drain lines capacitance.

The elements of the IIM of a single-stage amplifier for the simple transistor model IIM (see Figure 3) can be calculated by equating right and left image as follows:

$$Z_{11} = \sqrt{\frac{2L_d - w^2 L_d^2 C_{ds}}{C_{ds}}},$$
$$Z_{22} = \sqrt{\frac{2L_g - w^2 L_g^2 C_{gs}}{C_{gs}}}, \quad (7)$$
$$Z_{21} = 0,$$

and

$$Z_{12} = gm[Z_{11}Z_{22} + jwL_dZ_{22} + jwL_gZ_{11} - w^2 L_d L_g]/$$
$$[w(wC_{ds}C_{gs}Z_{11}Z_{22} - jC_{gs}Z_{22} - jC_{ds}Z_{11} + jw^2 Z_{22}L_dC_{ds}C_{gs}$$
$$+ jw^2 Z_{11}L_gC_{ds}C_{gs} + wL_gC_{gs} + wL_dC_{ds} - w^3 L_dL_gC_{ds}C_{gs})].$$

4. VOLTAGE TRANSFER FUNCTION

The last step is to obtain the voltage transfer function (VTF) of the DA. Based on the definition of the IIM, if the DA's right ports are terminated at their IIM, the input impedance matrix seen at the left ports is equal to IIM (***Z***). Now if ports G_0 and D_0 are terminated at Z_{11} and Z_{22} respectively, their voltages and currents can be obtained as the functions of the DA's input voltage (V_{in}) as follows:

$$\begin{bmatrix} V_{D0} \\ I_{D0} \\ V_{G0} \\ I_{G0} \end{bmatrix} = \begin{bmatrix} \frac{Z_{12}}{4Z_{22}} \\ \frac{-Z_{12}}{4Z_{11}Z_{22}} \\ \frac{1}{2} \\ \frac{1}{2Z_{22}} \end{bmatrix} V_{in}. \quad (8)$$

Transforming the left ports' voltages and currents to the right ports' voltages and currents using (1), they can be calculated by

$$\begin{bmatrix} V_{DN} \\ I_{DN} \\ V_{GN} \\ I_{GN} \end{bmatrix} = (D^N)^{-1} \begin{bmatrix} \frac{Z_{12}}{4Z_{22}} \\ \frac{-Z_{12}}{4Z_{11}Z_{22}} \\ \frac{1}{2} \\ \frac{1}{2Z_{22}} \end{bmatrix} V_{in}, \quad (9)$$

where N is the number of amplifier stages. Consequently, the voltage transfer function of the amplifier is V_{DN}/V_{in}. This analysis is also applicable to any DA with an arbitrary terminating network.

5. SIMPLE TRANSISTOR MODEL SIMULATION RESULTS

A simple transistor model is adapted for the simulation of the VTF of the DA, while the output resistance of the transistor is ignored. Figure 3 depicts this transistor model that includes the transistor's transconductance (g_m) and the intrinsic transistor capacitance that combined with the transmission lines capacitance to form C_{ds} and C_{gs}. Note that that the body and the source of the NOS transistor are connected together. The on-chip inductors are assumed to be ideal in this simulation (a very high quality factor). According to the image impedance theory [10], the bandwidths of the gate and drain lines are $\sqrt{2/(L_gC_{gs})}$, and $\sqrt{2/(L_dC_{ds})}$, respectively, which will be the amplifier bandwidth if $L_gC_{gs} = L_dC_{ds}$.

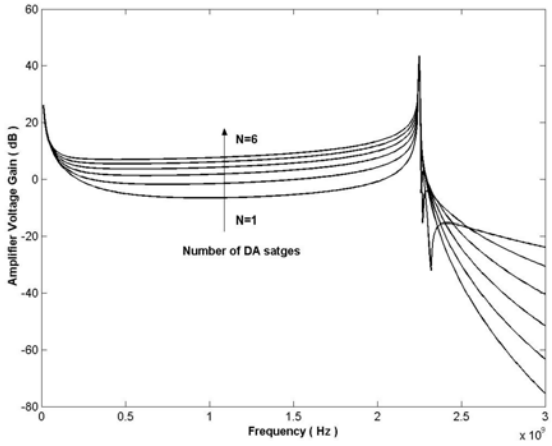

Figure 4. Amplifier voltage gain as a function of frequency for a DA with IIM terminating networks.

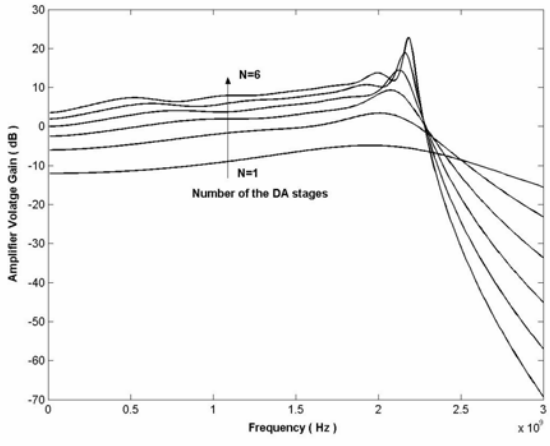

Figure 5. Amplifier voltage gain as a function of frequency for a DA with matching terminating networks.

In this simulation, the values of gm, L_d, L_g, C_{ds}, and C_{gs} are chosen to be 100 mA/V, 1 nH, 1 nH, 10 pF, and 10 pF, respectively. From a design perspective, the ratio of $L_g C_{gs}$ or $L_d C_{ds}$ must be minimized to achieve the largest possible bandwidth. The minimum values of C_{ds} and C_{gs} are limited to the intrinsic capacitance of the transistors, whereas the practical values of the on-chip spiral inductors in CMOS technology are in the range of few nHs. The simulation results, shown in Figure 4, indicate that the gain and the gain uniformity are improved by increasing the number of amplifier stages at the cost of using a greater die area.

To compare the results of the proposed design with those of the conventional design, a same matrix-based analysis is also used for DA modeling. Here the DA ports are connected to the matching impedances of the gate and drain transmission lines, i.e., $\sqrt{L_g/C_{gs}}$ and $\sqrt{L_d/C_{ds}}$. The simulation results for 1-stage to 6-stage amplifiers with matching terminating networks are shown in Figure 5. It is obvious that the gain and gain uniformity is improved in the new design. Figures 6 and 7 illustrate the simulation results for the elements of the IIM as functions of the frequency. Note that Z_{11} and Z_{22} are real impedances (pure resistors) within the amplifier's bandwidth, but an pure imaginary impedance elsewhere, whereas Z_{12} is an imaginary impedance within the amplifier's bandwidth, and is a resistive impedance elsewhere.

7. CONCLUSIONS

In this paper, a novel matrix-based lumped-element analysis/design method is developed for CMOS DAs. The new DA design, based on the image impedance technique, provides a higher voltage gain and a better gain uniformity than the design using transmission line matching method. This matrix-based analysis method is more appropriate for circuit designers by providing closed-form formula for the amplifier's figures of merit as functions of the amplifier's lumped elements. The analysis results can be used for the optimization or customization of the amplifier's specifications.

8. REFERENCES

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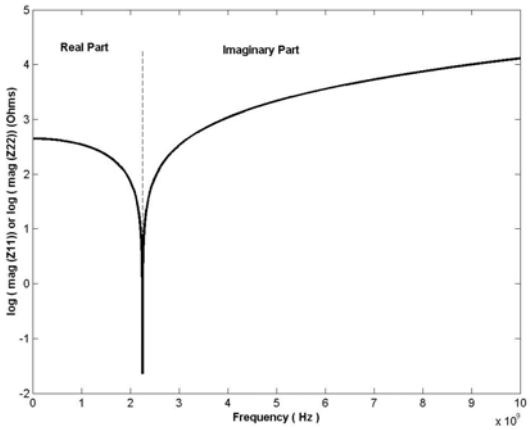

Figure 6. Magnitude of Z_{11}/Z_{22} as functions of frequency (logarithmic scale).

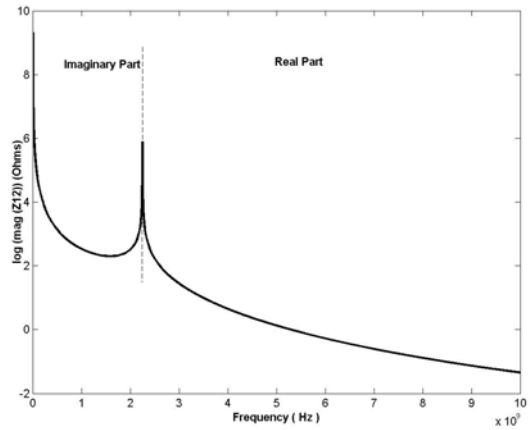

Figure 7. Magnitude of Z_{12} as a function of frequency (logarithmic scale).

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