A Dual-Mode Highly Efficient 60 GHz Power Amplifier in 65 nm CMOS

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***Abstract* — This paper presents a 60 GHz power amplifier utilizing a novel technique to achieve high efficiency at high output power levels. The proposed topology provides the capability of dual mode operation. The output power of a conventional class A power amplifier will be combined with the power provided by an amplifier operating at a different class to achieve higher efficiency at higher output levels. Driver stages to provide high power gain consist of an enhanced cascode stage followed by a common source amplifier with transformer-coupled impedance matching networks. Fabricated in 65 nm CMOS process, the measured gain of the 0.32 mm2 power amplifier is 17.7 dB at 60 GHz with a wide 3dB band width of 12 GHz while consuming 378 mW from a 1.2V supply. A maximum saturated output power of 16.8 dBm is measured with the 14.5% peak power added efficiency at 60 GHz.**

***Index Terms* — 60 GHz wireless communication, CMOS power amplifier, power added efficiency.**

I. Introduction

The ever-increasing demand for high data rate short-range wireless communication devices motivates the designers to develop new wireless devices capable of fulfilling these consumer demands. Driven by the need for higher data-rates, the continuous 7 GHz bandwidth around 60 GHz is a promising contender because it is unlicensed and well suited for high speed indoor wireless personal area network (WPAN) applications [1]. Electromagnetic energy of oxygen molecules is one particular feature of the 60 GHz band that increase the path loss at these specific frequency compared to lower GHz frequencies [1]. The signal attenuation requires millimeter wave (mmW) transmitter to transmit higher output powers than their low GHz counterparts in order for the receiver to successfully detect the transmitted signal. The need for high output power along with the operation of transistors near cut-off frequencies makes the design of 60 GHz power amplifiers (PA) very challenging.

Continuous scaling of CMOS technology has resulted in significant improvement of f_{max} enabling the low cost integration of 60 GHz front-ends on a single chip. Nevertheless, design of efficient CMOS PAs remains challenging because of low gain of transistors at these frequencies, low breakdown voltage of CMOS transistors and losses of on-chip passive power combiners in deep sub-micron CMOS process [1]. To date, there have been several CMOS PAs targeting high gain and output power at 60 GHz [2]-[11]. Considering the fact that the gain of the power MOSFETs with large channel width is relatively low at mmW frequencies, a single-stage PA cannot deliver a high gain and high power simultaneously [3]. Therefore, in all reported 60 GHz CMOS PAs, different power combining techniques such as using on-chip transformers, Wilkinson power combiners and distributed active transformers (DAT) are proposed to increase the output power of CMOS PAs [2]-[11]. However, the power combiners themselves cause additional losses limiting the maximum achievable output power and PAEs of CMOS PAs.

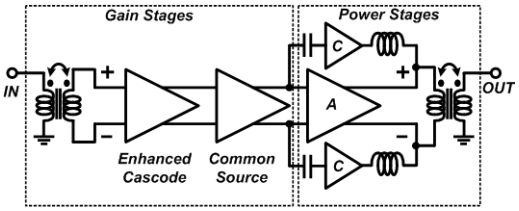


Fig. 1. 60 GHz PA building blocks.

This paper presents a differential 60 GHz PA topology with a novel circuit design technique which provides the ability of dual-mode operation at high-level output powers. A class C amplifier is designed in parallel with a conventional class A power stage to achieve higher level of power when the out stages are experiencing the power saturation. In addition to achieve a high power added efficiency (PAE), the driver amplifiers consist of an enhanced cascode stage followed by a common source stage, provide a high gain over a wide range of frequency.

II. Design of 60 GHz PA

The methodology for the design and implementation of 60 GHz PA based on the dual-mode technique is presented in this section. The block diagram of the proposed PA is illustrated in Fig. 1. A new circuit design technique is proposed to force the power stages to operate at higher efficiency when the amplifier drives by a high-power input. The amplifier stages are designed in differential mode to provide the ability of combining the output power of two individual PAs to achieve higher output power compared to the single-ended designs. The

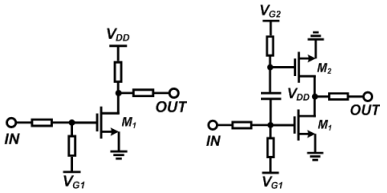


Fig. 2. Power amplifier stages, a) class A b) dual biased PA

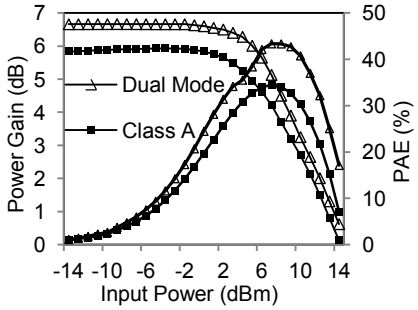


Fig. 3. Simulation results of the gain-efficiency tradeoff

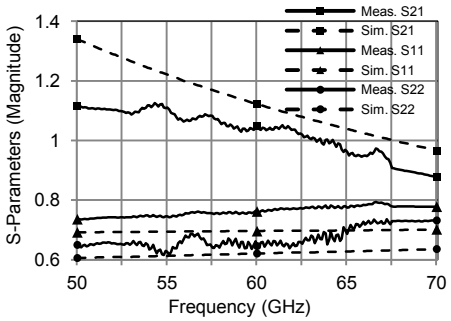


Fig. 5. Simulated and measured S- parameter of the power MOSFET.

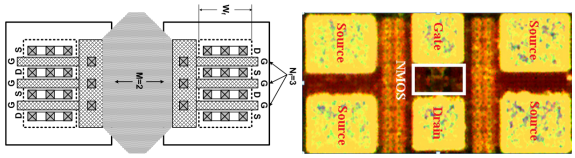


Fig. 4. Power MOSFETS. a) Multi-finger paralleled NMOS layout, b) Micrograph of a fabricated NMOS.

output power, gain, and the efficiency are the parameters which must be simultaneously optimized while designing a PA. Driver stages and gain stages are necessary to increase the total power gain of the amplifier. The output power and the PAE are determined by the current handling capability of the last stage of the PA core. Achieving high level of current using power MOSFETs with large channel width and low f_{max} is the main challenge.

A. Dual-Mode Power Stage

In order to achieve a high efficiency PA stage, a new topology based on the dual-mode operation is proposed as shown in Fig. 2.b. The most challenging aspect of designing the proposed technique was to choose a topology which can satisfy both the impedance transformation and the bias requirements. The proposed circuit consists of a main amplifier (M_1) which can provide linear class-A of operation at lower levels of input power and an auxiliary amplifier (M_2) with tunable class of operation when the gate biasing of the transistor M_2 can be controlled independently. Utilizing the new topology, the auxiliary stage can deliver more current when the main stage runs into the saturation mode.

A conventional class-A structure like Fig. 2.a is designed at 60 GHz band and simulated to be compared in terms of efficiency and gain. The power gain and PAE of a conventional class-A PA and the proposed circuit are compared in Fig. 3. In comparison with the same size conventional class-A topology, higher power gain and higher PAE is achieved for the proposed dual-biased PA as illustrated in Fig. 3. The other advantage of the

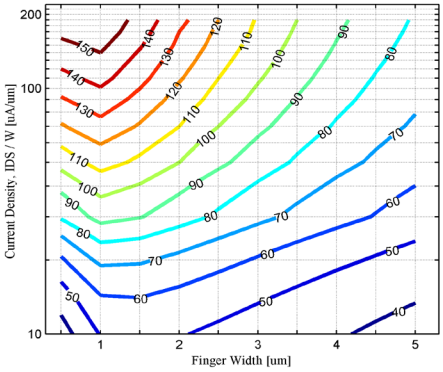


Fig. 6. F_{max} of n-MOSFETs for different current densities and channel widths (32 numbers of fingers).

proposed topology is the capability of tuning the auxiliary stage to operate at not only linear modes of operations, but also the non-linear modes can be realized by changing the V_{G2} from zero to V_{DD}.

B. Power stage transistors

In addition to lossy passive impedance transformers, a major challenge in the design of a fully integrated mmW PA is dealing with the low power gain of the large transistors which are used at such high frequencies [1]. The most important parameters that characterize the frequency dependant gain performances of a MOSFET are the cut-off frequency (f_T) and the maximum frequency of operation (f_{max}) [1]. In addition to this, a high level of output current is required for power amplifier application which poses the challenge of using transistors with large channel width. To achieve the wider channel width and higher current, the multi-finger parallel configuration must be used as shown in Fig. 4.a. Using multiple fingers is a common way in order to build high power MOSFETs. However, this has the negative effect that increasing the total number of fingers with a fixed finger width leads to a large layout. In this case, although the poly-silicon gate resistance per finger remains fixed, large inter-connections are needed to connect the gates and drains of multiple fingers, which cause additional resistive losses and leads

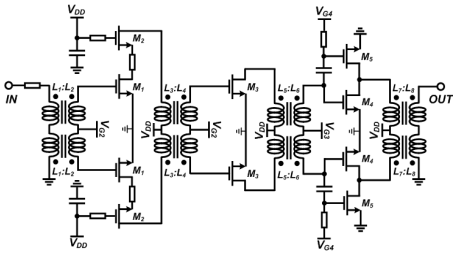
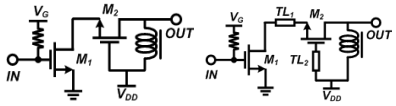


Fig. 7. Schematic of the 60 GHz power amplifier.



(a) (b)

Fig. 8. Cascode Amplifier, a) conventional, b) enhanced cascode.

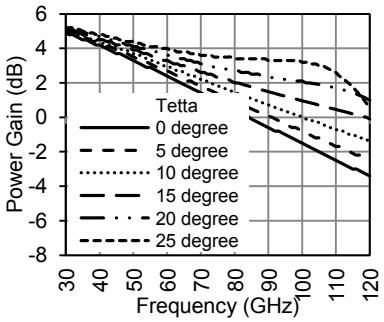


Fig. 9. Simulation results of the power-gain of conventional and enhanced cascode stages.

to a lower f_{max} and gain. In addition, the I/O impedances drop when the number of fingers is increased which leads to higher matching network losses because the higher transformation ratio is needed. Fig. 4.b presents a power MOSFET with 120 um channel width designed and fabricated in 65 nm CMOS technology. Simulation and measured S-Parameters of the fabricated MOSFET are illustrated in Fig. 5 to prove the large deviation between the measured and simulation models produced by the interconnects. Figure 6 presents the measured f_{max} for n-MOSFETS with various channel widths and current densities. According to Fig. 6, transistors with total gate width of 72 µm (30 numbers of fingers and 2.4 µm of finger width) have been chosen to keep the f_{max} above 60 GHz.

C. Gain stages and Inter-stage matching

The schematic of the 60 GHz CMOS power amplifier is presented in Fig. 7. To ensure a reasonable power gain at 60 GHz, the driver stage and the gain stage were cascaded before the main power stage. Cascode amplifiers followed by a common source (CS) stage are designed as driver and gain stages respectively. The transistors were laid out in 30 fingers with 2 µm wide fingers for the CS stage and with 30 fingers, 1 µm and 1.5 µm for Cascode transistors respectively. Bias conditions were set to achieve the maximum current density at frequencies near f_T. The gate bias (V_{GG}) voltage is set to be 0.8V while the supply voltage (V_{DD}) is 1.2 V for all the stages.

A compensation technique is used to enhance the gain performance of the cascode stage. Figure 8 shows a conventional cascode amplifier and the enhanced version with transmission lines (T-Lines) between the transistors connections (TL_1, TL_2). Figure 9 illustrates the simulation results for power gain and f_{max} of the enhanced cascode amplifier for different electrical lengths (θ). T-Lines have been optimized to get 20 GHz more fmax with θ of 10^o or 60 µm physical lengths. For inter-stage matching circuits, stacked transformers with conductor width of 6 µm were modeled in Advanced Design System (ADS) and fabricated on the M_9 and M_8 metal layers from input stage to the output with radii of 40 µm, 22 µm, 25 µm and 20 µm respectively. Utilizing the M_8 and M_9 metal layers, a coupling factor of 0.75 and maximum quality factor of 15 is achieved based on EM simulations. Simulated gain and I/O reflections of the 60 GHz PA are illustrated in Fig. 11.

III. MEASURED RESULTS

The proposed 60 GHz PA is fabricated in TSMC 1P9M 65nm CMOS process. The chip micrograph of the PA is shown in Fig. 10. The PA only occupies a core area of 0.32 mm^2. The S-parameter measurements are performed using Agilent N5251A solution and compared with the simulation results in Fig. 8. Applying 1.2V supply, a power gain of 17.7 dB is measured within the 3dB bandwidth of 12 GHz. With the stability factor of greater than unity, the amplifier is unconditionally stable over the frequency range of operation.

Power measurements have been performed using Rohde-Schwarz NRP-Z power sensors and the R&S ZVA67 VNA. The measured results are shown in Fig. 12. The measured 1dB compressed output power (P_{1dB}) is 15.5 dBm and the saturated output power (P_{sat}) is 16.8 dBm. The measured peak PAE is 14.5%. Compared to the reported 60 GHz PAs, the wide-band PA is a compact design with high PAE and P_{sat} while improving the linearity based on the measured 1dB compression point. Table. I summarizes a comparison with the state-of-the-art 60 GHz PAs in 65nm CMOS technology.

IV. CONCLUSION

A novel dual-mode CMOS power amplifier for 60 GHz applications has been proposed. Utilizing the dual-mode operation, the proposed PA provides higher efficiency at higher output power rates in comparison with the conventional class A amplification. The PA core consists

TABLE I

COMPARISON WITH PUBLISHED 60 GHZ PAS IN 65NM CMOS

60 GHz PAs in 65nm CMOS Technology	B.W. [GHz]	Stage	Architecture	P_{sat} dBm	P_{1dB} dBm	G_{max} dB	PAE_{max} %	P_{DC} [mW]	Size [mm^2]	Power/Area [mW/mm^2]	Ref.
	57-65	2	Single-ended/C.S	13	8.9	8	11	64.8	0.29	45	[2]
	58-65	3	Differential/C.S	11.5	2.5	15.8	11	43.5	0.05	230	[3]
	55-65	2	Differential/C.S/4x	17.9	15.4	18.6	11.7	460	0.83	22	[4]
	53-68	2	Single/Cascode/8x	18.1	11.5	15.5	3.6	1504	0.46	140	[5]
	55-65	1	Single-ended/C.S	9	6	4.5	9	27.6	0.27	29	[6]
	-	4	Single-ended/C.S	13.8	12.2	13.4	7.6	300	1.28	19	[7]
	59-67	2	Single-ended/C.S	10.6	9.2	13.2	8.9	80	0.29	40	[8]
	56-62	3	Differential/C.S	14.6	10	23.2	16.3	135	0.60	48	[9]
	58-64	3	Single-ended/C.S/2x	17.8	13.8	11	12.6	-	0.28	214	[10]
	54-66	3	Differential/C.S	16.8	15.5	17.7	14.5	378	0.32	160	This work

of an enhanced cascode driver stage followed by two cascaded common source stages with transformer-based inter-stage matching. The peak power gain of 17.7 dB and 16.8dBm saturated output power are measured over the 3dB bandwidth of 12 GHz. The 0.32 mm^2 die area consumes 378 mA from a 1.2V supply and presents 14.5% PAE at saturation.

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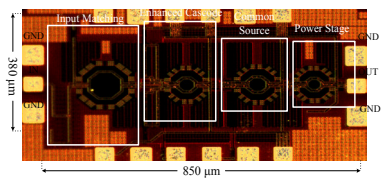

Fig. 10. Chip micrograph of the PA.

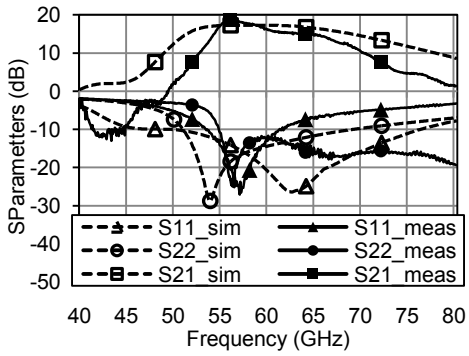

Fig. 11. Measured and simulated S-parameters

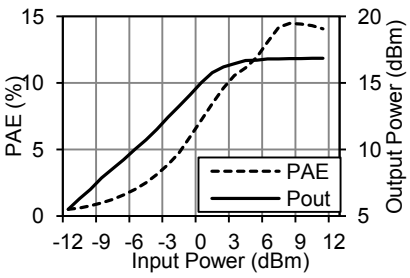

Fig. 12. Measured output power and efficiency