Compact High-Power 60 GHz Power Amplifier in 65 nm CMOS

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***Abstract*— This paper presents a compact 60 GHz power amplifier utilizing a novel 4-way multi-conductor power combiner and splitter. The proposed topology provides the capability of combining the output power of four individual power amplifier cores in a compact die area of 0.025 mm^2 with the advantage of lower insertion loss and higher efficiency compared to the conventional distributed active transformer topology. Each power amplifier core consists of a three-stage common-source amplifier with transformer-coupled impedance matching networks. Fabricated in 65 nm CMOS process, the measured gain of the 0.19 mm^2 power amplifier is 18.8 dB at 60 GHz with 3dB band width of 4 GHz while consuming 424 mW from a 1.4V supply. A maximum saturated output power of 18.3dBm is measured with the 15.9% peak power added efficiency at 60 GHz.**

I. Introduction

The ever-increasing demand for high data rate short-range wireless communication devices motivates the designers to develop new wireless devices capable of fulfilling these consumer demands. Driven by the need for higher data-rates, the continuous 7 GHz bandwidth around 60 GHz is a promising contender because it is unlicensed and well suited for high speed indoor wireless personal area network (WPAN) applications [1].One particular feature of the 60 GHz band is that the oxygen molecules absorb electromagnetic energy at these specific frequency at higher rate compared to low GHz frequencies [1]. The signal attenuation requires millimeter wave (mmW) transmitter to transmit higher output powers than their low GHz counterparts in order for the receiver to successfully detect the transmitted signal. The need for high output power along with the operation of transistors near cut-off frequencies makes the design of 60 GHz power amplifiers (PA) very challenging.

Continuous scaling of CMOS technology has resulted in significant improvement of f_{max} enabling the low cost integration of 60 GHz front-ends on a single chip. Nevertheless, design of efficient CMOS PAs remains challenging because of low gain of transistors at these frequencies, low breakdown voltage of CMOS transistors and losses of on-chip passive power combiners in deep sub-micron CMOS process [1]. To date, there have been several CMOS PAs targeting high gain and output power at 60 GHz [2]-[11]. Considering the fact that the gain of the power MOSFETs with large channel width is relatively low at mmW frequencies, a single-stage PA cannot deliver a high gain and high power simultaneously [3]. Therefore, in all reported 60 GHz CMOS PAs, different power combining techniques such as using transformers, Wilkinson power combiners and distributed active transformers (DAT) are proposed to increase the output power of CMOS PAs [2]-[11]. However, the power combiners themselves cause additional losses limiting the maximum achievable output power and PAEs of CMOS PAs.

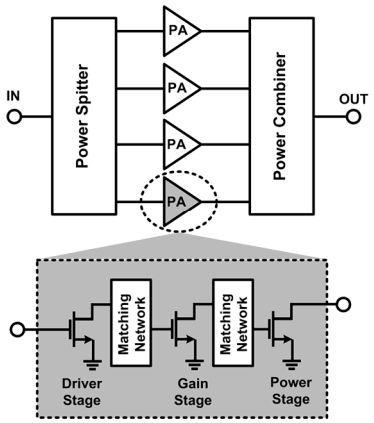

Fig. 1. 60 GHz PA building blocks.

This paper presents a 60 GHz PA topology with a novel multi-conductor transformer-based power combiner. The proposed topology provides a power combining solution in a compact area with minimum insertion loss. In addition to perform the power combining, the network matches the 50-Ω load to the optimum load impedance of the PA to maximize the power/gain performance as well eliminating the need of additional impedance matching networks.

II. Design of 60 GHz PA

The methodology for the design and implementation of 60 GHz PA based on the multi-conductor combiner is presented in this section. The block diagram of the proposed PA is illustrated in Fig. 1. A distributed 4-way parallel power combiner is proposed based on multi-conductor cross-coupled transformer architecture to combine the output current of the four individual PAs to achieve higher output power compared to the reported designers. The output power, gain, and the efficiency are the parameters which must be simultaneously

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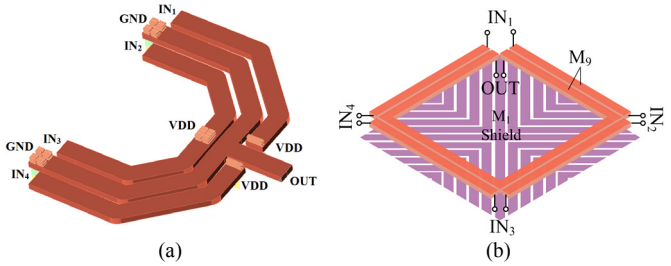


(a) (b)

Fig. 2. Power combiners. a) Proposed Topology b) Conventional DAT

optimized while designing a PA. The output power of the four PA cores is combined by a 4-way transformer-based power combiner. Each PA cores is constructed by cascading three stages of common-source amplifiers. The output power is determined by the current handling capability of the last stage of the PA cores. Driver stages and gain stages are necessary to increase the total voltage gain of the amplifier. Also, the power splitters are providing the necessary input power for the input stages. By the use of power combiner/splitter, a PA can be derived by high input power which is resulting in a higher output power than a single stage. The smaller transistors are needed because of the low input power of each PA core, so that the transistors can be designed for achieving high f_{max}.

A. Multi-conductor mmW power combiner

In order to combine the output power of the four separated PA cores, a 4-way multi-conductor transformer is proposed as shown in Fig. 2.a. The most challenging aspect of designing the transformer was to choose a topology which can satisfy both the impedance transformation and the bias requirements. The proposed topology can simultaneously provide impedance transformation, power combination, and biasing for the power transistors at output. Utilizing the multi-conductor topology, more electromagnetic waves can be prevented to penetrate into the conductive substrate which results in higher power transfer efficiency compare to the conventional DAT structure which is basically two coupled planar inductors.

Two thick metal layers (M_9 as ultra thick and M_8 as thick) are available for fabricating transmission lines and on-chip inductors in TSMC 1P9M CMOS technology. The thickness and width of the metal layers are the parameters which determine the quality factor of the inductors while the gap between two layers determines the coupling factor between two metal layers. The ultra-thick metal layer (M_9) with thickness of 3.4 µm is preferred to maximize the quality factor of the windings. The minimum distance (2 µm) between two metal lines on the same layer and the dielectric gap between two different metal layers (0.85 µm between M_8 and M_9) are the process restrictions which limit the performance of mmW transformers. Primary and secondary metal widths, (8 µm and 6 µm respectively), and the gap between two windings are adjusted to avoid the additional lossy tuning capacitors. By eliminating the tuning capacitors, the proposed transformers are guaranteed to have a higher efficiency compared to the typical stacked transformer-based network. Another major

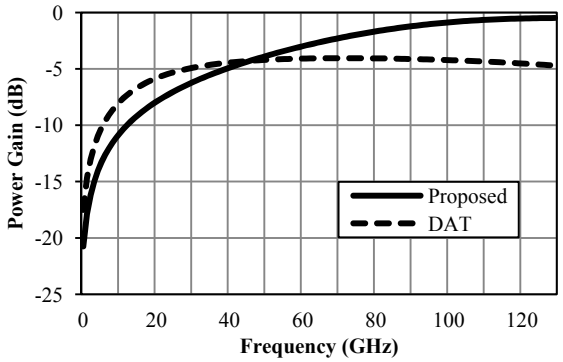


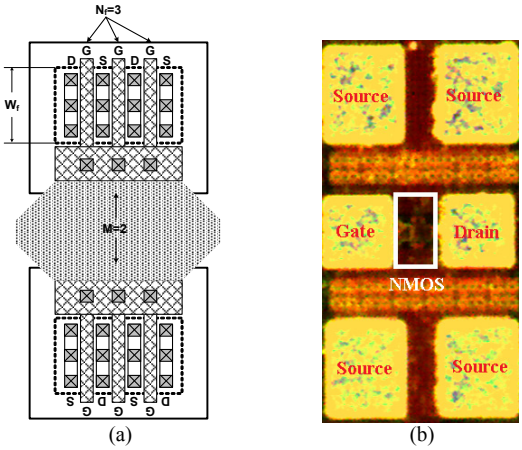
Fig. 3. Insertion loss of the proposed topology vs. conventional DAT

advantage of the proposed transformer is the adjustable gap between to windings which can provide different coupling factors. Moreover, the proposed topology has the advantage of being very compact.

3D EM simulations are performed to extract the S-parameters and evaluate the proposed topology. Fig. 2.a illustrates the proposed topology. A conventional DAT structure like Fig. 2.b is designed and simulated to be compared in terms of efficiency and loss. In comparison with the same size conventional DAT topology, higher power gain and lower insertion loss is achieved for the proposed power combiner at frequencies higher than 60 GHz as illustrated in Fig. 3. The other advantage of the proposed topology is the capability of using a same topology as input power splitter which is a solution to avoid the use of lossy Wilkinson power splitters and matching components.

B. Power stage transistors

In addition to lossy passive power combiners, a major challenge in the design of a fully integrated mmW PA is dealing with the low power gain of the large transistors which are used at such high frequencies [1]. The most important parameters that characterize the frequency dependant gain performances of a MOSFET are the cut-off frequency (f_T) and the maximum frequency of operation (f_{max}) [1]. In addition to this, a high level of output current is required for power amplifier application which poses the challenge of using transistors with large channel width. For mmW MOSFETs, the f_{max} is primarily limited by the series gate resistance and the losses in the drain and source connections [1][3]. To provide a high level of output power, a transistor with a large channel width is required. To achieve the wider channel width and higher current, the multi-finger parallel configuration must be used as shown in Fig. 4.a. Using multiple fingers is a common way in order to build high power MOSFETs. However, this has the negative effect that increasing the total number of fingers with a fixed finger width leads to a large layout. In this case, although the poly-silicon gate resistance per finger remains fixed, large inter-connections are needed to connect the gates and drains of multiple fingers, which cause additional resistive losses and leads to a lower f_{max} and gain. In addition, the I/O impedances drop when the number of fingers



(a) (b)

Fig. 4. Power MOSFETS. a) Multi-finger paralleled NMOS layout b) Micrograph of the fabricated NMOS.

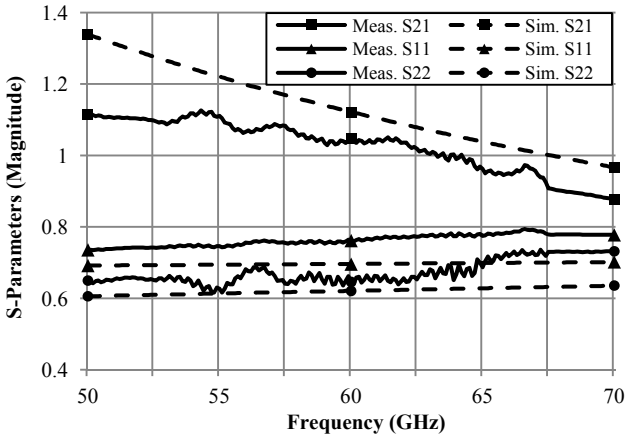


Fig. 5. Simulated and measured S- parameter of the power MOSFET.

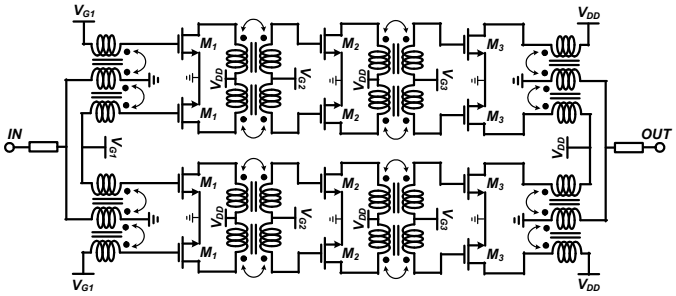


Fig. 6. Schematic of the 60 GHz power amplifier.

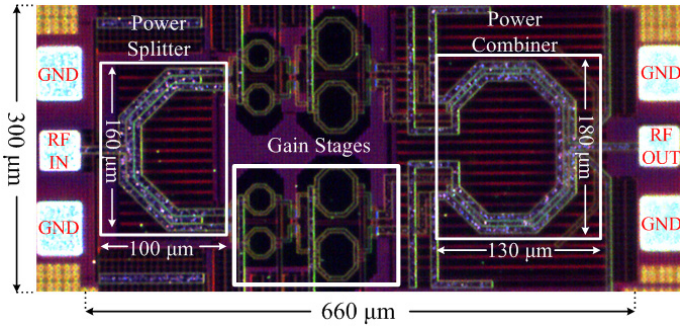


Fig. 7. Chip micrograph of the 60 GHz PA.

is increased which leads to higher matching network losses because the higher transformation ratio is needed. A power MOSFET with 120 um channel width is designed and fabricated in 65 nm CMOS technology shown in Fig. 4.b. The output current of 63 mA is measured using a 1.4V supply and the gate voltage of 0.8 V. Simulation and measured results of the fabricated MOSFET are illustrated in Fig. 5. According to Fig. 5, using a total gate width of 120 µm keeps the f_{max} above 60 GHz.

C. *Gain stages and Inter-stage matching*

The schematic of the 60 GHz CMOS power amplifier is presented in Fig. 6. The transistors were laid out in two parallel 32 fingers with 1.8µm wide fingers for the last stage and with 32 fingers, 1.2 µm and 1.6 µm for driver and gain stages respectively. To ensure a reasonable voltage gain, the driver stage and the gain stage were cascaded before the main power stage. Bias conditions were set to achieve the maximum current density at frequencies near f_T. The gate bias (V_{GG}) voltage is set to be 0.8V while the supply voltage (V_{DD}) is 1.4 V for all the stages.

To ensure a reasonable voltage gain, the driver stage and the gain stage were cascaded before the main power stage. For inter-stage matching circuits, stacked transformers were modeled in Advanced Design System (ADS) and fabricated on the M_9 and M_8 metal layers with radii of 15 µm and 20 µm and conductor width of 6 µm. Utilizing the M_8 and M_9 metal layers, a coupling factor of 0.75 and maximum quality factor of 15 is achieved based on EM simulations. Simulated gain and I/O reflections of the 60 GHz PA are illustrated in Fig. 8.

III. Measured Results

The 60 GHz PA is fabricated in TSMC 1P9M 65nm CMOS process. The chip micrograph of the PA is shown in Fig. 7. The PA only occupies a core area of 0.19 mm^2 by utilizing a compact power combiner and splitter. The S-parameter measurements are performed using Agilent N5251A vector network analyzer (VNA) solution which uses an E8361 power network analyzer (PNA), millimeter wave test controller and broadband frequency extenders. The measured S-parameters are compared with the simulation results in Fig. 8. Applying 1.4V supply, a power gain of 18.8 dB and a 3dB bandwidth of 4 GHz (58 to 62 GHz) are measured. With the stability factor of greater than unity, the amplifier is unconditionally stable over the frequency range of operation.

The 60 GHz power measurements have been performed using Rohde-Schwarz NRP-Z power sensors and the R&S ZVA67 VNA. The measured results are shown in Fig. 9. With 1.4V supply voltage, the measured 1dB compressed output power (P_{1dB}) is 16.9 dBm and the saturated output power (P_{sat}) is 18.3 dBm. The measured peak PAE is 15.9%. Compared to the reported 60 GHz PAs, the narrow-band PA is smaller in size for comparable higher output power while improving the linearity based on the 16.9 dBm measured 1dB compression point. Table. I summarizes a comparison with the state-of-the-art 60 GHz PAs in 65nm CMOS technology.

TABLE. I
COMPARISON WITH PUBLISHED 60 GHZ PAS IN 65NM CMOS.

	B.W. [GHz]	Stages	Architecture	P_{sat} [dBm]	P_{1dB} [dBm]	G_{max} [dB]	PAE_{max} [%]	P_{DC} [mW]	Size [mm^2]	Power/Area [mW/mm^2]	Ref.
60 GHz PAs in 65nm CMOS Technology	57-65	2	Single-ended/C.S	13	8.9	8	11	64.8	0.29	45	[2]
	58-65	3	Differential/C.S	11.5	2.5	15.8	11	43.5	0.05	230	[3]
	55-65	2	Differential/C.S/4x	17.9	15.4	18.6	11.7	460	0.83	22	[4]
	53-68	2	Single/Cascode/8x	18.1	11.5	15.5	3.6	1504	0.46	140	[5]
	55-65	1	Single-ended/C.S	9	6	4.5	9	27.6	0.27	29	[6]
	-	4	Single-ended/C.S	13.8	12.2	13.4	7.6	300	1.28	19	[7]
	59-67	2	Single-ended/C.S	10.6	9.2	13.2	8.9	80	0.29	40	[8]
	56-62	3	Differential/C.S	14.6	10	23.2	16.3	135	0.60	48	[9]
	58-64	3	Single-ended/C.S/2x	17.8	13.8	11	12.6	-	0.28	214	[10]
	58-62	3	Single-ended/C.S/4x	18.3	16.9	18.8	15.9	424	0.19	360	This work

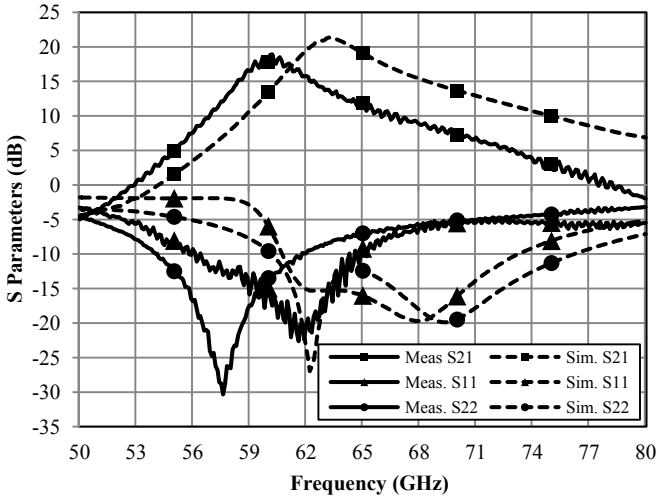


Fig. 8. Measured and simulated S-parameters

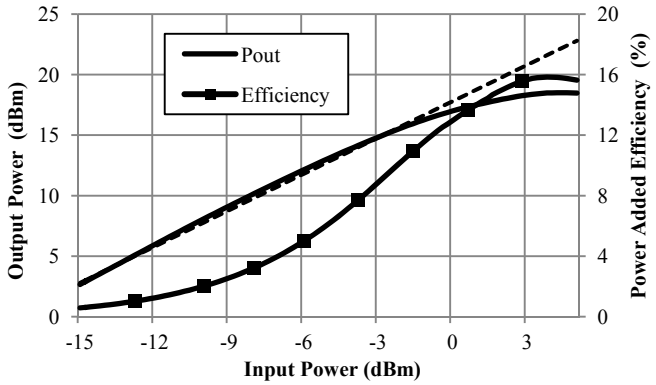


Fig. 9. Measured output power and efficiency

IV. CONCLUSION

A novel multi-conductor power combiner for an integrated 60 GHz CMOS PA has been proposed. The proposed topology provides a compact 4-way power combining capability to combine the output power of four individual PA cores. The PA core consists of cascaded common source stages with inter-stage matching. The peak power gain of 18.8 dB and 18.3dBm saturated output power are measured over the 3dB bandwidth of 4 GHz. The 0.19 mm^2 die area consumes 424 mA from a 1.4V supply and presents 15.9% PAE at saturation.

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