Fully-Integrated Passive Threshold-Compensated PMOS Rectifier for RF Energy Harvesting

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***Abstract*— This paper presents an RF-DC rectifier for radio frequency energy harvesting applications. The proposed passive multi-stage RF-DC rectifier uses standard PMOS transistors to allow individual bulk biasing without the requirement of deep nwell technology. The RF-DC conversion circuit is based on passive threshold self-compensated topology. A design strategy to enhance the input voltage range and to optimize the power conversion efficiency is presented. Designed and simulated in IBM 130-nm CMOS technology, the proposed 915-MHz rectifier shows improved output voltage and power conversion efficiency compared to recent works. When driving a 1-MΩ load, the RF-DC power conversion unit is able to supply 1-V output with an input power of -22 dBm (6.3 μW) and obtains an efficiency of 11.4% at -16.1 dBm (24.5 μW) while supplying 2-V to the output.**

I. Introduction

There is a growing interest to use energy harvesting to partially/fully supply the energy required for the operation of portable electronic devices. The required power can be obtained by extracting energy from sunlight, mechanical vibrations, radio waves or other harvestable energy sources. Scavenging ambient energy from the available radio waves commonly referred as RF energy harvesting is one of the most popular power extraction method [1].

An RF-DC rectifier is an important building block for RF energy harvesting. A highly efficient rectifier is required which produces high output voltages at low input power level. The performance of RF-DC rectifiers is significantly affected by the threshold voltage requirement of the rectifying device which reduces the efficiency and prevents operation at lower power level. Schottky diode can operate at much lower threshold voltage compared with a standard MOS transistor but has the disadvantage of requiring additional fabrication steps at added cost in manufacturing [2]. External voltage compensators can be used to reduce the threshold voltage. This technique, commonly referred as active energy harvesting requires a secondary battery [3] and is generally used in active sensors or active RFID. In some CMOS processes, low V_{TH} transistors are available that can be used for construction of passive (battery-less) energy harvesting circuits [4], though not attaining comparative performance in terms of compensating voltage.

As an alternative to using semiconductor technologies offering low V_{TH} devices, circuit level techniques comprising passive threshold reduction schemes have been used. An internal V_{TH} cancellation circuit is used in [5], where a capacitor stores the threshold voltage that is applied at the gate-source terminal of the MOS transistor. This technique uses high capacitance and resistance value which leads to higher silicon area on the chip. Instead of generating a passive threshold voltage through additional circuitry, work in [6] utilizes floating gate transistors as rectifying diode. The floating gate transistors are able to store pre-charged voltage, thus effectively lowering the threshold voltage. Still, this technique requires an additional pre-charge phase making it unsuitable for fully battery-less applications. The RF-DC power conversion circuit consisting of NMOS transistors with bulk grounded leads to an increase in the threshold voltage of the transistor with the number of stages due to the body effect. This degrades the efficiency of the power conversion circuit. The bulk of the transistors can be dynamically controlled using additional circuit [7]. This may again generate substrate current reducing the efficiency. Authors in [8] introduced a self-compensation scheme based on Dickson topology [9]. NMOS transistors with deep nwell were used to provide individual bulk biasing and to reduce the variation of threshold voltage between different rectifier stages. The compensating voltage was provided by connecting the gate terminal to later stages. The parasitic capacitance at each node is increased in deep nwell source-bulk connected devices.

The proposed scheme is based on multi-stage Dickson topology. It consists of multiple PMOS transistors in cascade instead of deep nwell NMOS tranistors. The compensating voltage is provided by the connection of gate terminal to previous stages, also referred as back-compensated topology. The RF-DC power conversion circuit in this paper is designed and simulated in IBM-130 nm CMOS technology. The RF-DC power conversion circuit is further compared to a recent work [8].

II. Rectifier Design

A PMOS voltage doubler structure is used as the rectifier unit in the RF-DC power conversion circuit. The voltage doubler structure rectifies the ac input in both positive and negative cycles.

The diodes are implemented by connecting the drain and the gate terminal of the MOS transistor together such that

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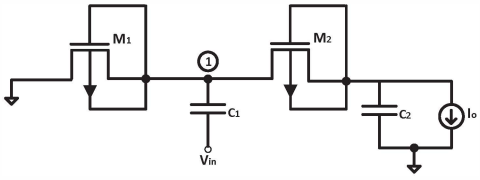

Fig. 1. Conventional PMOS voltage doubler.

the transistor is always in saturation region in forward bias condition. In reverse bias, the reverse current flow is limited to the reverse leakage current of transistors. During the negative cycle, the potential at node1 remains constant to $-|V_{TP1}|$ and the capacitor C_1 charges to $V_{amp} - |V_{TP1}|$ where V_{amp} is the maximum amplitude of the ac signal and $|V_{TP1}|$ is the threshold voltage of PMOS transistor M_1. During the positive cycle, diode connected transistor M_1 is reverse biased and the current flows through M_2 and charges the capacitor C_2. The voltage at the output is $2V_{amp} - |V_{TP1}| - |V_{TP2}|$. Thus the maximum possible voltage is twice the RF signal's amplitude only when the threshold voltage of the diodes is equal to zero. Ideally this is possible but can lead to problems such as reverse current leading to ripple generation and leakage. Hence an optimum threshold value should be chosen.

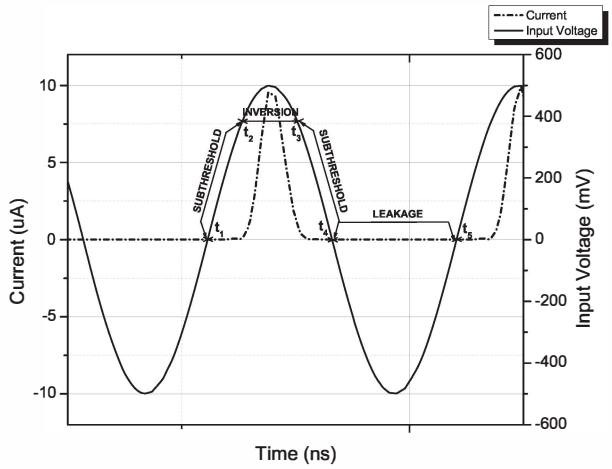

Fig. 2. Transient analysis of output current and input voltage of PMOS voltage doubler

Fig. (2) shows the simulation for a one stage PMOS voltage doubler. The actual charge transfer mechanism is only for a short duration while other parameters such as leakage, subthreshold has to be considered for the rest of the cycle. There are three regions of operation for PMOS transistors for which the operation of the circuit is described as follows:

A. *Subthreshold* $[t_1, t_2]$ *and* $[t_3, t_4]$

It extends from $V_{in} = 0$ to $V_{in} = |V_{TP}|$, where V_{in} is the input voltage. The threshold voltage is not constant and varies due to the source-bulk bias effect as the input voltage is a variant. The current in this region is given by [2]

$$I_{d,sub} = I_{SO}.\frac{W}{L}.e^{|V_{gs}|/\eta V_T}.(1 - e^{-|V_{ds}|/\eta V_T}).(1 + \lambda_{sub}|V_{ds}|) \quad (1)$$

where $I_{d,sub}$ is subthreshold drain current, I_{SO} is reverse saturation current, V_{gs} is gate-source bias, V_{ds} is drain-source bias, V_T is thermal voltage, λ_{sub} is subthreshold region channel length modulation and η is subthreshold region swing parameter.

As seen from the Spectre simulation, in the sub-threshold region, the current is minimal while the input voltage is close to zero and increases with V_{in}.

B. *Inversion* $[t_2, t_3]$

It extends from $V_{in} = |V_{TP}|$ to $V_{in} = V_{amp}$. In the inversion region, the output current continues to increase and reaches its peak when $V_{in} = V_{amp}$. The charge transfer is maximum at this point.

$$I_d = \frac{1}{2}\mu_p C_{ox}.\frac{W}{L}.(|V_{gs}| - |V_{TP}|)^2 \quad (2)$$

where I_d is drain current, μ_p is PMOS mobility and C_{ox} is oxide capacitance.

As seen from the simulation, this point is the peak of the output current which is 9.5 μA at V_{amp} = 500-mV. Comparing this with the subthreshold current which is at maximum in hundreds of nanoamperes.

C. *Leakage* $[t_4, t_5]$

It extends from $V_{in} = 0$ to the next $V_{in} = 0$ in the negative half cycle. The current that flows through transistor M_2 during the time interval is referred as reverse leakage current. Ideally, it should be zero. In this region, the source and the drain terminals are interchanged resulting in $V_{gs} = 0$.

$$I_{d,leakage} = I_{SO}.\frac{W}{L}.(1 - e^{-|V_{ds}|/\eta V_T}).(1 + \lambda_{sub}|V_{ds}|) \quad (3)$$

Comparing Equation (1) and (3), the leakage current $I_{d,leakage}$ will be smaller than the sub-threshold one but has a non-zero value. The leakage current has a dependence on reverse saturation current which depends on the mobility, channel doping and is relatively lesser for PMOS devices. Another consideration is W/L (aspect ratio) and for higher aspect ratio, greater leakage is expected.

As seen from the simulation, the leakage current during the negative half cycle is in few nanoamperes. For instance, the maximum leakage current is around 65 nA for the result in Fig. (2). As the output current and the load current for multi-stage rectifier operating under low power condition is generally less compared with a single stage, the leakage current cannot be neglected.

For a standard PMOS rectifier in our CMOS process, the onset of more than 100 nA of current is at an input voltage of approximately 380-mV. Thus, there has to be a minimum input voltage before a significant amount of current appears at the output. The multi-stage rectifier design is implemented

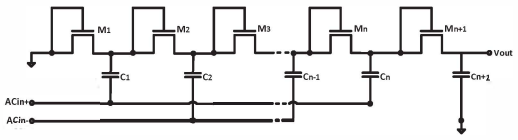

Fig. 3. Conventional Dickson charge multiplier

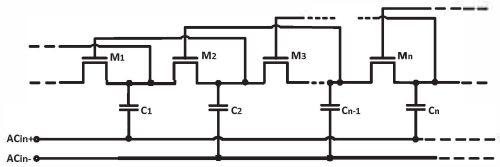

Fig. 4. Forward-compensated charge multiplier topology for NMOS

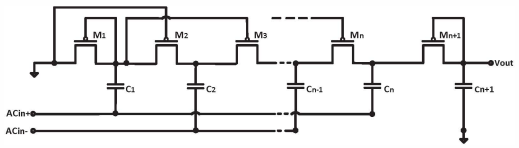

Fig. 5. Proposed back-compensated charge multiplier topology for PMOS

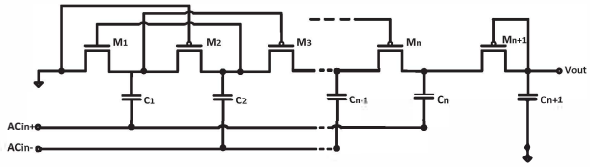

Fig. 6. Proposed back-compensated charge multiplier topology with NMOS-PMOS

while considering the different regions of operation in the rectifier. The next section discusses about the proposed scheme in multi-stage rectifier.

III. Proposed Design

The voltage doubler structure can be implemented as a cascade of two halfwave rectifiers to increase the output voltage. The standard Dickson multiplier can be modified for designs involving energy harvesters where the input voltage is low. Fig. (3) shows an *n*-stage conventional Dickson multiplier. Patent [10] describes a threshold self-compensation technique. The gate of the transistor in this technique is connected to the adjacent source of the transistor instead of the traditional diode connected structure. Thus, providing bias voltage equivalent to the incremental voltage across each stage. Based on this technique, a forward compensated topology was implemented by [8] where the bias voltage was increased by extending the gate length connection.

Fig. (4) shows the basic forward compensated topology. Fig. (5) shows the proposed back-compensated Dickson charge multiplier. This scheme is applicable for PMOS transistors. A negative gate-source bias is generated due to the backward connection as shown in Fig. (5). The last stage of the multiplier is left uncompensated to reduce the leakage. The proposed *n*-level back-compensated Dickson charge multiplier requires *'n'* initial NMOS transistors to compensate for the threshold voltage of each of them. Fig. (6) shows the proposed *n*-level back-compensated Dickson charge multiplier. The first stage is replaced by NMOS transistor and a forward gate connection is used. The length of the gate connection can be increased to further reduce the threshold voltage. In the proposed scheme, the terminal *ACin-* is grounded while the source is connected to *ACin+*.

The proposed scheme can be summarized as follows
A voltage multiplier circuit is designed consisting of multiple PMOS transistors in cascade. Patent in [10] discussed the need for higher potential at the gate terminal to offset the threshold voltage. A PMOS transistor requires negative gate-source potential which is achieved by connecting the gate potential to the previous node rather than later node. The proposed scheme reduces the threshold voltage leading to increased output voltage. The scheme shown in Fig. (5) and Fig. (6) is level-1 compensation. The compensation can be increased by increasing the level i.e. instead of connecting the gate terminal of PMOS to the immediate previous neighbor, increasing the length of the gate connection. For an *n*-level compensation, for the proposed scheme, there will be *'n'* initial PMOS transistors that will be uncompensated. These *'n'* transistors are compensated by using NMOS transistors.

IV. Discussion and Results

The design of the rectifier using proposed scheme involves selecting key parameters such as number of stages, width of the transistor, level of compensation and capacitance. For the proposed scheme, a level-3 compensated, 12 stage rectifier with pumping capacitance (C = 2 pF) and (W = 8-μm) was found to be the best choice through extensive simulations. The strategy while designing the multi-stage rectifier is as follows: The individual stages of the voltage doubler can be cascaded to increase the output voltage. As the number of stages increases, the output voltage increases. With the increase in the number of stages, the efficiency decreases and the output voltage saturates. Hence the transistors as well as the pumping capacitors are scaled while increasing the stages. The scaling is done to maintain the incremental voltage per stage and the efficiency relatively constant with the increase in the number of stages.

Fig. (7) shows the output dc voltage as the function of input power. The simulated circuit is able to provide an output voltage of 1-V for an input power as low as -22 dBm for a load of 1-MΩ. The power conversion efficiency curve is plotted in Fig. (8) where a maximum efficiency of 11.4% is obtained while delivering 2-V to a load of 1-MΩ at an input power level of -16.1 dBm. When driving a 5-MΩ load, the circuit can deliver 2.2-V at an input power level of -13.5 dBm with an efficiency of 2%. The results are compared to a recent work [8] which is based on NMOS forward compensated topology. The efficiency comparison as a function of received power in Fig. (8) is done while de-embedding the input reflections in [8].

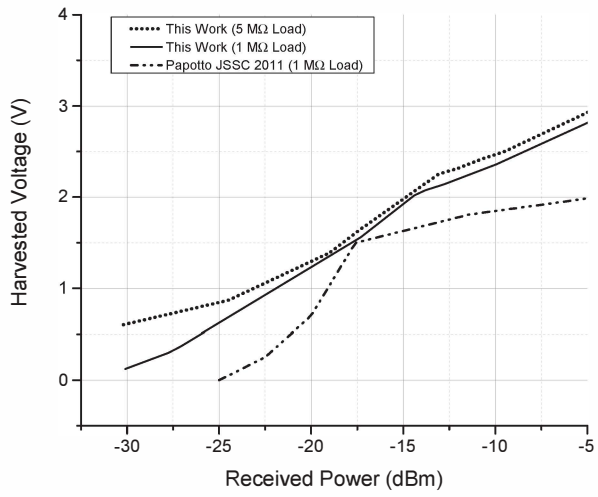

Fig. 7. Harvested voltage as a function of received power

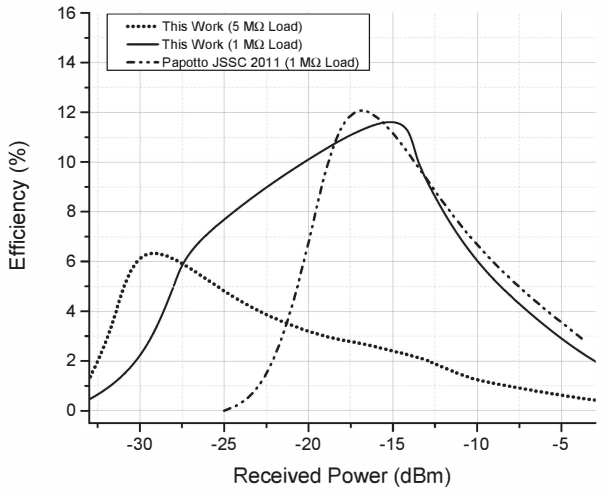

Fig. 8. Efficiency as a function of received power

V. Conclusion

A passive threshold-compensated multi-stage PMOS RF-DC power conversion circuit operating at 915 MHz is presented. The proposed power conversion circuit employs PMOS transistors and *'n'* number of NMOS transistors for a *n*-level compensated multi-stage rectifier eliminating the need for deep nwell technology. It also uses a unique back-compensated threshold scheme. The simulation result confirms an output voltage of 1-V at -22 dBm and achieves an efficiency of 11.4% at -16.1 dBm when driving a 1-MΩ load. The power conversion circuit has a wide array of applications in RF energy harvesting and low power wireless sensor networks.

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