A Compact CMOS UWB LNA Using Tunable Active Inductors for WLAN Interference Rejection

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***Abstract*—A compact 2.0-11.0GHz CMOS ultra-wideband (UWB) low-noise amplifier (LNA) using tunable active inductors for suppressing in-band (over 4.8-6.0GHz) WLAN interference signals is presented. In the proposed LNA, the active inductor in series with a small capacitor forms an active *LC* resonator which rejects or notches the undesired signals at the resonance frequency. Employing multiple resonators in the LNA increases the rejection depth. Moreover, the tunability of the active inductors allows for notching the signals over a wide frequency range. Designed and simulated in a 90nm digital CMOS process, the proposed LNA with such active inductors used in notch filters occupies a core chip-area of only 0.0182mm^2. The LNA exhibits an average power gain of 16.5dB over 2.0-11.0GHz bandwidth while the rejection of unwanted WLAN interference signals is -44.8dB at 5.81GHz. The notch-frequency can be tuned in excess of 4.5-6.6GHz, and the rejection depth can be increased to -87.5dB, the highest rejection among the reported notch-filter UWB LNAs.**

I. Introduction

UWB radio technology uses the bandwidth of 3.1-10.6GHz (7.5GHz), and in multiband (MB) UWB systems the 7.5GHz UWB spectrum is divided into fourteen sub-bands of 528MHz each as shown in Fig. 1 [1]. Then, these bands are grouped into five band-groups, and MB-UWB systems can operate in any one or more than one of these band groups. However, the in-band WLAN signals over 4.9-5.9GHz (Figure 1) develop a strong interference (+30dB higher) with weak UWB signals. The interference products may saturate the high gain RF front end and desensitize the whole UWB receiver. Hence, a robust interference-rejection technique is required in the LNA, the first stage of the receiver, to reject or suppress WLAN signals before being amplified.

UWB LNAs suppressing WLAN interference signals using notch filters have been reported in [2-4]. These notch filters are realized as passive *LC* resonators with low notch depth, and have a limited tuning range. On-chip passive inductors are bulky and occupy a large chip area. Moreover, they are non-tunable, non-scalable with technology scaling, and incompatible with most standard digital CMOS processes. To reduce size and cost of chips, passive inductors need to be replaced with transistor-only active circuits, namely, active

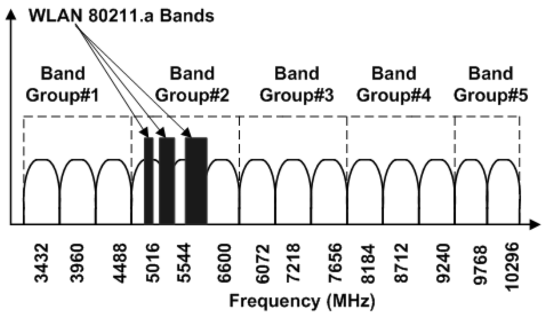

Figure 1: Bands and band-groups of MB-UWB systems

inductors that can be implemented in inexpensive digital CMOS processes.

In this paper, we present a three-stage UWB LNA using series active *LC*-resonators in the input and output stages where active inductors replace passive inductors (*L*). An active inductor (AI) consists of only a few transistors. Therefore, it occupies a fraction of the area of a passive inductor and is well compatible to be implemented in standard digital CMOS processes. Moreover, the bias dependent operation of active inductors allows for tuning them widely [5]. The proposed LNA is designed and simulated in STMicroelectronics 90nm digital CMOS process.

This paper is organized as follows. Section II presents the proposed UWB LNA and its design technique. Design realization, and simulation results are presented in Section III followed by a brief conclusion in Section IV.

II. Design of UWB Notch-Filter LNA

The circuit of the proposed three-stage UWB LNA is shown in Figure 2. Two *LC* networks are connected at the outputs of the first-stage cascode amplifier (consisting of transistors M1, M2 and M3) and the final-stage common-source amplifier (consisting of M6 and R_L). The AI replaces each of the passive inductor *L*, and it can be tuned with a varying inductance and operating bandwidth. A small capacitor *C* (50fF) is used in series with the AI to form the series active *LC* (or AI-*C*) resonator or filter. When the inductance of the AI resonates with *C* at the undesired

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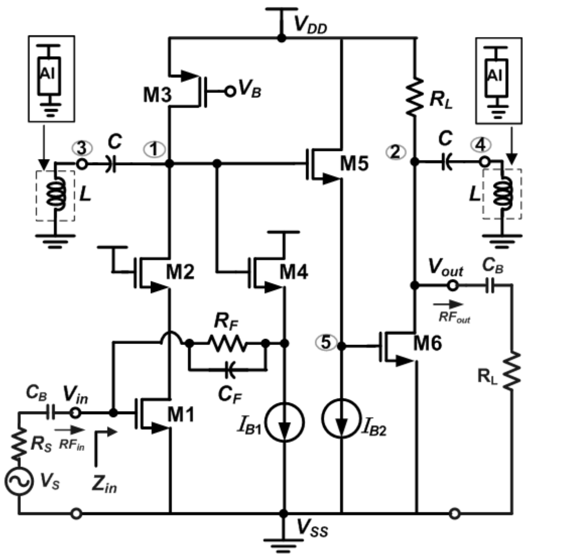

Figure 2: Proposed UWB LNA using active *LC* notch-filters

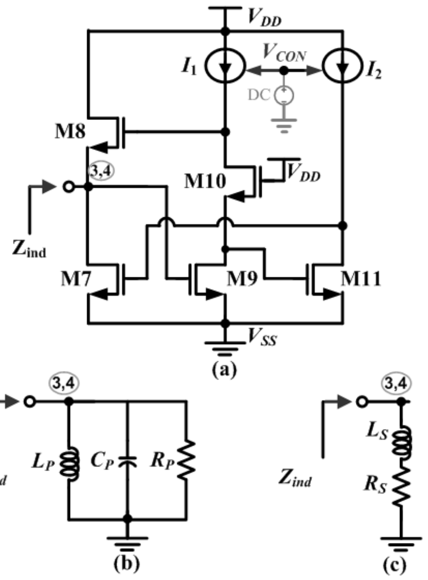

Figure 3: Active inductor and its equivalent *RLC* model.

frequency, the series AI-C resonator exhibits a very low resistance, which shorts the unwanted signals to the ground. Thus, the unwanted signals are filtered out, and are not processed in the system. Two identical AI-C filters being resonant at the same frequency increase the undesired signal attenuation; that further increases the rejection. The circuit of AI is shown in Figure 3(a) [6]. An external control voltage, V_{con} tunes both of the AIs, and changes their inductances that results in different resonance frequencies with a fixed capacitance C in each filter.

The proposed UWB LNA is the modification of the multi-stage UWB LNA using tunable active inductors [7]. The input cascode and the output common-source amplifiers of the LNA are separated by an inter-stage buffer amplifier (consisting of M5 and current-source I_{B2}) making the input and output matching independent. The input 50Ω wideband-matching is achieved using a local feedback network through a source-follower (consisting of M4 and current-source I_{B1}) and a feedback resistor R_F. A small capacitor C_F (25fF) eliminates peaking in the amplifier frequency response.

A. Active Inductor

One port of the inductor (L) in the series LC resonator (Figure1) is grounded, and hence, a one-port grounded AI is required for the proposed LNA. CMOS transistor-only one-port grounded active inductors were reported in the literature [6-9]. The input impedance of these active inductors is inductive over a certain frequency range. The inductive input impedance is modeled by a parallel RLC circuit yielding a second-order transfer function. Besides inductance (L_P), two important performance parameters of this RLC circuit are resonance frequency (ω_P) and quality factor (Q). A high ω_P increases the operating range of the inductive impedance, and a high Q means low loss yielding a small resistance in the equivalent series circuit (see below) of the AI.

Here, in the proposed LNA, as it was mentioned above, we employ the AI of Figure 3a, reported in [6].

Using simple transistor models (transconductance and input capacitance), at mid frequencies, the input inductive admittance, Y_{ind} (=1/Z_{ind}) looking at node 3 (or 4) in Figure 3 (a) may be obtained as (Figure 3(b))

$$Y_{ind} \approx C_P s + G_P + 1(L_P)s \quad (1)$$

where $C_P = C_{gs9}$, $G_P = 1/R_P = g_{m9}\left(1 + \frac{g_{m7}}{g_{m10}} \frac{V_{DS11}}{V_{GS11} - V_{TN}}\right)$

and

$L_P = C_{gs8}/(g_{m8}g_{m9})$. Here, C_{gs} and g_m with subscripts (7,8, 9) are gate-source capacitances and tranconductances of corresponding transistors (M7, M8 and M9). The stage M11, I_2 where transistor M11 operates in triode regime is used as an amplifier with a small negative gain of $A_v = -V_{DS11}/(V_{GS11} - V_{TN})$ defined by the DC voltages at the drain and gate of M11.

In our application, the admittance Y_{ind} is used at the frequencies below the resonant frequency of $\omega_p = 1/\sqrt{L_p C_p}$, and the Q-factor of this parallel tank is sufficiently high. Then the circuit of Fig. 3(b) can be substituted by a series circuit of Figure 3(c) including $L_S \approx C_{gs8}/(g_{m8}g_{m9})$ and $R_s \approx 0$. These L_S and R_S represent the inductance and series resistance of the active inductor respectively, and, eventually, L_S in series with R_S replaces the active inductor at node 3 (or 4) of Figure 1. Note that L_S is a bias-dependent parameter. Tuning the currents I_1 and I_2 by a common control-voltage, V_{con} changes the transconductances (g_{m8} and g_{m9}) of transistors, and in turn, changes the inductance L_S.

B. Tunable Active Notch-Filter

The AI, represented by the inductance L_S (with a small resistance R_S) is connected in series with a small capacitance

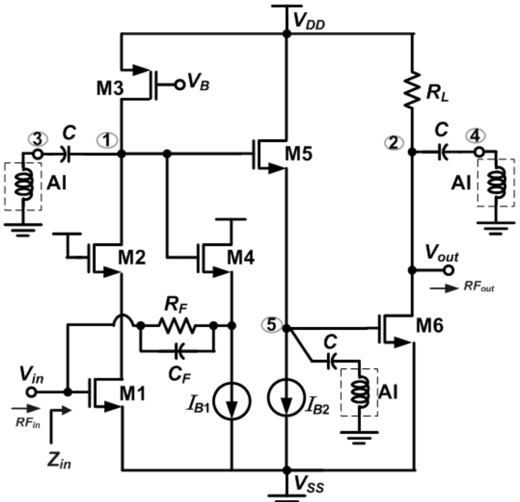

Figure 4: UWB LNA for increased attenuation

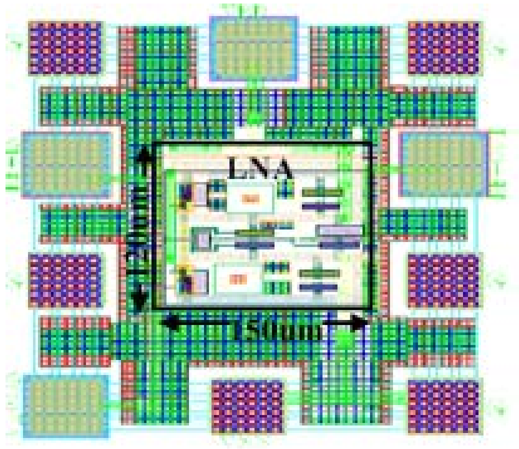

Figure 5: Layout of the proposed LNA

C, and forms the series AI-C filter. A series LC filter provides the minimum resistance at resonance frequency. The output signals of the amplifier will be filtered out at the resonance (notch) frequency, ω_n , which is calculated as

$$\omega_n = \frac{1}{\sqrt{L_S C}} \, . \qquad (2)$$

Changing the inductance of the AI, the resonance frequency ω_n is tuned at different frequencies resulting in the tunable notch filter. The Q-factor of the tuned $L_S C$ resonator is defined as

$$Q_n = \frac{\omega_n L_S}{R_S} = \frac{1}{R_S}\sqrt{\frac{L_S}{C}} \, , \qquad (3)$$

and for a very small resistance R_S, Q_n becomes very high. Thus, a high selectivity, and in turn, a very sharp frequency-response (roll-off or roll-on) is obtained around the notch frequency, $f_n=\omega/(2\pi)$. The higher is the Q, the higher is the loss of the signal amplitude due to low R_S. For two identical AI-C notch filters (Figure 2) resonating at the same frequency, the loss or attenuation of unwanted signals is increased. For further attenuation of the undesired WLAN signals in increasing the rejection or notching depth, the proposed LNA can be modified as shown in Figure 4 with an additional notch filter inserted at node 5.

The active inductors consisting of transistors generate more noise than passive inductors. The overall noise figure of the proposed LNA is mainly determined by noises contributed by the transistors and resistors of the first-stage cascode amplifier, the feedback network (R_F, M4, I_{B1}), and the active-inductor at the output of the cascode amplifier [7]. Since, the AI is connected at the output, the high gain of the cascode amplifier, and the feedback at the input of the LNA through the buffer (M4, I_{B1}) reduces the noise contribution of the AI significantly [7]. The AIs at the output nodes 2 and 5 are far apart from the input of the LNA. Therefore, these two AIs do not contribute a significant amount of noise to the overall noise-figure of the LNA.

III. DESIGN REALIZATION AND SIMULATION

The proposed UWB notch-filter LNA (Figure1) is designed and simulated in STMicroelectronics 90nm digital CMOS process.

A. Design Realization

Transistors M1 (W=135µm), M2 (W=45µm) and M4 (W=18µm), I_{B1} (≈1mA) and resistor R_F (200Ω) are sized (width, W, is the transistor width) to achieve 50Ω wideband matching. The gain of the cascode stage is traded with the overall input matching of the LNA. Approximately 4mA current is spent in the first-stage cascode amplifier with M3 of W=39µm. The inter-stage buffer consisting of transistor M5 (W=60µm) and I_{B2} (≈2.2mA) are chosen to keep its gain close to unity and the bandwidth unaffected. The common-source amplifier boost the overall gain of the LNA with a large M6 (W=90µm) and R_L of 75Ω while spending a current of 6mA approximately. The transistors in the active inductors are chosen with the widths of 1.5µm to 7.5µm [6]. All the transistors in the core LNA and AIs have the length (L) of 100nm. The capacitor C in the notch filter is 50fF only. The layout of the proposed LNA is shown in Fig.5 and the core LNA (excluding bonding pads) occupies an area of 0.0182mm^2 (140µm x 130µm).

B. Simulation Results

The simulations (extracted) were performed in a 50-ohm system (R_G = R_L =50Ω) and the proposed LNA consumes 16.5mW from a 1.2V power supply. Figure 6 shows the simulated results of the LNA of Fig. 2 for V_{con} of 540mV (for the AIs). The LNA shows an average power gain (S21) of 16.5dB, noise-figure (NF) of 2.2-3.4dB and input return loss (S11) of less than -12.0dB over 2.0-11.0GHz with a -44.8dB rejection at 5.81GHz. Tuning the AIs of the LNA (as in Figure 2) results in notches at different frequencies (4.49GHz, 4.9GHz, 5.81GHz, and 6.6GHz) as shown in Figure 7. Figure 8 shows the tuning of the LNA of Figure 4 that uses three AI-C filters for the same tuning frequencies. Note that for the LNA of Figure 4, the notch or rejection of signals goes down to -87.5dB at the same notching frequency of 5.81GHz. Figure 9 shows the NF of the LNA with and without AI-C

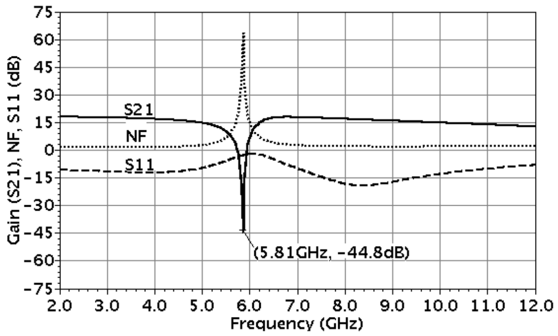

Figure 6: Gain (S21), NF and Insertion loss (S11)

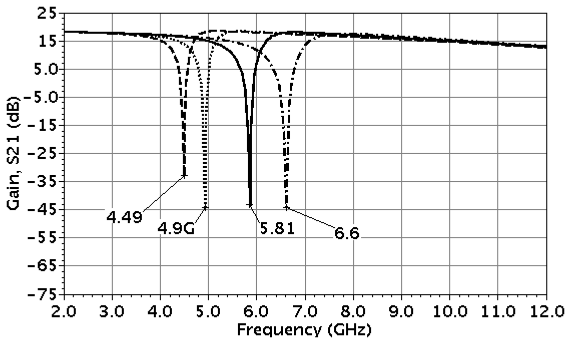

Figure 7: Tuning of notch frequency of the LNA of Figure 2

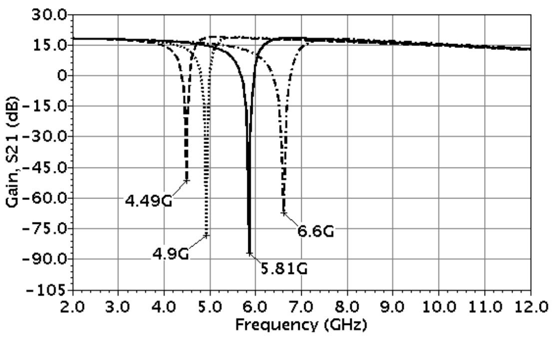

Figure 8: Tuning of notch frequency of the LNA of Fig. 4

filters. The dashed line (WO-AI), solid line (W-2AI) and dotted line (W-3AI) represents the NF of the proposed LNA with no notch-filter, with two notch-filters and with three notch-filters respectively. Note that NF does not degrade significantly with AI-*C* filters over the desired bandwidth.

IV. Conclusion

A very low-chip area ($0.018mm^2$) notch-filter LNA exhibiting the highest rejection (-87.5dB) of WLAN signals and the widest tuning range of notch frequencies (in excess of 4.4-6.66GHz) is presented. Increasing the series resistance (R_S) with inductance (L_S) can widen the notch but it will reduce the notch depth. The design with active inductors

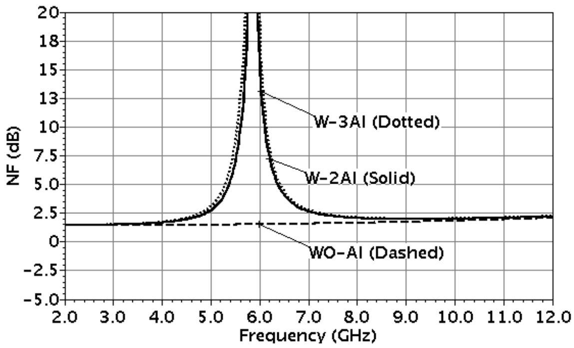

Figure 9: NF of the LNA with and without notch filters

makes the LNA compact and suitable for implementing in digital CMOS processes. The mismatches between active inductors may cause a slight variation of the notch depth. The individual control of the inductors can eliminate this problem. The chip is under fabrication process.

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