# A High Resolution Multibit $\Delta$–$\Sigma$ DAC using Noise Shaping

Swaran R. Singh, Vincent Gaudet, and Kambiz Moez
Department of Electrical and Computer Engineering
University of Alberta, 9107 - 116, Edmonton, Alberta T6G 2V4
Email: {ssingh, vgaudet, kambiz}@ece.ualberta.ca

***Abstract*— Sensor technology for space, planetary, and terrestrial applications has improved at a rate which has outpaced the increase in resolution of conventional data converters. As a result, the electronics subsystem has suddenly become the bottleneck in sensor-based applications. High resolution digital-to-analogue converters in excess of 130dB SNR are required to utilize the resolution provided by modern sensors. This paper presents an architecture for a digital-to-analogue converter (DAC) which can meet this specification across a bandwidth of 0.001–10Hz.**

## I. Introduction

High-resolution sensors must be coupled to equally high-resolution data converters. As sensor technology progresses, front-end readout electronics such as data converters have become the bottleneck in many terrestrial and space-oriented applications. In order to take full advantage of the resolution that the sensors provide, accompanying high-resolution data converters must be developed.

In the applications of interest, the resolution and accuracy of the data converters are required to be in excess of 1 part per million (greater than 21 bits). For example, consider the measurement of a gravitational field by use of a superconducting gravity gradiometer. Figure 1 shows a block diagram detailing the workings of such a device.

The resolution of the gradiometer read-out depends on how close to the centre position the proof mass begins. To achieve a 130dB readout resolution, the voltage on the capacitive plates must be controlled to a tolerance of 1.5$\mu$V at a full-scale voltage of 3.0V. This corresponds to approximately 21 bits of resolution. Due to the low operational frequency of these sensors, the DAC must achieve this resolution at a sensor bandwidth of 0.001–10Hz.

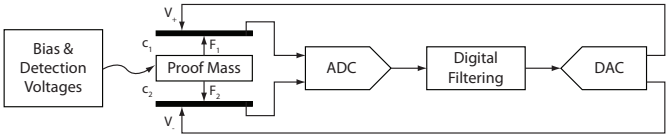


Fig. 1. Gradiometer Loop

While there have been commercial designs which achieve up to 120dB SNR [1], these results have been achieved at A-weighted frequencies, and still fall 10dB short of the goals proposed here. This paper presents an architecture designed to meet the demands of the sensors described above. Key system issues presented are the need for multibit quantization, the ensuing need for a dynamic element matching (DEM) system, and the circuit issues which arise from the high-resolution, near-DC signal band requirements.

## II. Multibit $\Delta\Sigma$ DAC Architecture

Figure 2 shows a block diagram of the multibit, noise-shaped $\Delta\Sigma$ DAC. The 32-b input signal encodes a baseband signal in the range of 0.001–10Hz. This input is delivered as a PCM signal already oversampled to 1.5625KHz. The signal is further oversampled to 1MHz via a three-stage sinc$^k$ interpolation filter with rate multipliers of 80, 80, 100, respectively. A second-order, 5-b $\Delta\Sigma$ modulator ($\Delta\Sigma$M) aggressively shapes the (32 - 5) = 27 bits of quantization noise outside of the signal baseband. The 5-b quantizer output is then fed to the DEM system which generates the selection logic for the unit DAC elements. Finally, the summed DAC output is low-pass filtered to re-create the desired analogue signal.

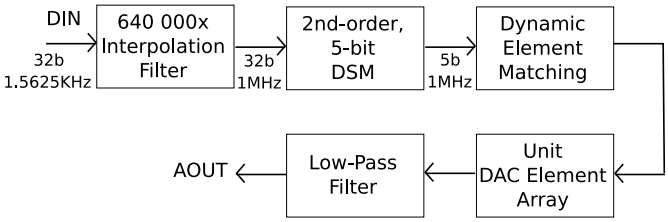


Fig. 2. System Block Diagram

### A. $\Delta\Sigma$ Modulator

Increasing the resolution of a $\Delta\Sigma$ modulator can be achieved by increasing the oversampling ratio (OSR), the order of the modulator, or the width of the quantizer. The method of raising the OSR is bounded by the maximum achievable clock frequency and jitter performance, whereas modulator order is governed by the issues of stability and signal amplitude. Increasing the width of the quantizer is limited by the number of unit DAC elements which can be implemented, and the mismatch between them.

Equation 1 gives the Signal-to-Quantization Noise (SQNR) performance of a second-order $\Delta\Sigma$M with a single-bit quantizer. If the entire system targets a 130dB SNR, each cascaded noise source must contribute less than -130dB of noise. Thus, with a conservative SQNR target of 140dB for the $\Delta\Sigma$M at a maximum signal amplitude (M) of -6dBFS, the second-order

978-1-4244-4480-9/09/$25.00 ©2009 IEEE

modulator must have an OSR of 1835. In contrast, a first-order modulator would require an OSR of over 150 000 to achieve the same noise performance.

$$SQNR_{2nd-order} = \frac{15M^2OSR^5}{2\pi^4}$$
$$(in\ dB) = 10log_{10}\left(\frac{15M^2}{2\pi^4}\right) + 50log_{10}(OSR)$$

Given a baseband signal of 0.001–10Hz, an OSR of 1835 would place the clock rate of the $\Delta\Sigma$M at 36.7KHz. This is a fortunate result on account of the fact that typical (6pF) quartz oscillators have a resonant frequency of 32.768KHz. In the proposed design, however, a clock frequency of 1MHz is used in order to provide adequate clocking to other digital subsystems.

### B. Multibit Quantization

A 1-bit quantizer necessitates a single unit DAC element used to reconstruct the analogue output signal. Due to a binary output, the DAC is inherently linear (as only a perfect line can connect two points). However, a 1-bit quantizer leads to a high truncation error. This error manifests itself as high-frequency components with relatively large amplitudes in the quantized data signal. This spurious content reduces the dynamic range of the converter.

Multibit quantizers offer two advantages to a DAC. First, the overall SNR of the data conversion system improves as the number of bits in the quantizer increases (assuming ideal D/A conversion). Second, the quantization noise power decreases proportionally with the number of quantization levels [2]. This relaxes the requirements on the analogue low-pass reconstruction filter. Increasing the quantizer to 5-b reduces the quantization noise by approximately 30dB. Figure 3 shows the simulation results of a second-order $\Delta\Sigma$ modulator using a 1-b and 5-b quantizer. The 5-b result is shifted down by 30dB, confirming the expected result from theory.

## III. Dynamic Element Matching

There is a barrier to using multibit quantizers, however. When a plurality of unit DAC sources are used, they will suffer from static mismatch due to processing variations. This static mismatch causes the DAC to become non-linear. In the frequency domain, these static errors appear as high-powered spurs in the signal band, thereby crippling the achieved resolution. For example, an 8-level DAC must have greater matching than 10ppm in order to achieve 16 bits of integral linearity. This represents the general limit of matching tolerances on a VLSI process [4].

Mismatch-shaping has become a preferred method of mitigating the effects of unit DAC element non-linearities in multibit data converters [5] – [9]. Mismatch-shaping methods use techniques similar to $\Delta\Sigma$ modulation in order to shape mismatch-induced noise out of the signal band, and in a manner which is uncorrelated to the signal input. Hence, rather than simply trying to improve mismatch from a fabrication or

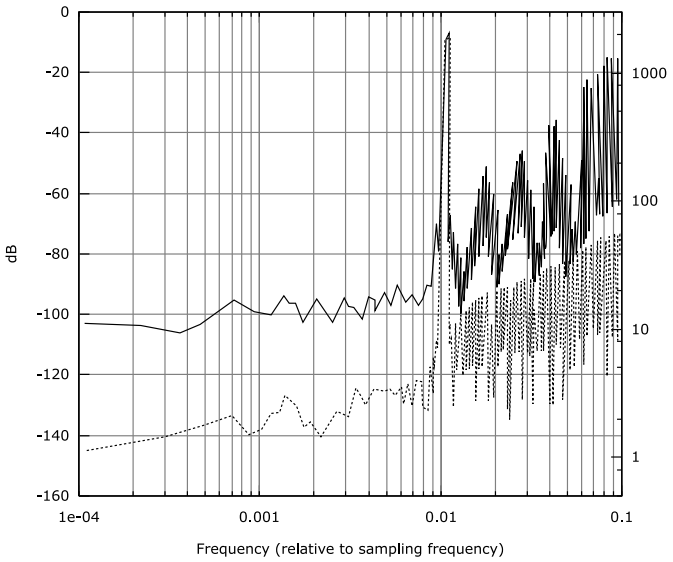


Fig. 3. Simulated output spectra of 1-b and 5-b $\Delta\Sigma$Ms

layout point of view, the mismatches are accepted as being inevitable, but processed using digital circuits. As a result, it is possible to both employ multibit quantization as well as achieve high linearity of the internal DAC. Figure 4 illustrates the nature of mismatch-shaping, and how it resembles $\Delta\Sigma$ modulation in behaviour.

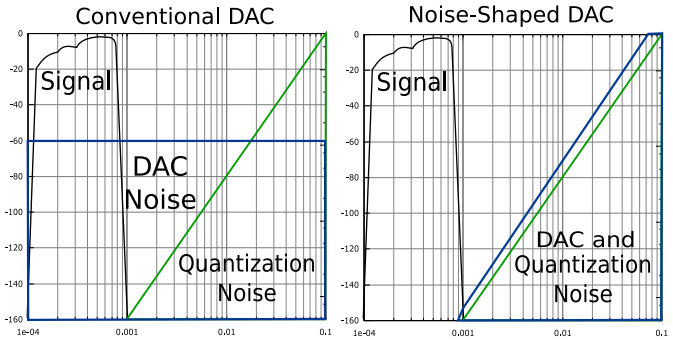


Fig. 4. Conventional vs. Noise-shaped DAC PSDs

The two classes of dynamic element matching systems are high-pass filtering [7] and randomizing [9]. High-pass filtering DEM, such as data-weighted averaging (DWA), is desirable because it spectrally-shapes the mismatch noise outside of the signal band. Randomization converts the mismatch-induced noise power in to white noise which is spread out across the range of DC to the oversampling frequency.

While high-pass noise shaping is preferable, the known high-pass DEM schemes suffer from non-idealities that can limit performance. The high-pass DEM schemes often have a correlated input and output which lead to high-power spurs in the filtered data signal. This correlation is difficult to predict without running rigorous simulations across the entire design space. In contrast, the mathematics of partial and full randomization schemes have been well-researched [10] [11].

The switching network used for implementing the fully-randomized DEM is shown in figure 5. A detailed explanation of the inner-workings is provided in [11]; in brief, the output of the 5-b quantizer represents *how many* unit DAC elements need to be activated, whereas the DEM network determines *which* unit DAC elements should be enabled. The switching network accepts the quantized 5-b value from the $\Delta\Sigma$ modulator and expands it in to a randomized selection array. The expansion is made random by using random bits to control internal switching.

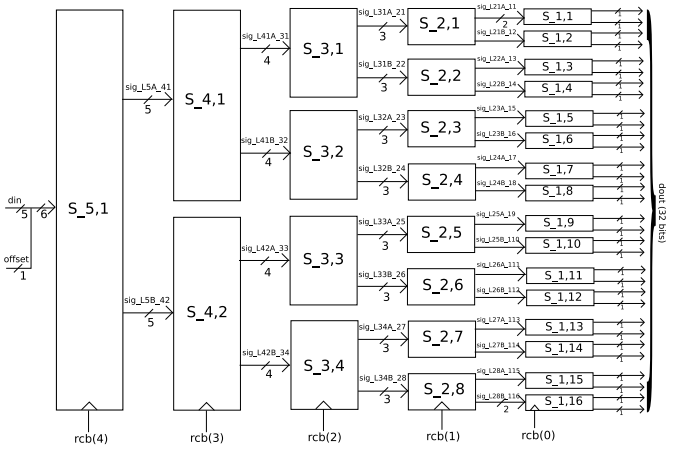


Fig. 5. DEM Switching Matrix

The quality of the random numbers has a first-order impact on the performance of the DEM system. If there is a systematic bias in the generation of the random bits which control the switching behaviour, the bias can manifest itself as distortion in the data signal. Random number generators based on sampling thermal noise across a resistor are high-quality, but are complex in imlpementation and costly in area. Hence, digital solutions such as linear feedback shift registers (LFSRs) or cellular automata (CAs) were investigated.

Autocorrelation tests can be used to determine the quality of the random numbers. However, due to the very low system signal bandwidth coupled with the very high oversampling ratio, it is easy to roll-over an LFSR or CA. A maximal-length N-bit LFSR will have $2^N - 1$ possible states. If a 32-b LFRS is used in a system clocked at 1MHz, it will repeat itself approximately every 4300 seconds. This corresponds to a frequency of 0.23mHz, which is close to the signal band. Due to folding effects, this period will appear in the data signal, thereby corrupting the SNR. Thus, maximal-length LFSRs of at least 40-b need to be used in the randomizing DEM system.

## IV. Unit DAC Architecture

Current sources are used for the unit DAC elements. Given a 5-b quantizer, the DAC must be able to create 32 distinct signal levels. If five, binary-weighted current sources are used, they are likely to suffer from a high degree of mismatch due to processing variations, and it will not be possible to perform dynamic element matching. Instead, 32 unit current sources are used in the DAC. As an example, figure 6 shows how a 3-b unit DAC array creates each required output level.

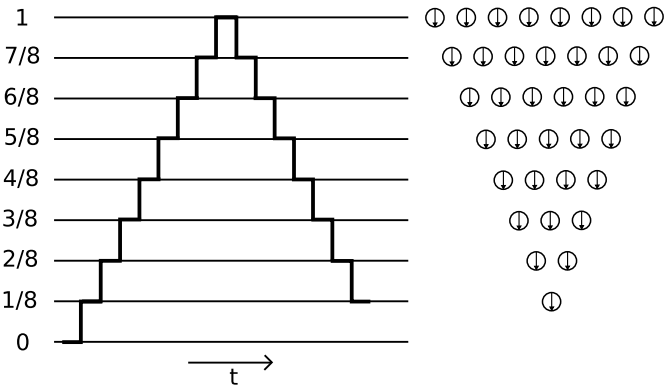


Fig. 6. Unit current sources implementing binary-weighting

The current sources are implemented as seen in figure 7. The DAC cell uses output switches M5, M6, and M7 to direct the DAC current. The current through M1 is adjustable, while M4 provides $I_0$ which provides 90% of the output current. Transistors M1 and M4 are cascoded by M3 to provide a fixed bias voltage at their drains and a high output impedance. Two current paths, $I_{dac}$ and $I_{dummy}$ are provided in order to keep the unit current sources linearly biased even when disconnected from the system analogue output.

A calibration system is used to compensate for silicon mismatch between the unit current sources. The calibration system can be seen in figure 7. In brief, the 2.5V and 5V references in conjunction with the calibration resistor produce a reference current, $I_{ref}$. This reference current is used to calibrate the gate voltage seen on M1. In doing so, static mismatch errors between the unit current sources can be compensated, thereby increasing their effective matching properties.

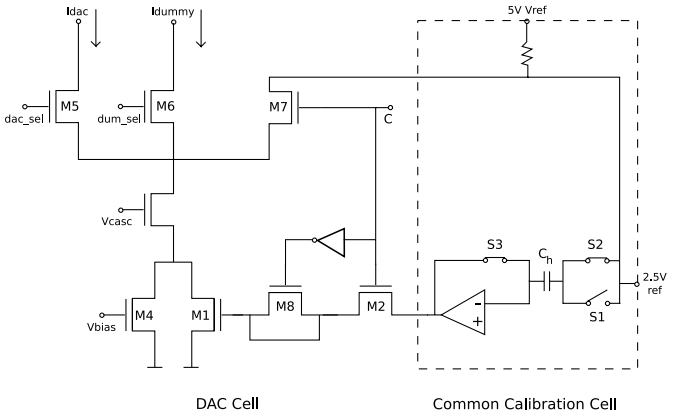


Fig. 7. Single DAC cell including the calibration cell

To conserve hardware, only one calibrator is used in the system. Since a current source cannot be used while it is being calibrated, an additional unit current source must be implemented. Thus, 33 unit current sources are required, with 32 being online at any given time, and one offline for

calibration.

The op-amp used in the calibrator can suffer from offset. This offset can be compensated using correlated double sampling (CDS). The inherent input-referred offset of the op-amp is sampled on to a holding capacitor $C_h$. When the op-amp needs to be used, the voltage across the capacitor is subtracted from the input signal, thereby negating the effects of the offset. Since the input signal bandwidth is in the range of 0.001–10Hz, clocking the CDS circuit at the system clock of 1MHz will provide a high degree of offset cancellation.

## V. Conclusion

A general architecture for a high-resolution digital-to-analogue converter has been presented. It has been shown that, given the low signal bandwidth, a second-order $\Delta\Sigma$ modulator can achieve the target SNR of $\geq$130dB at a clock rate of 1MHz. A 5-b, 32-level quantizer was used in the modulator in order to reduce truncation noise and to relax the design constraints of the analogue reconstruction filteres. A randomization-based dynamic element matching system was used to reduce the impact of static mismatch in the unit DAC elements, with linear feedback shift registers in excess of 40-b used to generate the required randomizing bits. Further, to reduce the static mismatch directly, a calibration scheme has been implemented which allows for dynamic compensation of mismatch errors in a harware-efficient manner.

## References


[1] I. Fujimori et. al., "A Multibit Delta–Sigma Audio DAC with 120-dB Dynamic Range," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, August 2000.

[2] J.G. Kenney and L.R. Carley, "Design of multibit noise-shaping data converters," *Analog Int. Circuits Signal Processing Journal*, vol. 3, pp. 259 - 272, 1993.

[3] F. Medeiro et al., "A 74dB Dynamic Range, 1.1-MHz Signal Band 4th-Order 2-1-1 Cascade Multi-Bit CMOS $\Delta\Sigma$ Modulator for ADSL," *Proc. of the 1997 ESSCIRC*, pp. 72 - 75, September 1997.

[4] I. Galton, "Delta-Sigma Data Conversion in Wireless Transceivers," *IEEE Tran. on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 302 - 315, January 2002.

[5] B. H. Leung and S. Sutarja, "Multi-bit sigma-delta A/D converter incorporating a novel class of dynamic element matching techniques," *IEEE Tran. Circuits Syst. II*, vol. 39, pp. 35 - 51, January 1992.

[6] F. Chen and B. H. Leung, "A high resolution multibit sigma-delta modulator with individual level averaging," *IEEE J. Solid-State Circuits*, vol. 30, pp. 453 - 460, April 1995.

[7] R. T. Baird and T. S. Fiez, "Linearity enhancement of multi-bit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst.*, vol. 42, pp. 753 - 762, December 1995.

[8] R. Schreier and B. Zhang, "Noise-shaped multi-bit D/A converter employing unit elements," *Electron. Lett.*, vol. 31, no. 20, pp. 1712 - 1713, September 1995.

[9] I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 808 - 817, October 1997.

[10] H.T. Jensen and I. Galton, "A Performance Analysis of the Partial Randomization Dynamic Element Matching DAC Architecture," *Proc. of the IEEE Symposium on Circuits and Systems*, vol. 1, pp. 9 - 12, June 1997.

[11] J. Welz et. al., "Simplified logic for first-order and second-order mismatch-shaping digital-to-analog converters", *IEEE Transactions on Circuits Syst. II*, vol. 48, no. 11, pp. 1014-1028, November 2001.