AN INTEGRATED A-SI TFT DEMULTIPLEXER FOR DRIVING GATE LINES IN ACTIVE-MATRIX ARRAYS

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ABSTRACT

This paper reports on the analysis, design, and implementation of integrated amorphous silicon thin film transistor demultiplexers (a-Si TFT DEMUXs) for driving the gate lines in active matrix display/imaging arrays. The integration of demultilexer into the display/imaging board reduces the pin-count of the system, and consequently the system cost. Three different integrated a-Si TFT DEMUXs are examined. The two proposed a-Si TFT DEMUX circuits outperform previously-proposed circuit by providing larger output voltage swings (OVSs), faster dynamic responses and less sensitivities to the device instability. The measurement results show a 15 to 20 percent improvement in the OVS over that of previous circuit under the same bias condition. As a key issue in the design of a-Si TFT circuits, the a-Si TFT instability, particularly the threshold voltage (V_T) shift, and its mechanisms are studied. Then, the expressions of circuit OVS sensitivity to the TFT's V_T are derived and compared. Pulse-bias stress experiments, simulating the normal conditions of operation, are conducted on the a-Si TFT DEMUX circuits, and the deviations of the circuit electrical characteristics are measured over a period of 24 hours. The measurement results are in agreement with the analysis in this work.

1. INTRODUCTION

The active matrix array is the commonly-used addressing architecture in flat-panel display/imaging systems such as Active Matrix Liquid Crystal Displays (AMLCDs), Active Matrix Organic Light Emitting Displays (AMOLEDs), and Active Matrix Imaging Arrays. The backplane semiconductor materials of the large area display/imager panels are either amorphous silicon, microcrystalline, or poly-crystalline silicon due to their high uniformities over large areas. Amorphous silicon hydrogenated thin film transistors (a-Si:H TFTs) are widely used as pixel active devices in active matrix arrays in display/imaging arrays. Multiplexers/demultiplexers

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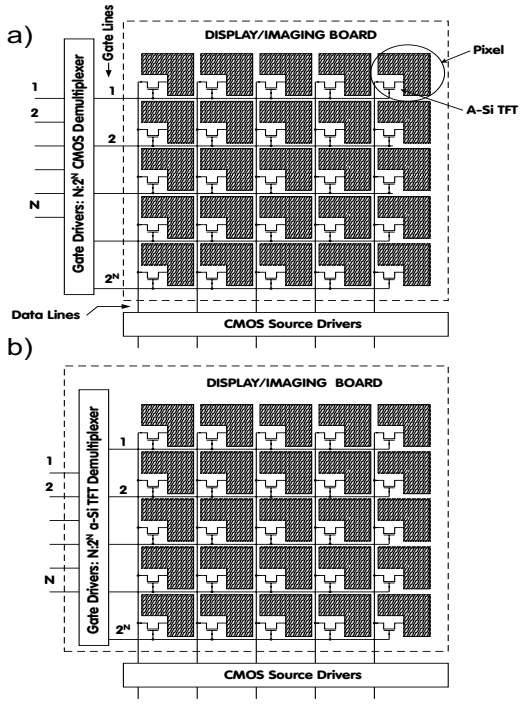

Fig. 1. (a) Active matrix arrays with off-board demultiplexer, and (b) active matrix arrays with on-board demultiplexer.

are employed in the gate/source drivers of active matrix arrays for selecting the gate/data lines to be read/written. In current commercial products, these multiplexers are implemented externally in CMOS technology. In high resolution display/imaging arrays, the pin-count of the display/imaging panel is large, and hence, the cost of external chips to multiplex and drive gate/data lines constitutes a significant portion of the cost of the overall system. As illustrated in Fig. 1, integrating multiplexers into display/imager boards can reduce the pin-count of the system from 2^N, the number of the array's gate/data lines, to N, the number of the selecting signals of the demultiplexer. This significant reduction in the pin count of the board leads to a noticeable saving in the

system's cost. The integrated multiplexer has to be implemented either in a-Si or poly-Si technologies. The analysis and design of a-Si TFT multiplexer circuits and their stability are the main focus of this paper.

2. A-SI TFT DEMULTIPLEXER ANALYSIS AND DESIGN

A-Si TFT digital circuits are different from their counterparts in CMOS technology due to the limitations of amorphous silicon technology: 1) The lack of the P-channel transistor due to the very low mobility of holes in amorphous silicon makes the use of complementary logic impossible, 2) a-Si TFT circuits operate at frequencies much lower than current CMOS circuits, since the room temperature mobility of amorphous silicon is about 1 $cm^2V^{-1}s^{-1}$ or even below, one thousand times less than crystalline silicon mobility [1], 3) and s-Si TFTs suffer from electrical instability, particularly threshold voltage shifts due to the prolonged application of bias voltage to the transistors' gates.

The only work on a-Si TFT multiplexers is published by Mohan et. al. in [2]. This Pass Logic Transistor (PTL) circuit, shown in Fig. 2 (a), has the unique advantage of employing a minimum number of transistors by sharing the transistors in the different branches; subsequently consuming a minimum die area. The main drawback of this circuit is the lack of a large OVS, leading to the employment of a larger resistor to provide an acceptable voltage swing. The V_{OH} can be calculated by equating the currents in the resistor and a-Si TFT: $V_{Out}/R_L = k/\alpha(W/L)(V_{GS} - V_T)^{\alpha}$, where α is a number between 2 and 3 and constant k is a function of the device physical parameters according to the a-Si TFT model in [3]. By replacing $V_{GS} = V_{DD} - V_{OH}$ and $V_{out} = V_{OH}$, a nonlinear equation is obtained. This equation can be solved by linearizing it around the point $V_{DD} - 2V_T$, resulting in the following:

$$VS_a = (V_{DD} - (2 - \frac{1}{\alpha})V_T)(1 - \frac{1}{1 + kR_{L(a)}\frac{W}{L}(V_T)^{\alpha-1}}). \quad (1)$$

By switching the location of the resistors and transistors, a larger OVS can be achieved. This is due to two reasons 1) Since a-Si TFTs are N-type devices, their use in pull-up network causes their currents to be a function of both the input and output voltage, reduced by the increase in the output voltage. 2) Because the ON resistance of a-Si TFTs is in the order of several $M\Omega$s, cascading these transistor leads to a very high resistive path, slowing down the circuit. The resistive load multiplexer (RL), depicted in Fig. 2 (b), provides a much larger OVS, employing much smaller load

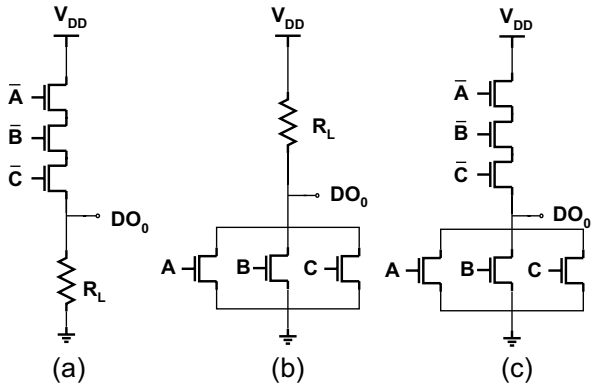

Fig. 2. Three different 1:8 demultiplexer circuits in amorphous silicon technology.

resistor. The OVS of this circuit is simply given by

$$VS_b = V_{DD}(1 - \frac{1}{1 + kR_{L(b)}\frac{W}{L}(V_{DD} - V_T)^{\alpha-1}}). \quad (2)$$

By comparing voltage swing expressions, 1 and 2 clearly indicate that the OVS of the proposed RL circuit is larger than the OVS of the PTL circuit because the first and second term are greater in 1 than in 2 assuming $V_T << V_{DD} - V_T$. It is evident that the OVS increases with the increase in the resistor value. If R_L is assumed to be large enough to make the second term almost equal to 1, the maximum OVS of the proposed circuit is equal to V_{DD}, while maximum OVS of the circuit (a) is $V_{DD} - (2 - 1/\alpha)V_T$. For both circuits to have almost the same OVS, much larger load resistors must be chosen in circuit (a). Even by equating the second terms, it can be concluded that to achieve even a close voltage swing, the following condition should be fulfilled:

$$\frac{R_{L(a)}}{R_{L(b)}} > \frac{V_{DD} - V_T}{V_T}. \quad (3)$$

For instance, for a V_{DD} of 20V and the threshold voltage of 2V, the load resistor in circuit (a) should be more than nine times larger than the resistor in the proposed circuit in order to have the same voltage swings. However, even in this condition, the PTL circuit is unable to provide a voltage swing as large as that the proposed circuit provides. It can be easily proven:

$$\frac{t_{pHL(b)}}{t_{pHL(a)}} = \frac{t_{f(b)}}{t_{r(a)}} = \frac{R_{L(b)}}{R_{L(a)}}. \quad (4)$$

Since $t_{pHL(a)} >> t_{pLH(a)}$ and $t_{pHL(b)} << t_{pLH(b)}, t_{pHL(a)}$ and $t_{pLH(b)}$ dominate the propagation delay of the respected circuit; therefore, the following can be written:

$$\frac{t_{p(b)}}{t_{p(a)}} \simeq \frac{R_{L(b)}}{R_{L(a)}} \quad (5)$$

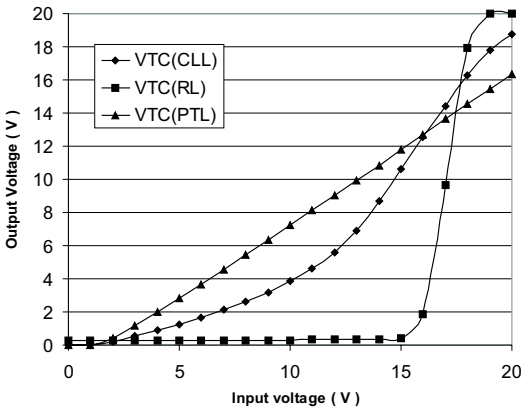

Fig. 3. Measured VTCs of the simplified branches of three demultiplexer circuits.

The large resistor in the pull-down network of the PTL-based circuit increases the high-to-low propagation delay in comparison to the low-to-high propagation delay of the RL circuit. Hence, the proposed circuit operates several times faster than the previously proposed circuit. The second proposed circuit ,circuit (c) in Fig. 2, employs only active devices, a-Si TFTs. The a-Si TFT can be fabricated in this technology with less tolerance compared to n^+ microcrystalline resistors. This circuit provides an OVS of $V_{DD} - V_T$ which is also larger than that of the PTL circuit for any value of the load resistance. The dynamic performance of the circuit also shows its superiority over the previous proposed circuits. In circuits (a) and (b) of the Fig. 2, the delay time ,for charging/discharging of the capacitor load through the resistor, takes the lion share of the total propagation delay. Due to eliminating the passive resistors in the complementary-like logic (CLL) structure of this circuit, the propagation delay reduces significantly compared to the other circuits in Fig. 2. All three circuits have been fabricated in-house for a simple 1:2 demultiplexer with a low temperature 260^oC completely wet-etch process [4]. The measured voltage transfer characteristics (VTC), the output voltage as a function of the input voltage for the three different circuits are portrayed in Fig. 3.

3. STABILITY ISSUES

A-Si:H TFTs suffer from electrical instability, when a prolonged voltage stress is applied to the TFT gate. This instability appears as a threshold voltage shift and degradation in subthreshold slope. There are two different physical mechanisms that account for the threshold voltage shift in a-Si TFTs: defect state creation [5] and charge trapping in the insulator layer [6]. Defect state creation is related to an increase in the dangling bond states in the amorphous silicon because of the broken weak bonds. Charge trapping takes place at the trap sites in the gate insulator (silicon nitride) or at the insulator/a-Si:H interface. Charge trapping dominates at a higher gate bias and longer duration of bias stress. Alternately, defect state creation is the predominant mechanism at lower gate biases as well as shorter bias stress durations. In the defect state creation, the direction of V_T shift is positive for both the positive bias stress and negative bias stress, whereas for charge trapping, the shift is in the same direction as bias stress. In addition, for negative DC bias stress, a turn around effect has been reported at high negative bias stress, where the negative charge trapping V_T shift overcomes the positive state creation V_T shift, resulting in a negative V_T shift [7] [8] [2]. The threshold voltage shift mechanism is different under DC and pulse bias stress. Defect state creation is the dominant mechanism in pulse bias stress, although charge trapping also occurs simultaneously in the same manner as the DC bias stress [9]. One approach to solve this problem is to design circuits whose characteristics are less sensitive, or insensitive, to transistors' V_T.

3.1. Threshold Voltage Sensitivity

To compare the stability condition of the three circuits, the sensitivity of their OVSs to the threshold voltage, $S_{V_T}^{VS} = V_T/VS \times \partial VS/\partial V_T$, can be calculated by differentiating the OVS equations to V_T as follows:

$$S_{V_T}^{VS_a} = -\frac{(2-1/\alpha)V_T}{V_{DD}-(2-1/\alpha)V_T} - \frac{\alpha-1}{1+kR_{L(a)}\frac{W}{L}(V_T)^{\alpha-1}}, \quad (6)$$

$$S_{V_T}^{VS_b} = -\frac{V_T}{V_{DD}-V_T} \times \frac{\alpha-1}{1+kR_{L(b)}\frac{W}{L}(V_{DD}-V_T)^{\alpha-1}}, \quad (7)$$

and

$$S_{V_T}^{VS_c} = -\frac{V_T}{V_{DD}-V_T}. \quad (8)$$

Note that the second terms in 6 and 7 is almost about 0.1 for a good design. Bye comparing the above equations, it is clear that the output voltage swing of the circuit (b) shows the least sensitivity to the threshold voltage in the order of 1%. The CLL circuit static response is a sensitivity of about 10% to V_T shift which is less PTL-based circuit the sensitivity that can exceeds 25%.

3.2. Bias Stress Measurement

This section reports the results of the pulse-bias stress experiment on a-Si TFT demultiplexer circuits. The pulse-bias stress measurements are conducted on three demultiplexer circuits, while the circuits operate under normal conditions being driven bya 20/0 V input pulse. The circuit operation is interrupted every two hours in the first 12 hours of the

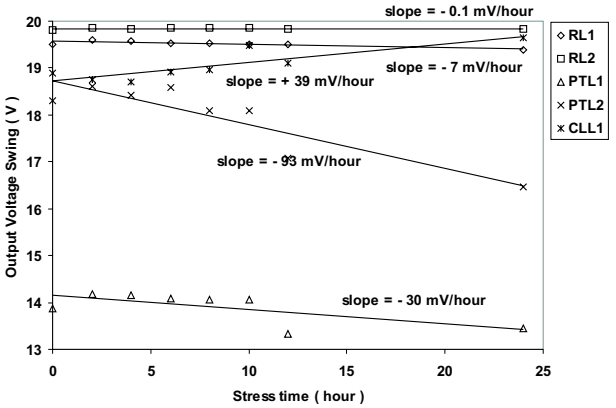

Fig. 4. OVSs of different multiplexer circuits as a function of stress time.

experiments, and then their voltage transfer characteristics (VTCs) are measured. Afetr the circuits operate for another 12 hours, and the VTCs are measured at the end of 24 hours of operation. The measured OVSs as functions of the stress time of each of these circuits are depicted in Fig. 4. The experiments are conducted on two resistive load demultiplexer circuits, RL1 and RL2, with load resistors of 96 $M\Omega$ and 238 $M\Omega$, respectively, two PTL demultiplexer circuit with the same resistor loads, PTL1 and PTL2, and on a CLL demultiplexer circuit. The a-Si TFTs in all the circuits have an aspect ratio of $230\mu m/23\mu$. Fig. 4 also shows the slopes of the extrapolated lines on the measurement data. The measurement results indicate that the RL circuit has the least OVS shift (less than -10 mV/hour) among all the circuits as expected. The PTL circuits OVS decreases significantly with time. Note that the induced V_T shift in the pull-up TFTs is less than the V_T shift in the pull-down network, because the average positive gate-source voltage of the TFTs in the pull-up network is smaller than that of the TFTs in the pull-down network. Although the induced V_T shift of the a-Si TFT in the PTL-based circuit is small; but because of the high sensitivity of OVS to V_T, this structure shows a severe OVS shift of about -100mV/hour. The OVS of CLL circuit is also noticeable. The interesting point here is that the voltage swing increases with time, which is desirable. This phenomenon occurs because the V_T shift of a-Si TFT in the pull-down network is larger than the V_T shift in the pull-down network. By increasing V_T, the a-Si TFT VTC moves toward the right. Therefore, the leakage current of pull-down a-Si TFT decreases, as long as the a-Si TFT operates in the reverse subthreshold region [3]. The lower leakage leads to a higher output voltage, since the pull-up transistor needs to provide less current, and hence, a small V_{GS} is required.

4. CONCLUSION

In this paper, two new integrated a-Si TFT demultiplexer circuits are proposed. The analysis, simulation and measurement results indicate that the proposed circuits outperform the previous PTL-based circuit. In addition to the sensitivity analysis, the normal operation experiments on the demultiplexer circuits suggests that the proposed integrated a-Si TFT demultiplexer reliability is satisfactory for long-term operation in active-matrix arrays that are used in hand-held electronic devices such as cell phones and calculators.

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