# A New Loss-Reduced Distributed Amplifier Structure

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***Abstract*—A novel loss-reduced distributed amplifier (DA), branched distributed amplifier (BDA), is presented. Unlike conventional DAs, in this structure the source/load is connected at the middle of input/output transmission lines. This technique effectively reduces the length of transmission lines and in turn lowers signal attenuation. Moreover, the optimal number of stages can be increased in the proposed structure. The final amplifier is implemented in 0.13µm IBM's CMRF8SF CMOS as two cascaded DAs with different number of stages. Post-layout simulation results show a 3-dB bandwidth of 38.5 GHz and an average pass-band gain of 20.5dB, resulting in a gain-bandwidth (GBW) product of 408 GHz. Input matching is less than -20dB and output matching is well below -10dB over the entire bandwidth. The chip area is 1.2mm by 0.6mm and power consumption is 154mW.**

## I. INTRODUCTION

Recent performance improvements driven by aggressive scaling of CMOS technology have made it possible to build low-cost radio receivers and transmitters requiring large bandwidths for high-rate data transmission [1-2]. Wideband amplifiers are the critical building blocks of broadband transceivers, the essential components of wireless communication networks [3]. Distributed amplification is considered as one of the most commonly used techniques for broadband amplification. However, losses in passive components and lower gain of active devices because of increased parasitics make broadband circuit design very challenging. Especially, undesired effect of lossy transmission line (TL) on distributed amplifier's gain is a major obstacle for design of new wideband, high gain DAs.

In this paper, we present a novel distributed amplifier structure, branched distributed amplifier (BDA), which helps reduce signal attenuation along lossy TLs. In the proposed structure, input and output are connected at the middle of transmission line while the two ends are terminated by matching resistors. As a result, traveling waves suffer from less loss on input/output TLs. This configuration along with tapering of TL segments presents a high gain structure for DA. Regulated cascode (RGC) configuration was used as the gain cell which presents higher gain compared to conventional cascode. To the best of our knowledge, this is the first time that RGC is used as a high-gain cell in DA. The final amplifier was implemented as two cascaded DAs with different number of stages. Cascading enables us to increase the internal termination resistors for higher gain.

The branched structure of DA is described in Section II. Section III explains the finals amplifier design. The post-simulation results of the proposed amplifier circuit are presented in Section IV. Finally, section V presents the conclusion of the paper.

## II. AMPLIFIER TOPOLOGY

### A. Lossy Transmission Lines

Transmission lines are important elements for MMW design. They have also been used in the design of recent wideband DAs because of area efficiency and less parasitics compared to those of spiral inductors but TLs are lossy elements. Fig. 1 demonstrates the structure of a conventional DA without the output TL and m-derived sections. It also shows the effect of TL losses on the amplitude of the traveling waves. As shown in Fig. 1, the traveling wave is attenuated more and more as it moves towards the termination resistor. Fig. 2 presents simulation results for loss of gate TL at termination resistor for this circuit. To assess the TL loss in DAs, coplanar wave-guide (CPW) structure was used in three DAs with four, five and six stages in 0.13µm IBM's CMRF8SF CMOS process. CMRF8SF is a fully RF-characterized CMOS technology in which reliable RF models for active and passive components are provided, and accompanied by their equivalent chip layout. Therefore, the simulation results in this environment carry a significant accuracy in the GHz frequency range - unlike the simulation result in a digital CMOS process. DAs were designed for 50 GHz bandwidth based on DA design methodology. TL Loss increases with frequency and the number of stages. As shown in Fig. 2, loss was highlighted in low and high frequencies. For 6-stage DA, the CPW loss at termination resistor is more than 3.5dB at 1 GHz and more than 9.0dB at 40 GHz. To alleviate the effect of TL loss, BDA structure is proposed.

### B. Proposed BDA Structure

Fig. 3 demonstrates the structure of branched DA. Unlike the conventional DA in which the input/output and termination resistors are connected to the two ends of TL, in proposed structure input/output is connected to the middle of TL while the two ends are terminated by matching resistors. In other words, the input power is halved between two branches. As shown in Fig. 3, compared to conventional DA, the distance between input signal and gain cells decreased so that the traveling waves moving toward left and right on the gate TL, tolerate less amount of loss.

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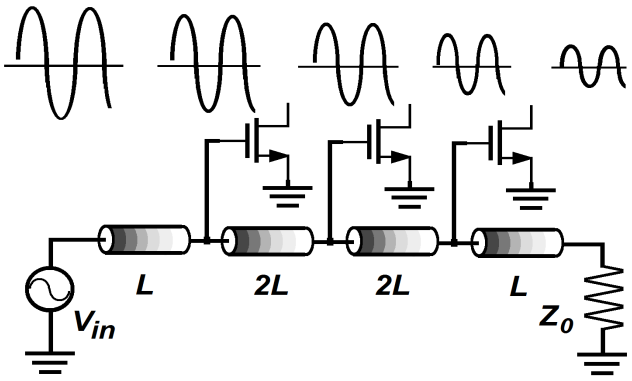



Figure. 1. Traveling wave attenuation on the gate of NMOS transistors as a result of lossy transmission lines in conventional DA.

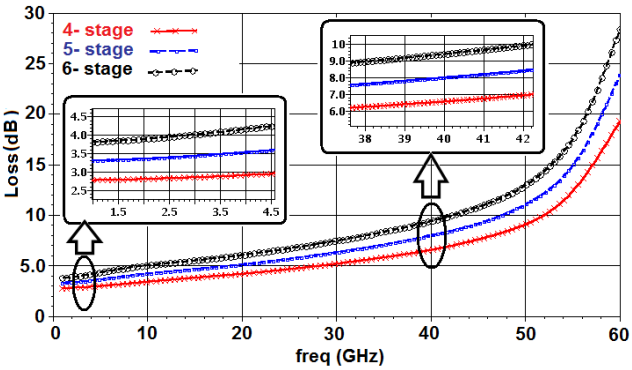



Figure. 2. Simulation results of loss of TR with CPW structure in 0.13µm IBM's CMOS process for 4-stage, 5-stage, and 6-stage DAs.

The output port of DA is connected to the middle of drain TL. Therefore, similar to gate transmission line, traveling waves tolerate lower loss on their path to the output in comparison to the conventional DA.

The cross connections of gain cells in Fig. 3 are necessary to create equal phase delay for traveling waves from input to output. In conventional DA, the source/load impedances and termination resistances are equal to $Z_0$ (typically 50Ω). To have acceptable matching in proposed structure, the termination resistors should be increased to $2Z_0$. As a result, relatively large inductances for the input/output TL are required. To keep the loss reduction capability of BDA with smaller inductances, we applied tapering to the impedance of the line segments in input/output TL. In our design, the line segment impedances are tapered (by a factor of √M) starting from the middle of input/output TL at both left and right sides towards the termination resistors and source/load. This can be achieved by changing the length of the input/output TL. Hence, using smaller inductances, TL losses decrease at input/output in comparison to conventional DA. According to the principle of distributed amplification, the gain of a DA can be written as [5]:

$$G = \frac{g_m^2 Z_d Z_g}{4} \frac{(e^{-N\alpha_g l_g} - e^{-N\alpha_d l_d})^2}{(e^{-\alpha_g l_g} - e^{-\alpha_d l_d})^2} \qquad (1)$$

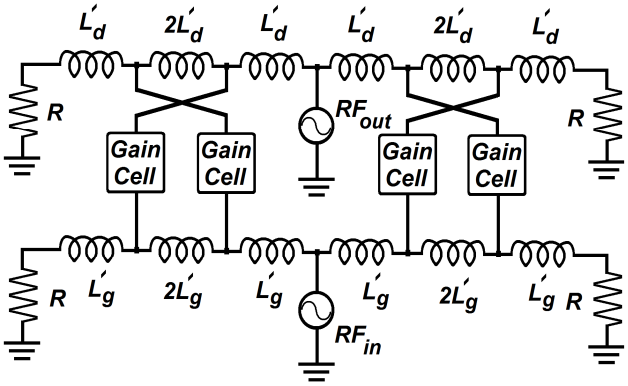



Figure. 3. Schematic of proposed branched distributed amplifier

where $g_m$ is the transconductance of the gain cells, $N$ is the number of stages, $Z_g$ and $Z_d$ are characteristic impedances of gate and drain TLs, $\alpha_g$ and $\alpha_d$ are attenuation constants, and $l_g$ and $l_d$ are the length of segment lines at gate and drain, respectively. In the proposed BDA, the effective length of gate and drain TLs ($l_g$ and $l_d$) is reduced. Therefore, DA gain increases (loss decreases) based on relation (1).

In conventional DAs, because of TL loss, the number of stages is limited to the optimal number of stages which is [5]:

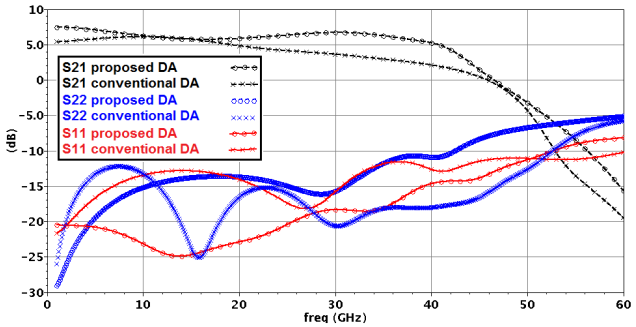
$$N_{opt} = \frac{\ln(\alpha_g l_g / \alpha_d l_d)}{\alpha_g l_g - \alpha_d l_d} \qquad (2)$$

Now consider $K$>1, as an approximate length reduction factor for both gate and drain TLs in branched distributed amplifiers. For BDA, relation (2) can be modified as:

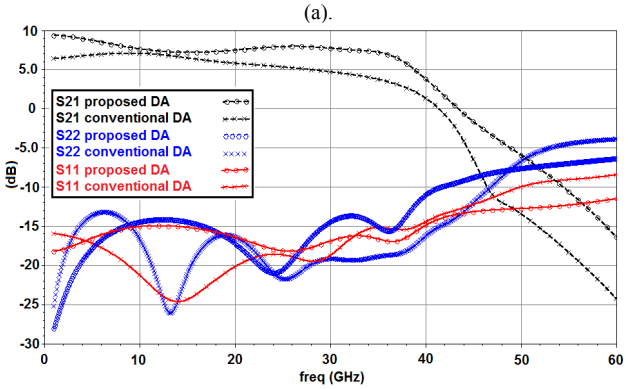
$$N_{opt} = K \frac{\ln(\alpha_g l_g / \alpha_d l_d)}{\alpha_g l_g - \alpha_d l_d} \qquad (3)$$

Hence the optimal number of stages can be increased by the factor of $K$>1 in BDA. Moreover, with tapering, output termination resistors can be chosen more than $2Z_0$ to achieve a high gain for BDA.

To evaluate the performance of the proposed structure, two 4-stage and 6-stage BDAs were designed in 0.13µm IBM's CMOS process and compared with the corresponding conventional DAs. We kept the comparison conditions the same for both BDAs and conventional DAs. The 4-stage DAs are designed for a bandwidth of 40 GHz and 6-stage DAs are designed for a bandwidth of 37 GHz. Cascode gain cells are used and the width of transistors kept the same in all designed DAs. Simulation results verify the efficiency of branched structure to reduce the TL losses. Fig. 4 demonstrates s-parameter simulation results for 4-stage and 6-stage DAs. BDAs present a higher gain (a lower loss) in comparison to conventional DAs. For the proposed 4-stage BDA, average pass-band gain is at least 1.5 dB more than conventional 4-stage DA as shown in Fig. 4(a). Proposed 6-stage BDA shows an average pass-band gain 2 dB more than that of the conventional 6-stage DA (Fig. 4 (b)). BDAs present better input matching ($S_{11}$) in comparison to conventional DAs and $S_{22}$ is less than -10 dB for the proposed BDAs over the entire bandwidth.




(a).




(b)

Figure. 4. Comparison of s-parameter simulation results for conventional DA and BDA (a) 4-stage (b) 6-stage

## III. Circuit Design

Fig. 5 illustrates the schematic of the designed loss-reduced DA. For simplicity, m-derived sections were not shown. The amplifier is composed of two cascaded DAs [4]. Cascading allows us to freely set the internal termination resistors to optimize for our desired performance. Higher gains can be obtained with increasing the internal termination resistors. The first DA is a 3-stage conventional DA with tapered line segments at drain TL while the second DA is designed as a 6-stage BDA. To avoid marginal value of -10 dB for $S_{11}$ in final chip implementation, tapering was not applied to the gate transmission line of the first conventional DA. As shown in Fig. 5, the output of first DA was connected to the middle of the gate TL in second DA.

Gain cells were designed using regulated cascode (RGC) configuration. RGC presents larger output impedance and a higher gain compared to those of conventional cascode topologies [6]. Fig. 6 demonstrates the schematic of RGC gain cell. It can be easily proven that RGC presents an approximate gain of:

$$A_v = g_{m1}g_{m2}g_{m3}r_{o1}r_{o3}R_L \qquad (4)$$

To the best of our knowledge this is the first time that RGC was used as gain cell in a distributed amplifier. Fig. 7 shows the simulation results for designed amplifier in 0.13µm IBM's CMOS process. 3-dB bandwidth is 39.5 GHz. The average gain of the amplifier is 21dB in pass-band. This high gain is as a result of proposed BDA along with tapering, and using RGC as gain cell. $S_{11}$ is well below -21 dB and $S_{22}$ is less than -12 dB over the bandwidth.

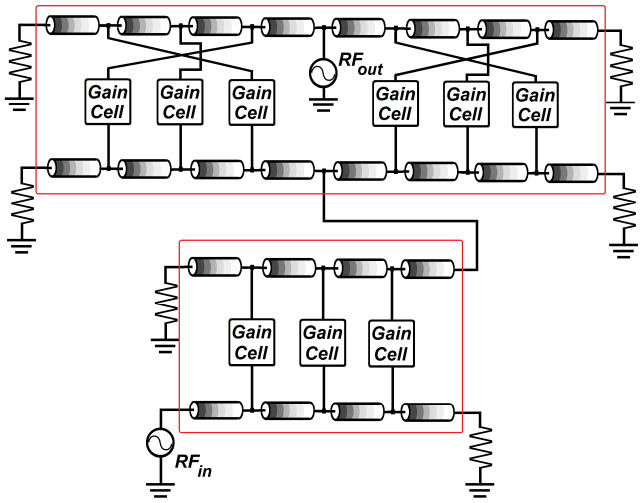



Figure. 5. Schematic of final amplifier including tapered conventional DA and BDA cascaded together (m-derive sections not shown).

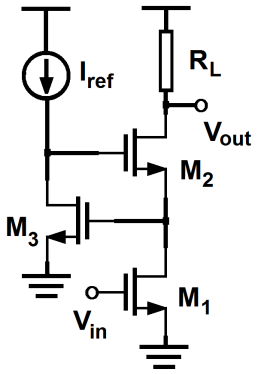



Figure. 6. Schematic of regulated cascode as gain cell.

## IV. Post-Layout Simulation Results

The proposed cascaded amplifier is designed in 0.13µm IBM's CMOS process. During layout design an iterative optimization process was employed to meet the design criteria while taking into account all parasitic elements. The amplifier layout is shown in Fig. 8. The chip area is 1.2mm by 0.6 mm. Fig. 9 shows post-layout simulation results for the implemented amplifier. The 3-dB bandwidth of cascaded DA is 38.5 GHz. The average value of $S_{21}$ is 20.5dB with less than ± 1dB fluctuations over the bandwidth. Therefore, amplifier presents a GBW of 408 GHz. $S_{11}$ is well below -20dB and $S_{22}$ is less than -10dB over the pass-band. Fig. 10 demonstrates simulated noise figure of the implemented amplifier, indicating a noise figure of less than 6.5dB over the entire bandwidth.

Power consumption is 154mW. Comparison of the performance parameters of several reported DAs in CMOS technology is presented in Table I. To the best of our knowledge, the proposed DA presents the highest GBW of all other reported DAs implemented in 0.13µm and 0.18µm CMOS technologies.

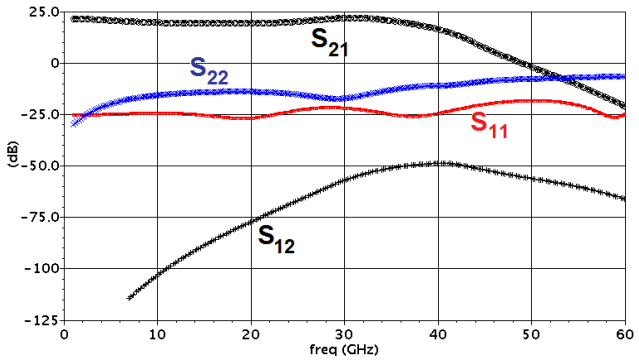



Figure. 7. Simulation results for proposed cascaded amplifier

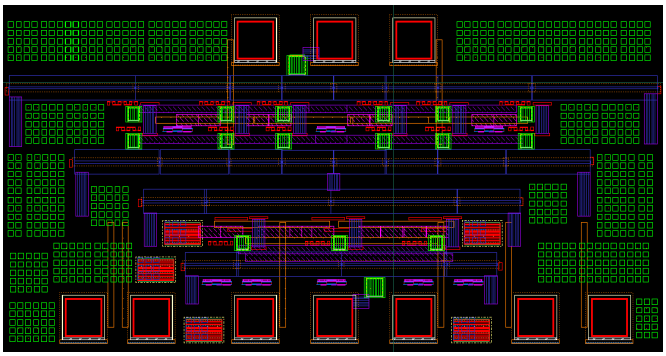


Figure. 8. Designed Layout for proposed cascaded amplifier.

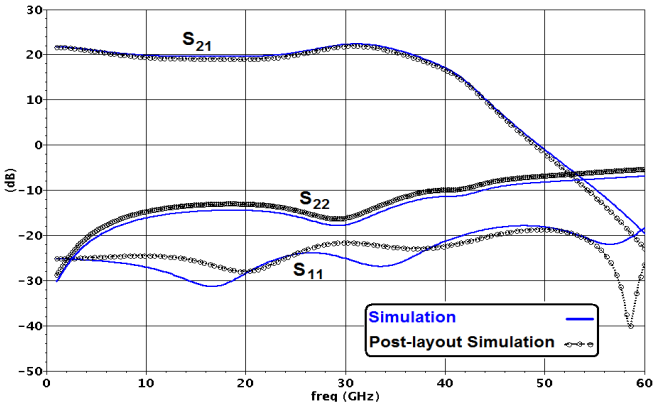



Figure. 9. Post-layout simulation results for proposed DA

## V. CONCLUSIONS

This paper has presented a novel loss-reduced distributed amplifier structure. In this structure, the source/load is connected to the middle of input/output transmission lines. As a result, the lossy transmission lines present smaller signal attenuations as the signal travels along the TLs, and consequently a higher gain that those of conventional DAs. With tapering line segments and using regulated cascode configuration for gain cells, a high-gain DA structure is obtained. Proposed cascaded amplifier achieves a 3-dB bandwidth of 38.5 GHz with a GBW of 408 GHz.

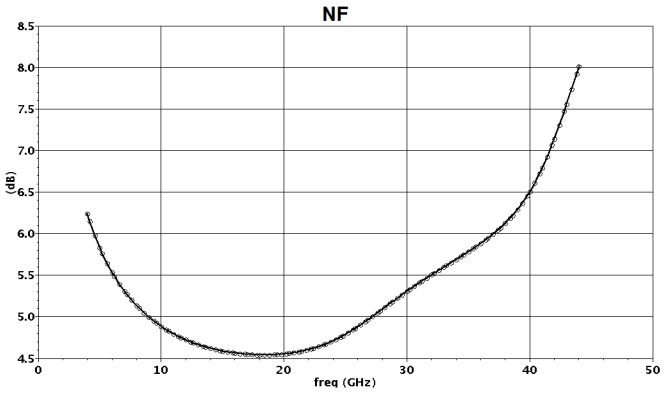



Figure. 10. Noise figure of proposed DA

TABLE I. CHARACTERISTICS OF SEVERAL REPORTED DAS

| ***Reference*** | [7] | [8] | [9] | [10] | This work |
|---|---|---|---|---|---|
| ***Technology*** | 90nm CMOS | 90nm CMOS | 0.18µm CMOS | 0.13µm CMOS | 0.13µm CMOS |
| ***GBW*** | 157 | 190 | 394 | 136 | 408 |
| ***$S_{21}$ (dB)*** | 7 | 7.4 | 20 | 9.8 | 20.5 |
| ***BW (GHz)*** | 70 | 80 | 39.4 | 43.9 | 38.5 |
| ***$S_{11}$/ $S_{22}$ (dB)*** | -7/-12 | -10/-8 | -10/-20 | -14/-8 | -20/-10 |
| ***Power (mW)*** | 122 | 120 | 250 | 103 | 154 |
| ***Area ($mm^2$)*** | 1.28 | 0.72 | 2.24 | 1.5 | 0.72 |

## REFERENCES


[1] E. Laskin, P. Chevalier, A. Chantre, B. Sautreuil, S. P. Voinigescu," 165-GHz Transceiver in SiGe Technology", IEEE Journal of Solid-State Circuits, vol. 43, no. 5, pp. 1087-100, May. 2008.

[2] B. Razavi, "A 60-GHz CMOS Receiver Front-End", IEEE Journal of Solid-State Circuits, vol. 41, no. 1, pp. 17-22, Jan. 2006.

[3] M. Michael and B. Pattan, "Millimeter Wave Propagation: Spectrum Management Implications," IEEE Microwave Magazine", pp. 54-62, Jun. 2005.

[4] J. Y. Liang, C. S. Aitchison, "Gain performance of cascade of single stage distributed amplifiers," Electron. Lett., vol. 38, no. 15, pp. 1260-1261, Jul. 1995.

[5] D. M. Pozar, "Microwave Engineering," 3rd Edition, John Wiley & Sons Inc., 2005.

[6] E. Sackinger, W. Guggenbuhl," A high-swing, high-impedance MOS cascode circuit," IEEE Journal of Solid-State Circuits, vol. 25, no. 1, pp. 289-298, Feb. 1990.

[7] M.-D. Tsai, H. Wang, J.-F. Kuan, C.-S. Chang, "A 70GHz cascaded multistage distributed amplifier in 90nm CMOS technology," ISSCC Dig. Tech. Papers, pp. 402-403, Feb. 2005.

[8] R.-C. Liu, T.-P. Wang, L. H. Lu, H. Wang, S. H. Wang, C. P. Chao, "An 80GHz travelling-wave amplifier in a 90nm CMOS technology," ISSCC Dig. Tech. Papers, pp. 154-155, Feb. 2005.

[9] J.-C. Chien, L.-H. Lu, "40Gb/s High-Gain Distributed Amplifiers with Cascaded Gain Stages in 0.18µm CMOS," ISSCC Dig. Tech. Papers, pp. 538-539, Feb. 2007.

[10] K. Moez, M. Elmasry, "A 10dB 44GHz loss-compensated CMOS distributed amplifier," ISSCC Dig. Tech. Papers, pp.548-549, Feb. 2007.