A Novel 0.6V CMOS Folded Gilbert-Cell Mixer for UWB Applications

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***Abstract*—A novel CMOS wideband mixer operating with only 0.6V power supply has been designed. Such low-voltage operation is achieved by reducing threshold voltage (V_{TH}) of the switching transistors in the folded Gilbert cell multiplier. For input RF frequency range of 3.5-8.0 GHz and IF range of 20MHz-2.5GHz, the 50Ω impedance matched condition is achieved, which make the proposed mixer suitable for UWB applications. The complete on-chip mixer is designed in 0.18-µm RF CMOS process. The proposed mixer exhibits a conversion gain of 11.0-5.5dB, SSB noise-figure (NF) of 8.0-10.0dB, and return losses (S11and S22) of less than –10 dB over frequency of 3.5-6.5GHz. The circuit consumes only 3.75mW from the DC power supply of 0.6 V.**

I. INTRODUCTION

Ultra-wideband (UWB) multi-band orthogonal frequency-division multiplexing (MB-OFDM) systems have been proposed for emerging short range and high data rate (up to 480Mb/s) wireless communications [1]. In the MB-OFDM proposal, FCC regulated 7500MHz (3.1-10.6GHz) UWB spectrum is divided into 14 bands of 528MHz each. Unlike low-noise amplifier (LNA), less attention has been paid to the design of mixer used in the receiver front-end for UWB applications. However, the problem of power supply voltage reduction was addressed, and some low-voltage broadband folded Gilbert-cell mixers have been proposed in [2]-[5]. The proposed UWB mixer in [2] can operate with as low as 0.8V power supply for the RF frequency range of 3-7 GHz giving very low conversion gain (CG). Besides it ignores ports (RF/IF) matching conditions and return losses (S11/S22).

In this paper, a very low voltage and low power, fully on-chip wideband down-conversion mixer for Mode 1 and Mode 2 MB-OFDM (3.432-6.6 GHz) UWB applications is designed. The circuit can operate with only 0.6V supply voltage. Such low-voltage operation is achieved reducing threshold voltage, V_{THP}, of p-channel transistors in the folded Gilbert cell multiplier by biasing their bulk nodes to the potential different V_{DD} (or ground for n-channel transistors). This control of threshold voltage is widely used [6] in operational amplifiers.

Biasing the bulk nodes of the p-channel switching transistors at a zero DC level reduces their threshold voltage by almost in half. The results given in this paper are demonstrated for this case of bulk connection. In this approach the maximum power supply voltage is limited as well, and the circuit operates within certain power supply range.

The proposed circuit (under the process of fabrication) is designed and simulated in TSMC 0.18-µm RF CMOS process.

This paper is organized as follows. Section II presents the proposed mixer. The design approach and circuit analysis are discussed in section III. The design realization and simulation results are presented in section IV. A brief conclusion is drawn in section V.

II. MIXER CIRCUIT

The proposed folded Gilbert-cell mixer is shown in Fig.1. RF (radio-frequency) and LO (local oscillator) signals are applied to, and IF (intermediate frequency) signals are taken from their respective terminals differentially.

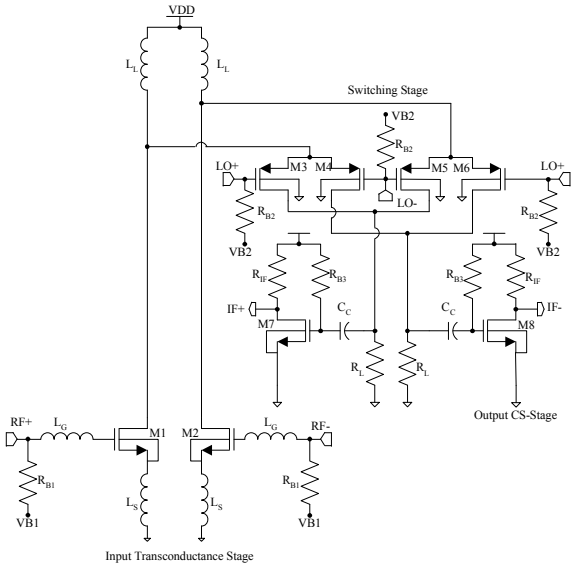


Fig.1 The proposed folded mixer for UWB applications

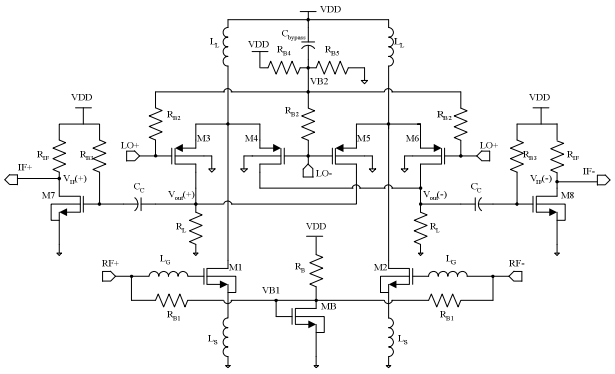


Fig.2 The complete on-chip UWB folded mixer

The input (or g_m) RF stage (transistors M1 and M2) is an inductive source-degenerated differential stage with direct biasing of the transistors (see Fig. 2). The wideband matching for the input RF signals is achieved with the inductors L_G and L_S. The switching stage consists of PMOS transistors (M3-M6) where bulk nodes of the transistors are grounded (this is not a mistake!). The differential LO port matching is achieved connecting the gates of the switching transistors through 150Ω resistors (R_{B2}) to a bias voltage *VB2*. The differential outputs (V_{OUT} + and V_{OUT} -) from the switching stage are coupled to two output common-source (CS) amplifiers through the coupling capacitors (C_C) and thus, there is no DC offset travelling from the switching stage to the final IF outputs (V_{IF} +and V_{IF} -). Wideband IF matching is achieved by the choice of the load resistor R_{IF}. Hence, all signal ports are wideband matched differentially, and only off-chip baluns are required for single-ended to differential conversion or vice versa. The complete circuit of the proposed mixer with all necessary biasing sub-circuits is shown in Fig.2.

The reduction of supply voltage is one of the most critical issues for present and future scaled-down CMOS technologies. Since folded mixer has only one active device between the power rails (and with strongly reduced V_{TH} voltage), it is a promising architecture for low voltage operation.

III. DESIGN APPROACH

In general, the folded Gilbert-cell mixer is considered as the most suitable circuit for low voltage operation. The proposed configuration includes only one stacked device in both input and switching stages. Further reduction of the supply voltage with given overdrive voltage, (V_{GS}-V_{TH}), requirement may be achieved only by reducing the threshold voltages, V_{THP} or/and V_{THN} of the transistors. Normally, $|V_{TH,P}| > V_{TH,N}$, and the connection of bulk nodes of p-channel transistors to a potential lower than V_{DD} is a sufficient measure for reduction of V_{DD} to the required value.

A. Folded Mixer Architecture

In the folded mixer architecture as shown in Fig.1, the g_m-stage has only one NMOS transistor with low-resistance inductive load (L_L) between the power rails and can easily be operated with any supply voltage (V_{DD}) slightly greater than one threshold voltage (V_{THN}). This design is more susceptible to supply voltage variation than g_m-stage using a differential pair with the tail current source [2]. Using positive body bias for the differential pair one could reduce V_{THN} as well in the technologies with double-well process.

For the switching stage (transistors M3 to M6), reducing V_{THP} allows one to decrease the overdrive voltage and increase the voltage drop across the load resistor R_L. Due to the folded architecture and inductive loading of the input stage, the bias current in the switching stage can be set independently on the input stage. Using small currents in the switching transistors one obtains a low voltage drop across the switching transistors and may increase the load resistor.

For higher conversion gain (CG), lower noise-figure (NF), and reasonable IIP3, a large DC current is required through the input g_m-stage only. Then, a large load resistor (R_L) in the switching stage also gives higher CG and lower NF. Very low DC current through the switching transistors reduces DC offset, thermal noise and *1/f* noise.

B. Output Stage

The CS output stage enhances the conversion gain and provides 50-ohm wideband matching from Low-IF (MHz) to about 2.5 GHz by a suitable choice of the load resistor (R_{IF}). Since, CS stage has very high input impedance and it is coupled to the switching stage through the coupling capacitors (C_C), it does not have loading effect on the switching stage.

C. Impedance Matching at the Ports

For most of the broadband designs, there is a severe trade-off [5] between input-impedance match and NF. For minimum NF, high Z_{in} is required whereas for maximum power transfer, Z_{in} needs to be matched with 50Ω [7]. The preference is usually given to the maximum power transfer. Because of this trade-off most of the broadband circuits show higher NF when matched to 50Ω.

The proposed mixer is fully matched to 50Ω at all the signal ports (RF, IF and LO). For maximum power transfer, the wideband matching at the RF port (3.5-8GHz) is achieved with the inductors L_G, and L_S in association with the input transconductance g_m (practically, this matching is calculated using the method of narrow-band matching [8] with low Q-factor of input circuit). LO port matching for wide frequency range (2-7GHz) ensures lower level of LO signal requirement for steering the switching transistors.

IV. DESIGN REALIZATION AND SIMULATION

The proposed UWB Mixer is designed and simulated in TSMC 0.18-µm RF CMOS process (under the process of fabrication). The input g_m-stage transistors, M1-M2 are sized to provide 1.55mA current to provide required RF gain at the bias voltage *VB1* equals to 570mV. The DC current through the output CS amplifier (M7, R_{IF}) is chosen to meet the condition of g_m = 20 miliohm^{-1} for the output impedance of 50Ω. The bias voltage *VB2* applied to the gate of switching transistors is 300mV and $|V_{THP}|$ of these transistors are

reduced to 350mV. Then, a very low DC current (25uA) is established through each of the switching transistors.

The transistor sizes are: M1-M2 (*W/L*) = 130µm/0.18µm, M3-M6 (*W/L*) =90µm/0.18µm, M7-M8 (*W/L*) =90µm/0.18µm, MB (*W/L*) =10µm/0.18µm. The resistors are: R_L =700Ω, R_{IF} =220Ω, R_B =480Ω, R_{B1}=2.5KΩ, R_{B2}=150Ω, R_{B3}=13KΩ, R_{B4}, R_{B5}=8KΩ, the inductances are L_G=2.8nH, L_S =1nH, L_L = 4.7nH and the capacitances are C_c=2.5pF, C_{bypass} (MOSFET cap) =2.5pF.

The layout of the proposed mixer is shown in Fig.3. It occupies a chip area of 0.7mm^2 (825µmx850µm). Large load inductors (L_L = 4.7nH) were implemented using two series inductors of 2.35nH (L_L/2).

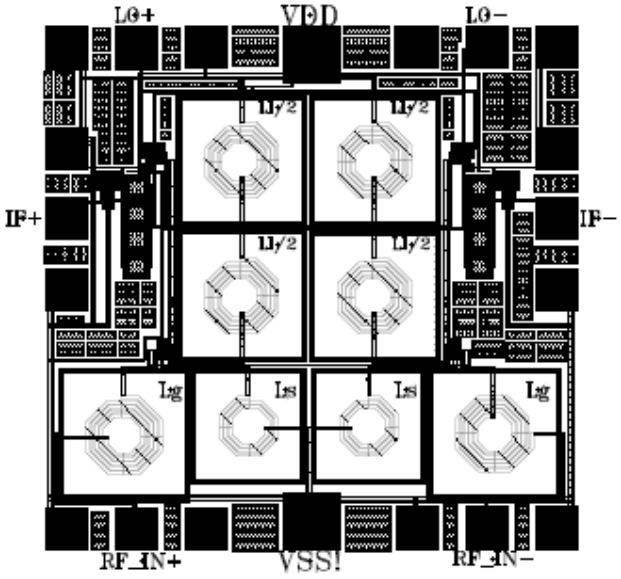
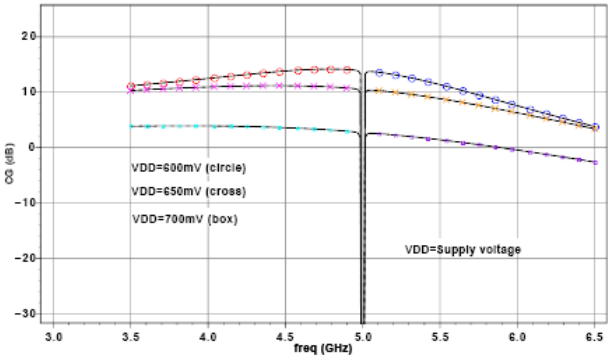


Fig.3 Layout of the proposed mixer for UWB applications

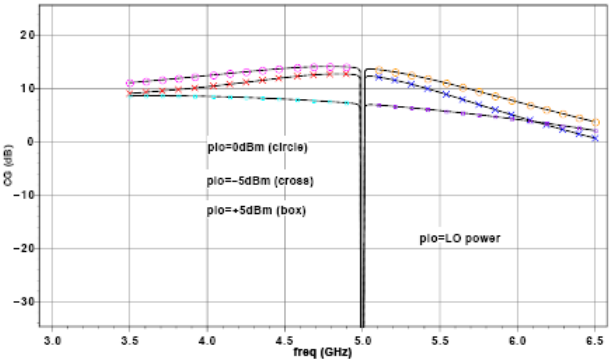
The post-layout pad-to-pad simulations were performed in a 50Ω system (the sources at RF and LO inputs have 50Ω impedance and LO port is loaded by 50Ω) with supply voltage of 0.6 V, to obtain CG, NF, IIP3, 1-dB compression point, and return losses at the ports (S11, S22). All the signal ports are single-ended and baluns were used in simulations. Since baluns do not transmit DC voltage for f_{rf}=f_{lo}, a dip shows in CG gain).

The simulation results (with 5GHz LO-frequency) for CG and NF are shown in Fig. 4 at different power supplies (VDD) and LO power levels. CG decreases with power supply voltage (it is lower at higher power supply!). Both CG and NF are the highest at 0 dBm and lowest at +5dBM of LO level.

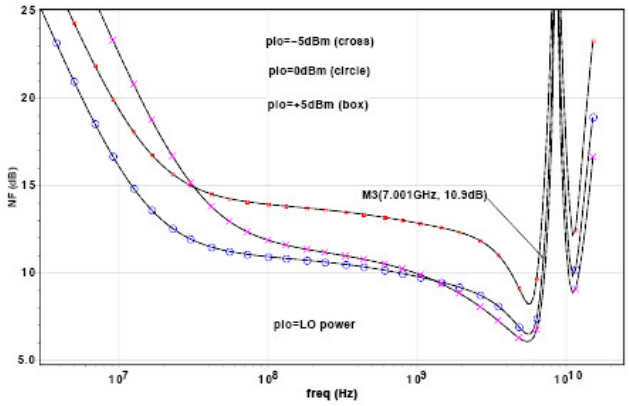
Fig.5 shows S-parameter responses where S11 (at RF port) is below -10dB from 3.5-8GHz input RF frequency range and S22 (IF port) satisfies the condition of less than -10 dB over the IF frequency range of 20MHz to 2.5GHz.



(a)CG for different power supply voltages (LO freq. is 5GHz)



(b) CG for different for different LO powers (LO freq. is 5GHz)



(c) NF for at different LO powers

Fig.4 Mixer CG and NF characteristics

Fig.6 depicts 1-dB compression point (CP). CG at different temperatures is shown in Fig.7. They show that the threshold voltage, in spite of connection of the body to ground, is still high enough, and its change with temperature may be neglected.

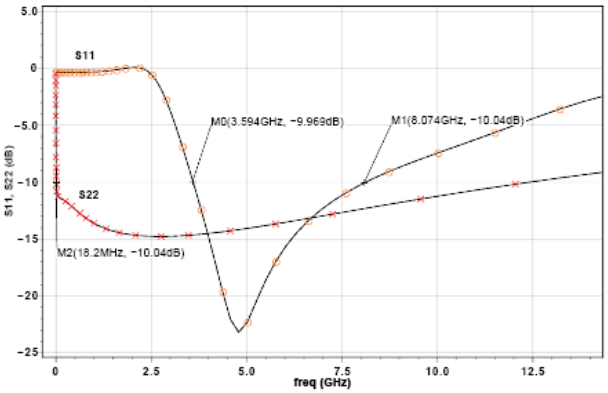


Fig.5 S-parameter responses: S11 (RF port) and S22 (IF port)

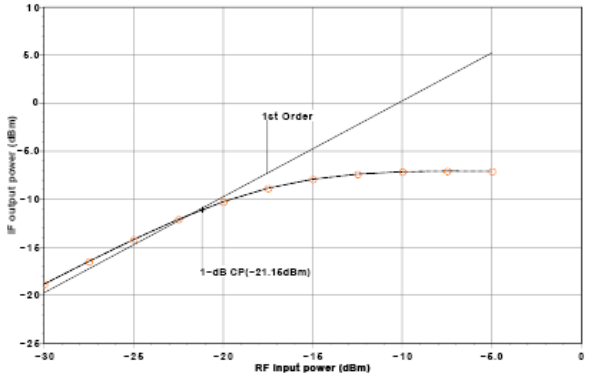


Fig.6 1-dB CP at RF=5.5 GHz, IF=500MHz with LO power 0dBm at 5GHz

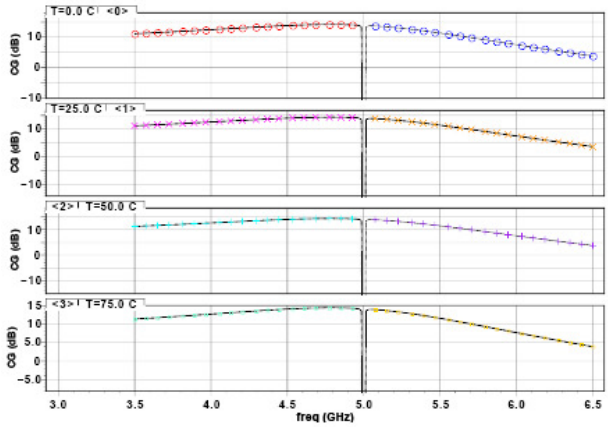


Fig.7 CG at different temperatures (stable CG over temperatures)

Table-1: Summary of mixer performances

Technology	0.18-µm
Frequency range	3.5-6.5 GHz
CG	11.2- 5. 5dB
SSB NF	8-10.0dB
1-dB CP	-21dBm
Power	3.75mW @ 0.6V
Chip area	825µmx850µm

V. Discussion and Conclusion

The reduction of the V_{TH} voltage (both for p- and n-cannel transistors, depending on technologies) may be considered as a viable way for reduction of the power supply voltage. Yet, the practical application of this method requires the development of body potential control circuits similar to that used now in some Op-Amp design [6]. The circuit temperature behavior should be carefully simulated, and one has to check that the circuit operation is not influenced by temperature. The circuit performance can be optimized for a chosen power supply voltage. Contrary to common approach the performance of the presented circuit deteriorates with excessive increase of power supply voltage because body-source diode of p-channel devices starts to conduct. Therefore, the power supply voltage should be limited to 0.8 V.

A novel CMOS wideband mixer operating with only 0.6V was designed based on the proposed approach. For RF frequency range of 3.5-8.0GHz for the input signal, the 50Ω output matched condition is achieved for IF frequency in the range of 20MHz-2.5GHz, which make the proposed mixer suitable for UWB applications. The circuit design assumes the knowledge of body-substrate cut-in voltage and good temperature model of transistors.

References

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