A 20-Stage CMOS Distributed Amplifier using CMOS Interconnects for Artificial Transmission Lines

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Abstract

This paper presents an area-efficient 20-stage distributed amplifier implemented in 0.18 μm CMOS process. To implement the artificial transmission line of the distributed amplifier, single-wire CMOS interconnects are employed instead of conventional on-chip spiral inductors. Based on this technique the area of CMOS DA is minimized to 0.4 mm^2. Implemented DA exhibits a gain of 9 dB and a unity gain bandwidth of 27 GHz. Input and output return losses are less than 12 and 8 dB, respectively.

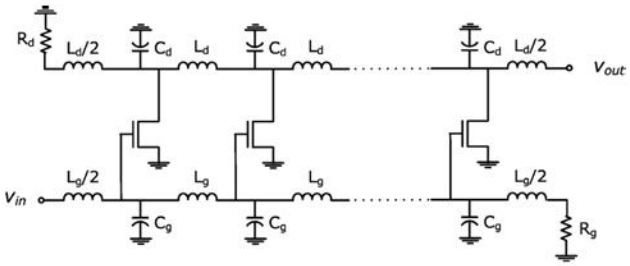
Introduction

Distributed amplification is widely used as a circuit technique to achieve a constant amplification and good input/output matching over a large frequency band. Conventional microwave DAs are constructed of two TLs that connect the drain and gate terminals of several field effect transistors (FETs). In CMOS, the TLs are artificially constructed of a ladder of lumped-element inductors and capacitors as portrayed in Fig 1. The intrinsic capacitors of transistors – the main cause of bandwidth limitation – are separated by series on-chip inductors to form a lowpass filter topology. This structure provides a relatively low gain due its additive nature of the paralleled gain cell, but achieves wideband amplification due to distribution of the parasitic capacitors in a lowpass LC circuit topology. While several implementation of inductors have been reported in the literature [1-9], the only viable integrated solution to use spiral on-chip inductors implemented on the thickest metal layer of the process.

CMOS Interconnects

The main drawback of a fully integrated DA is its large die area as it requires 2N+2 spiral inductors for an N-stage implementation. These on-chip spiral inductors and minimum separation form each other determine the total area of the chip. Considering that the area of the on-chip spiral inductors, and consequently the area of the CMOS DAs does not scale with the technology's feature size, it is necessary to explore alternative implementation of the inductors for cost-effective fully integrated CMOS chips.

In this paper, we use single wire top-metal interconnects to provide the inductances needed for the gate and drain transmission lines. The interconnects are modeled using an EM simulator in a three-dimensional environment. Based on EM-simulated S-parameters, the equivalent circuit, shown in Fig. 2, is produced to be supplied to a circuit simulator. Parallel RL networks with mutual inductance are added to the equivalent circuit to model the changes in series inductance and resistance with frequency. C_{ox1} and C_{ox2} simulate the capacitive coupling between the interconnect and substrate. R_{sub1} and R_{sub2} represent the resistive substrate loss. The resistive loss and substrate loss of the interconnects reduce the gain of the amplifier and degrade the input/output matching as frequency increases, preventing the DA from achieving its expected bandwidth.



$$BW_{gate} = \frac{2}{\sqrt{L_g C_g}} \qquad BW_{drain} = \frac{2}{\sqrt{L_d C_d}}$$

$$Z_{gate} = \sqrt{\frac{L_g}{C_g}} \qquad Z_{drain} = \sqrt{\frac{L_d}{C_d}} \qquad S_{21} \cong \frac{1}{2} g_m Z_L N$$

Fig. 1. Schematic diagram of CMOS DA, and expressions for bandwidth, characteristic impedance, and gain [9].

CMOS DA Design

The first step in the design of a distributed amplifier is to find the values of the capacitors and inductors of the gate

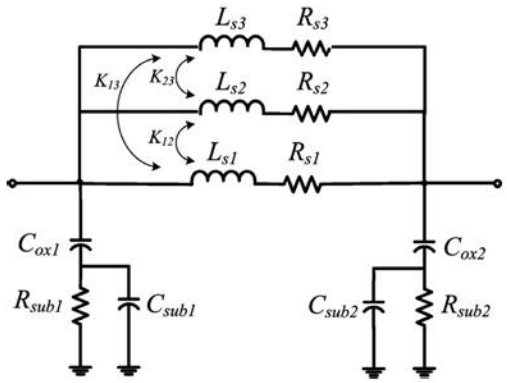


Fig. 2. Equivalent circuit of CMOS interconnects.

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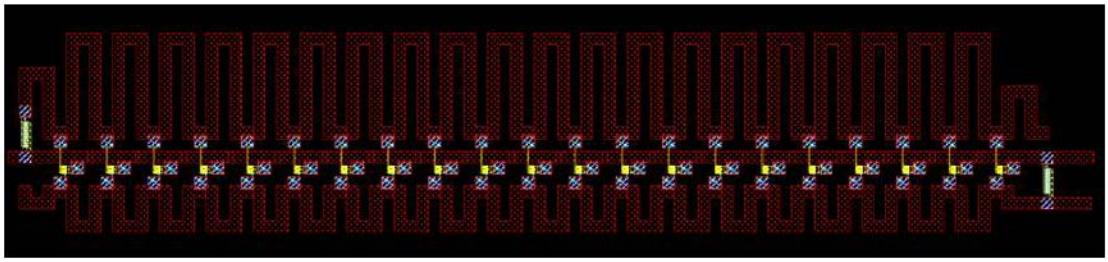

Fig. 3. Chip layout of twenty-stage CMOS DA.

and drain transmission lines such that they provide the required bandwidth of the DA. Since the limited quality factor of the interconnects significantly reduce the gain of the DA at higher frequencies, we choose an ideal bandwidth several times larger than that we expect in the presence of the resistive loss of the interconnects and substrate loss. As a proper DA design requires equal signal delays on the gate and drain transmission lines, the gate and drain transmission lines' bandwidths are required to be equal.

To ensure proper matching at input/output ports, the characteristics impedance of the gate and drain transmission lines, Z_{gate} and Z_{drain}, must be chosen equal to or close to the terminating resistors of the lines, R_g and R_d, respectively. If the DA is not connected to an off-chip load, it is not required to match the output line to a 50Ω load. Instead, we choose to terminate the output transmission lines with a 100Ω to improve the gain of the amplifier. The ratio of 2 to 1 for Z_{drain} to Z_{gate} is chosen because the total parasitic capacitance at the gate of the NMOS transistors is almost twice as the parasitic capacitance at the drain terminal. Therefore, there is no additional capacitor is needed to equalize the bandwidths of the gate and drain transmission lines as the inductors of the drain TL are two times larger than those of the gate TL ($L_d \quad 2Lg$ *and* $C_g \quad 2C_d$) . This condition implies the drain interconnect length are required to be two times of the gate interconnects length.

Co-Simulation

Assume that we have a network with N passive sub-networks and M active sub-networks. Using a standard network analysis procedure, we can find the final S parameters of the network as a function of its passive and active sub-networks' S parameters:

First, identify the internal and external ports of the network: internal ports are those ports that are terminated (load/ground) or connected to an adjacent sub-network. The rest of the ports, external ports, are those that act as ports of the main network. Assume that the network has K external ports and J internal ports. Next, record the information in the following (K+J) (K+J) matrix:

$$\begin{bmatrix} V_E^- \\ V_I^- \end{bmatrix} = \begin{bmatrix} S_{EE} & S_{EI} \\ S_{IE} & S_{II} \end{bmatrix} \begin{bmatrix} V_E^+ \\ V_I^+ \end{bmatrix} \tag{1}$$

where V_E^+, V_E^-, V_I^+, and V_I^- are the vectors of the incident and reflected voltages of external and internal ports, respectively. The element of matrices S_{EE}, S_{EI}, S_{IE}, and S_{II} are easily given by the equation

$$S_{ij} = \begin{cases} 0 & \text{if there is no direct relation between} \\ & \text{i and j through any of the subnetworks} \\ S_{ij\ \ subnetwork} & \text{if there is a direct relation between} \\ & \text{i and j through one of the subnetworks} \end{cases} \tag{2}$$

Next, find the connection matrix Γ for the internal ports: In this step, we enter the network connection configuration using connection matrix

$$V_I^- = \Gamma V_I^+ \tag{3}$$

The elements of Γ are given by the relation imposed on the internal ports by the interconnection among the sub-networks. For example, if port X of sub-network Y is directly connected to port X' of sub-network Y', the following relations shall be plugged in the connection matrix as

$$V_{X'}^- = V_X^+ \ \text{and} \ V_X^- = V_{X'}^+ \tag{4}$$

These relations set two elements, $S_{XX'}$ and $S_{X'X}$, of the Γ equal to 1. In another case, if port Z is terminated in a load with a reflection coefficient of Γ_L, the relationship

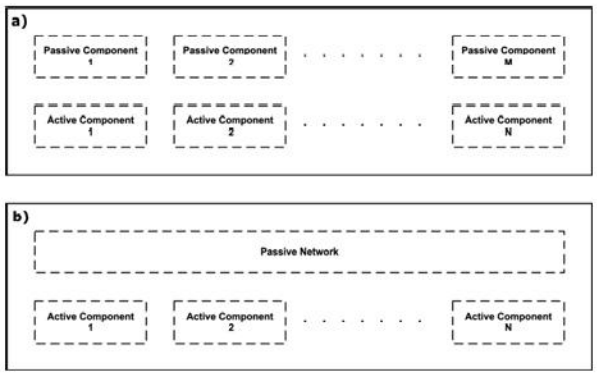

Fig. 4. a) EM-modeling of individual passive components, and b) EM-modeling of combined passive network.

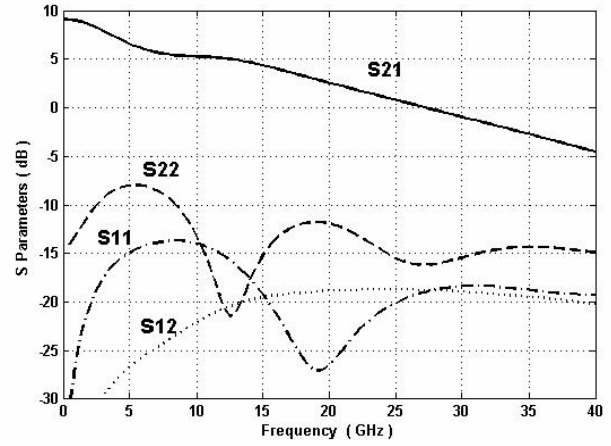

Fig. 5. S parameters simulation results.

$$\frac{V_Z^+}{V_Z} = \Gamma_L \qquad (5)$$

sets the value of S_{ZZ} in the connection matrix equal to $1/\Gamma_L$.

In the final expression of the equation, the final S parameters of the external port of the network can be obtained using

$$S^R = \frac{V_E}{V_E^+} = S_{EE} + S_{EI}[\Gamma - S_{II}]^{-1} S_{IE} \qquad (6)$$

Results and Conclusions

The proposed DA circuit is laid out in an area of 400 µm×1000 µm, and fabricated in a standard 0.18 µm TSMC CMOS technology with six metal layers. The TLs' interconnects are implemented onto metal 6 layer with thick metal option that extends the metal thickness to 2 µm. The chip layout of the fabricated chip is shown in Fig. 3.

The S-parameter simulation results are shown in Fig 5. The simulated gain (S_{21}) of the amplifier is 9 dB. The values of S_{11}, S_{22} and S_{12} are limited to -12 dB, -8 dB and -18 dB within the DA's bandwidth, respectively.

Table 1. Performance comparison of published CMOS DAs.

Technology (µm) and [Ref]	Bandwidth (GHz)	Gain (dB)	Area (mm2)
0.6 [1]	5.5	6.5	1.4×0.8
0.6 [2]	8.5	5.5	1.3×2.2
0.35 [3]	5.5	20	0.95×1.8
0.18 [4]	>11	18	1×2.2
0.18 [5]	15	8	1.3×1.8
0.18 [6]	24	7.3	0.9×1.5
0.09 [7]	70	7	0.9*0.8
0.09 [8]	80	7.4	1.2×0.6
0.18 [*]	27	9	0.4×1

* This work

Table 1 compares the performances and die areas of the previously published DAs with the one proposed in this work. The area of the proposed DA is 45% smaller than the die area of the smallest CMOS DAs reported in the literature.

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