Distributed Current Mode Logic

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Abstract—This paper introduces a new high-speed CMOS logic family called distributed current mode logic (DCML). This architecture is a combination of existing current mode logic (CML) architecture and the concept of distributed circuits. Distributed current mode logic takes advantages of distributed circuit, and is able to work up to 80 GHz in 0.13 μm CMOS technology. Because of the low noise behavior of the current mode logic family, DCML generates low power/substrate noise. Differential implementation of this logic makes it more immune to the noise generated by other blocks. These properties make this architecture a good candidate for very high-speed data communication integrated circuits.

I. Introduction

In today's society, there is an increasing demand for high-speed communication and fast data transmission [1]. Integrated circuits are one of the best solutions to realize this communication link. Integrated circuit implementation provides less power dissipation and higher performance than discreet circuit realization. A high-speed digital logic circuit is required to realize the high-speed data communication micro-chips; for example, on the receiver side, *Phase Lock Loop* (PLL) or *Clock and Data Recovery* (CDR) blocks employ high speed digital circuits [2, 3]. Implementation cost is an important issue: bipolar technologies are much more expensive to apply than CMOS technology. But CMOS technology offers more advantages than related technologies, except for high-frequency operation [4]. State-of-the-art standard CMOS logics cannot perform at more than 8 GHz [5-7]. Different techniques and architectures have been introduced to increase the speed of digital circuits [8, 9]. This paper introduces a novel architecture that is able to operate at higher frequency than the architectures of existing architectures and methods. The next section of the paper presents a review of the existing current mode logic method. Section III is devoted to the concept of distributed circuits, particularly on distributed amplifiers. Section VI explains the novel distributed current mode logic architecture. Section V compares current mode logic with distributed current mode logic, and Section VI presents the conclusions.

II. Current Mode Logic

MOS Current Mode Logic (MCML) has been introduced in [9]; it originated from emitter couple logic (ECL) [10]. The main concept in MCML is to reduce the voltage swing and switch the current to increase the frequency of switching. The MCML inverter shown in Fig. 1 explains the architecture and operation of Current Model Logic circuits.

The MCML inverter has the exact same architecture as a differential amplifier. A tail current source is connected to a differential pair transistor and pull-up resistors. The operation of the MCML logic is based on the differential pair circuit. The value of the input variable controls the flow of current through the two branches of the differential pair. In MCML logic, both of these transistors Q1 and Q2 work in saturation or linear regions. There is no need for the transistors to be completely off. Normally, designers try to have a ratio of around 10% and 90% of the tail current, I_{tail}, in the branches. For example, if V_{in+} is higher than V_{in-}, then most of the current passing through Q_1 exceeds the current passing through Q_2. Therefore, the positive output voltage begins to drop until it reaches a steady state, at which point the current through the resistor R1 matches the current through transistor Q1. In the

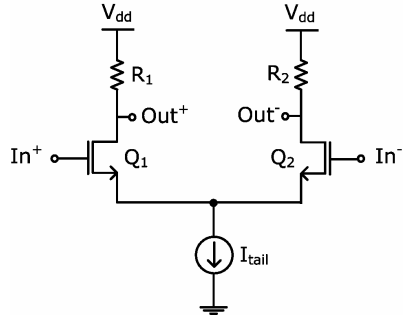

Fig. 1. MCML Inverter Cell.

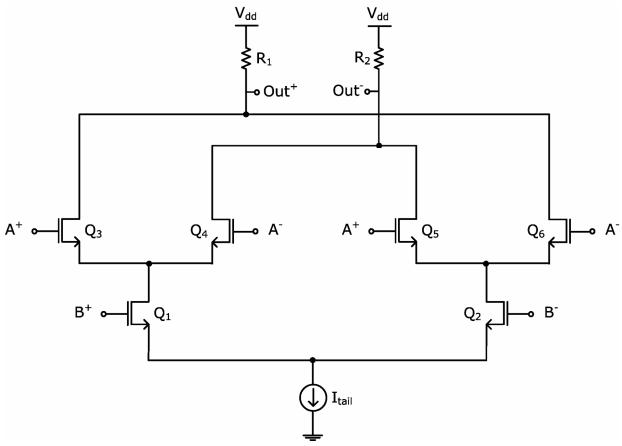

Fig. 2. MCML XOR Gate.

meantime, the negative output voltage is charged to supply voltage (VDD) through resistor R_2.

MCML circuits are faster than other logic families, because they use NMOS transistors only and because these transistors operate only in the saturation or linear regions. The small output swing of MCML circuits reduces the cross talk between adjacent signals. The constant current source reduces the switching noise and supply fluctuations. For these reasons, MCML is recommended for mixed signal design to reduce the interference between the digital and analog blocks [11]. Because of the differential nature of MCML, MCML circuits have high noise immunity; the technology has therefore been recommended for high-speed application [12]. Other essential digital blocks can also be built in this architecture. Fig.2 shows XOR gate implemented in MCML logic.

III. Distributed Amplifiers

The theory of distributed or traveling-wave amplification using discrete transistors concerns a technique whereby the gain–bandwidth product of an amplifier may be increased. In this approach, the input and output capacitances of the transistors are combined with lumped inductors to form artificial *transmission lines* (TL). These lines are coupled by the trans-conductance of the devices. The amplifier can be designed to give a flat, low-pass response up to very high frequencies. [13] A distributed integrated circuit design is one of the effective approaches for the design of optical communication ultra-wideband circuits, particularly in CMOS technology [14]. Early distributed amplifiers were implemented using vacuum tubes and high-speed GaAs MESFETs [15-19]. Wide-band pre-amplifiers and gain-controlled amplifiers (or limiting amplifiers) are the key building blocks of optical receivers [20]. Since distributed amplifiers (DAs), unlike other amplifiers, have no gain-bandwidth trade-off, they can offer wide-band amplification for high-speed application.

Conventional microwave DAs are constructed of two TLs that connect the drain and gate terminals of several field effect transistors (FETs). Since CMOS interconnects with typical length – less than a few hundred μms – are not considered to be TLs at frequencies up to 80 GHz, the TLs are artificially constructed of a ladder of lumped-element inductors and capacitors, as portrayed in Fig. 3. The intrinsic capacitors of transistors – the main cause of bandwidth limitation – are separated by series on-chip inductors to form a low-pass filter topology. This structure provides a relatively low gain due to the additive nature of the paralleled gain cell, but achieves wideband amplification due to distribution of the parasitic capacitors in a low-pass LC circuit topology. The main drawback of DA topology is its large die area because the system requires several on-chip inductors in the circuit topology. As with two cascaded low-pass LC filters, the maximum

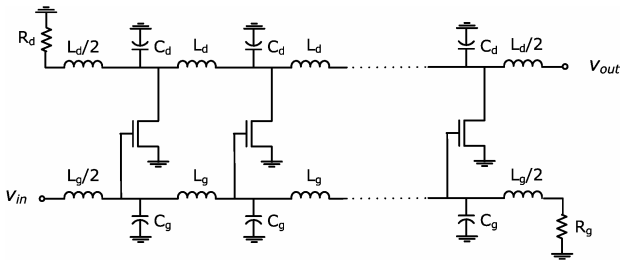

Fig. 3. Distrbiuted Amplifier

bandwidth of a DA is limited to the cutoff frequencies of its artificial gate and drain TLs. In practice, the bandwidth is further limited by the resistive loss of the TLs and by the output resistance of the amplifier cell gains.

IV. Distributed Current Mode Logic

Appling the distributed circuit concept to current mode logic circuits results in a new logic family, *Distributed Current Mode Logic* (DCML). DCML can operate up to very high frequencies because of the nature of distributed circuits. Fig. 4 shows the schematic diagram of a DCML inverter. The functionality of an inverter cell is almost the same as that of a differential distributed amplifier. Main digital cells can also realized in DCML, such as XOR, DFF.

DCML XOR has two differential inputs and one differential output. Both input nodes need to be considered as high-speed nodes connected through distributed LC network. Fig. 5 shows a schematic diagram of a DCML XOR.

The fist step in the design of a DCML gate is to find the values of the capacitors and inductors of the gate and drain transmission lines. The bandwidths of the gate and drain transmission lines are given by

$$BW_{gate} = \frac{2}{\sqrt{L_g C_g}} \quad and \quad BW_{drain} = \frac{2}{\sqrt{L_d C_d}}. \qquad (1)$$

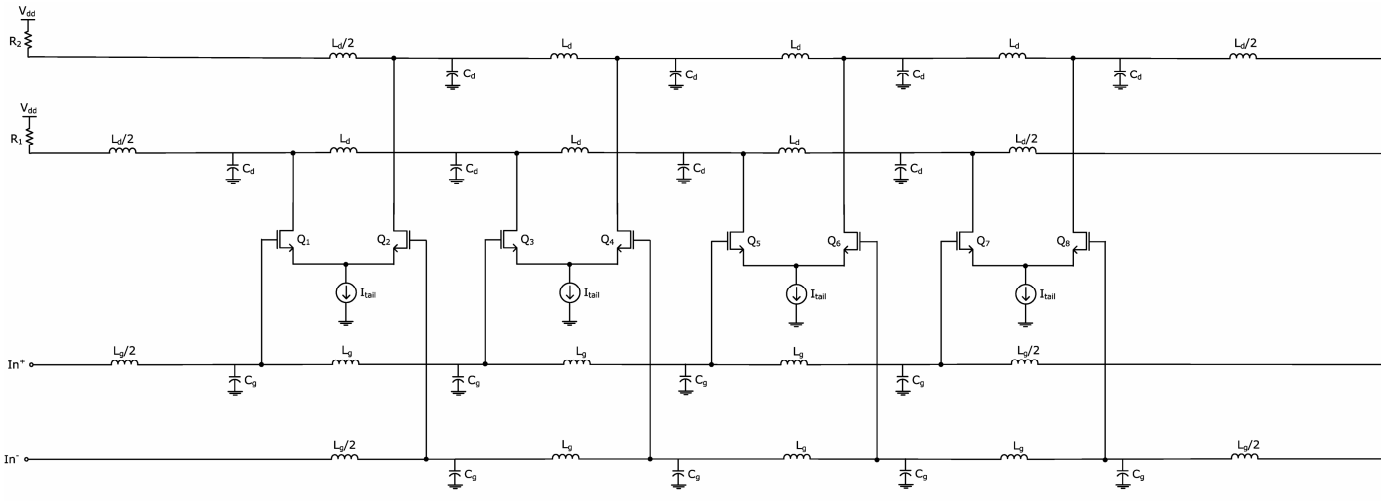

Fig. 4. DCML Inverter cell.

where Lg, Ld, Cg, and Cd are the inductor and capacitor of the gate and drain transmission lines. The required bandwidth is determined by the transmission rate of the digital data. For example, if the data rate is 40 Gbps, the desired bandwidth of the distributed amplifier is between 70% and 100% of the data rate, meaning 28 GHz to 40 GHz in this case. The voltage gain of a distributed amplifier is given by

$$A_v = ng_m \sqrt{Z_{gate} Z_{drain}}, \qquad (2)$$

where Zgate and Zdrain are the characteristic impedance of the gate and drain transmission lines, and can be expressed as

$$Z_{gate} = \sqrt{\frac{L_g}{C_g}} \quad and \quad Z_{drain} = \sqrt{\frac{L_d}{C_d}}. \qquad (3)$$

To ensure proper matching at input/output ports, the characteristics impedance of the gate and drain transmission lines, Zgate and Zdrain, must be chosen equal to, or nearly equal to, the terminating resistors of the lines, Rg and Rd, respectively. Since a proper DA design requires equal signal delays on the gate and drain transmission lines, the bandwidths of the gate and drain transmission lines are required to be equal. If the input and output ports are terminated with the same resistors, then this condition necessitates that the values of the inductors of capacitors of both lines be equal, that is Lg=Ld and Cg=Cd. Note that Cg and Cd are the total capacitance seen from the corresponding nodes of the circuit, including the parasitic capacitors of the transistors and on-chip inductors. Therefore, the parasitic capacitors set the minimum values of Cg and Cd and, consequently, the maximum achievable bandwidth of the transmission lines.

V. COMPARISSON

The outputs of the MCML inverter (Fig. 1) and DCML inverter (Fig. 4) are compared in Fig. 6. Simulation results show the latency in the output of DCMLs even though this latency exists in the result of the distributed amplifier. For most of the applications, such as phase detector block in PLLs and CDRs, latency is not an important issue while rise-time and fall-time are the main concern.

All the simulations have been performed in 0.13µm

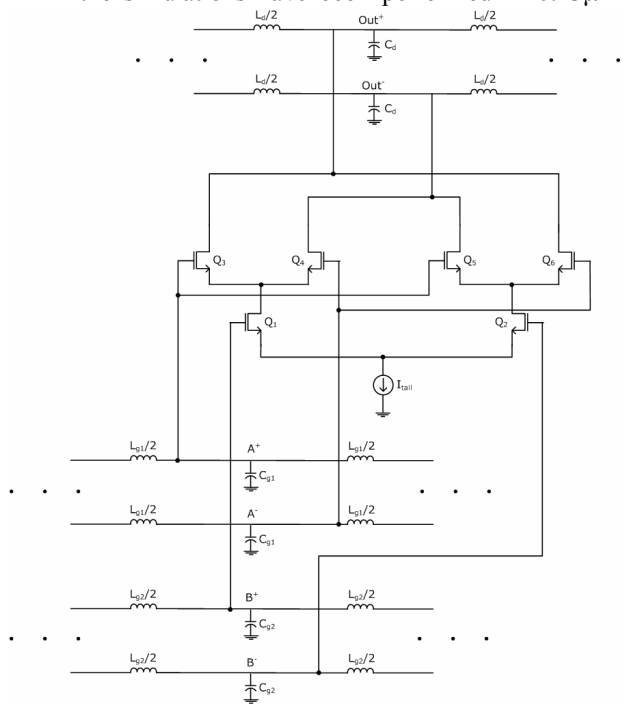

Fig. 5. Single stage of DCML XOR cell.

CMOS technology, showing that the cells are able to work in the frequency range of 80GHz. The required voltage gain for digital cells is 1V/V. Targeting this small gain helps designers to increase the frequency of operation. Fig. 7 compares the outputs of the MCML and DCML XOR gates shown in Fig. 2 and 5, respectively.

VI. CONCLUSION

In this paper current mode logic family and distributed amplifier have been studied. A new distributed current mode logic family (DCML) has been launched; DCML and CML have been compared. Simulation results show that the distributed-current mode logic family can be used for a wide range of very high-frequency system-on-chip applications, such as clock and data recovery block in the receiver block of optical communications.

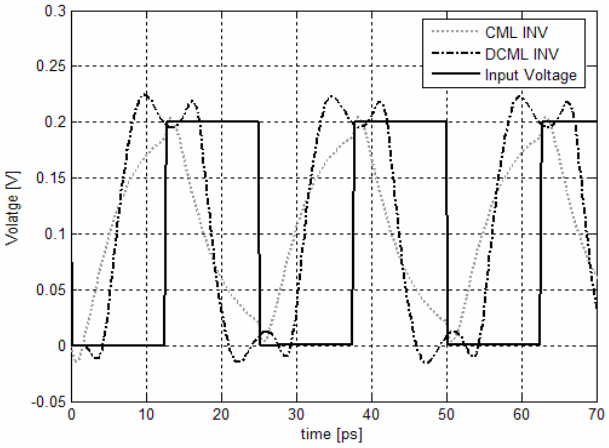

Fig. 6. CML Inverter and DCML Inverter simulation results.

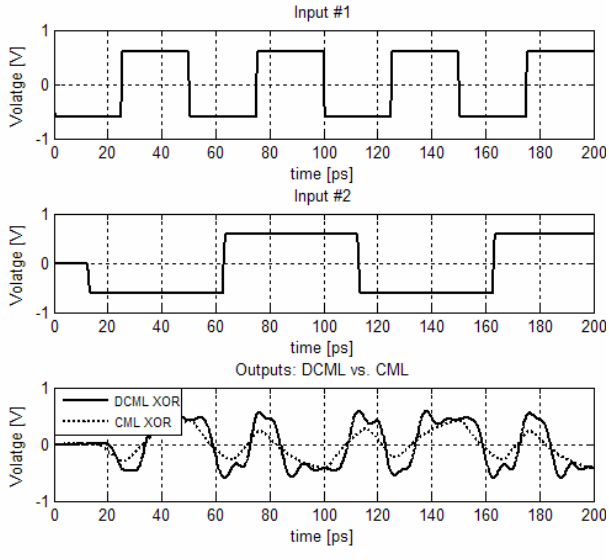

Fig. 7. CML XOR and DCML XOR simulation results.

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