A 3-10 GHz Low-Noise Amplifier for Ultra-Wideband Applications

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Abstract—This paper presents a new methodology for the design of low noise amplifiers for Ultra Wideband applications. Using the unwanted effect of the gate-drain capacitor of transistors on the input impedance to our benefit, the operation of the conventional narrowband LNA is extended to provide a very good input matching from 3 GHz to 10 GHz. Using a triple-resonance circuit as the drain impedance, a relatively flat gain is also achieved over the same operation band. A power gain of 8 dB, with good input and output matching(S_{11}< -14 dB and S_{22} < -14 dB) is achieved over a 3 to 10 GHz band in 0.13 µm CMOS technology.

***Index Terms*—low-noise amplifiers, ultra wideband, s-parameters.**

I. Introduction

Since the declassification of UWB technology in 2001, academia and industry have been eagerly working to develop the first UWB prototype. UWB transmitters do not modulate the signal with a career frequency like traditional narrowband technologies (WiFi, WiMAx, CDMA, etc) but instead transmit short pulses that represent the stream of a binary data, often at durations of less than one nanosecond. The UWB signal is compressed in time, and spread over a very wide bandwidth (3GHz to 10 GHz). UWB can transmit and receive wireless signals at rates in excess of several hundred of Mbits per second, while consuming a small amount of power without interfering with existing communications signals. UWB application is not limited to wireless; the technology is used for medical imaging, automotive radars, and security systems applications. The block diagram of a simple UWB receiver is shown in Fig. 1. According to FCC regulations depicted in Fig. 1, the emission power of UWB transmitters must be limited to very low values (less than -40 dB) in order not to interfere with other wireless devices operating under other wireless standards. Design of low-noise amplifiers (LNAs) for UWB applications is different from those of the narrowband wireless systems. The conventional LNA design usually exhibits an input matching in a very narrow band. In this paper, we present a novel approach for design that offers a good input match over the frequency band of 3 to 10 GHz, while not compromising the noise performance of the LNA

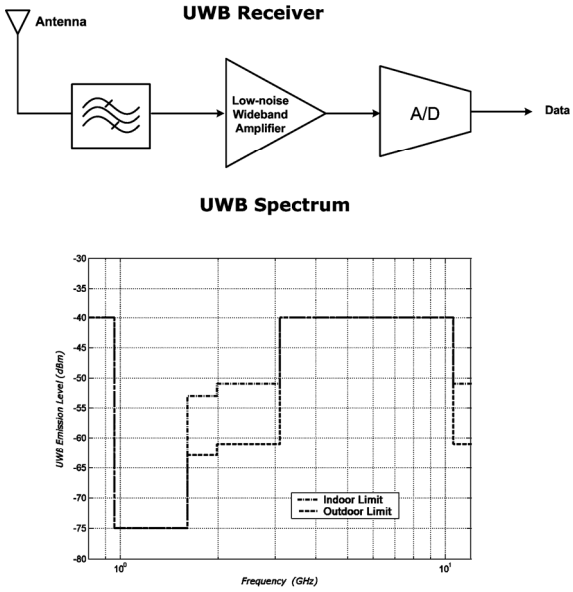

Fig.1. Block diagram of UWB receiver, and UWB emission level .

II. Conventional Narrowband LNA Design

Depicted in Fig. 2, conventional LNAs employs an inductor (L_S) at the source of the NMOS transistor to achieve both low noise performance and pure resistive input matching at a single frequency [1]. Based on a simple transistor model (consisting of the transistor's transconductance g_m and gate-source capacitor C_{gs}), the input impedance of the LNA can be expressed as:

$$Z_{in} = \frac{1}{jwC_{gs}} + jwL_S + \frac{g_m L_S}{C_{gs}} \qquad (1)$$

When designing CMOS LNAs, the size of the transistor is usually optimized for the best noise performance, which subsequently determines the values of g_m and C_{gs} in (1). Choosing an appropriate value for L_S, the real part of the input impedance can be matched to the output impedance of the antenna, i.e. 50 Ω. The imaginary part of the input impedance is equal to zero at the resonance frequency of L_S and C_{gs}. Note that the input matching is significantly deteriorated as the frequency of the operation slides off the resonance frequency.

Because the relatively small L_S (< 1nH for deep submicron CMOS technology) resonates with C_{gs} at relatively high frequencies, another inductor (L_G) is usually connected to the gate to bring the resonance frequency down to the range where most narrowband wireless applications are positioned. To bring down the resonance frequency to less than 3 GHz, a relatively large gate inductor is needed (several nHs). Because of the low quality factor of the on-chip inductors, a large inductor is accompanied by a large series resistor that can significantly worsen the noise performance of the amplifier. Placing an additional capacitor C_P in parallel to transistor C_{gs} will decrease the gate inductance needed for the same resonance frequency. After the addition of these components, equation (1) can be rewritten as follows:

$$Z_{in} = \frac{1}{jw(C_{gs}+C_P)} + jw(L_G+L_S) + \frac{g_m L_S}{C_{gs}+C_P} \quad (2)$$

This circuit topology is primary invented for narrowband applications. In the next section, we propose a modification to this circuit to broaden its operation band.

III. Ultra-Wideband LNA Design

A few new LNA designs are reported in the literature for Ultra Wideband applications [2][3]. The first work uses a resistive feedback to achieve a broadband input matching and a flat gain for the LNA. The second work uses an LC ladder to broaden the performance of the source-generated LNA. Both of these methods comprise the noise performance of the LNA to achieve a broadband input matching. The first method uses a resistive feedback that introduces extra noise in the circuit, while the second method adds several low-quality factor on-chip inductors at the gate of the transistor. The input impedance calculation for a narrowband LNA in the previous section was based on a simple transistor (g_m and C_{gs}) model, which no longer holds accurate for the large transistors optimized for the minimum noise figure. Therefore, bringing into account the effect of gate-drain capacitance (C_{gd}) to calculate the input impedance of the amplifier is necessary.

A. Effect of C_{gd} on Input Impedance

Considering the effect of C_{gd}, a parallel path is added to the input circuit. This path includes the C_{gd} in series with the impedance seen from the source terminal of the cascode transistor. If the gate-drain resistor of the cascode transistor is ignored, this impedance is equal to the parallel of C_{gs} and $1/g_m$. Since the symbolic analysis of the circuit results in a very complicated expression for the input impedance, the circuit is extensively simulated to evaluate the effect of each parameter on the input impedance. Fig. 3, 4, 5 and 6 depict the real and imaginary part of the input impedances as functions of C_P, W_{M1}, L_S, and W_{M2}, respectively. In each simulation, one circuit parameter is swept in the desired range while all other parameters are kept constant. Simulation results in Fig 3

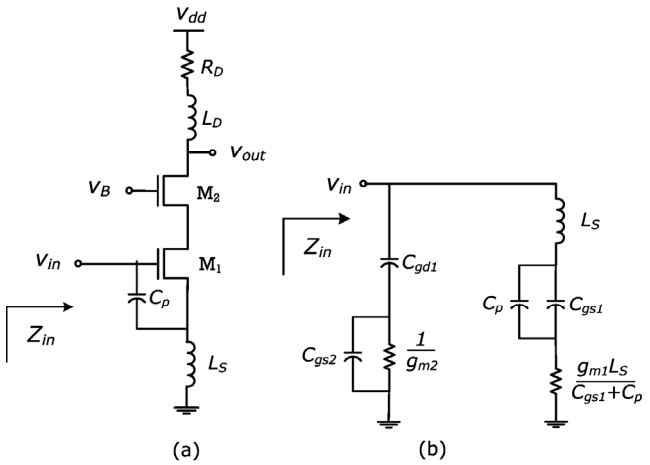

Fig. 2. (a) Schematic diagram of the source degenerated LNA, and (b) its equivalent input small-signal circuit.

indicate that the real part of the input impedance does not stay constant with the frequency for small values of C_P. This implies that matching the real part of the input impedance to a 50Ω resistor over a broad frequency range requires a large parallel capacitor (C_P). For large parallel capacitors, the imaginary part of the input impedance follows a specific pattern with respect to frequency: in the first phase, the imaginary part decreases in absolute values in reverse with frequency, where the two capacitors C_P+ C_{gs} determine the behavior of the input network. The second phase starts with an increase in the absolute value of the imaginary part and ends with a decline in the absolute values. In this phase, the gate-drain capacitor (C_{gd}) of the transistor plays an important role. In the third phase, the imaginary part of the input starts to increase (sign value), and approaches the electrical behavior of the inductor L_S after changing the polarity. This three-phase behavior of the imaginary part is also evident in other parametric simulations (Fig 4 to 6). As demonstrated in Fig. 4, for a particular value of C_P, there is a transistor size that provides the minimum variation of the real part of the input impedance with respect to frequency. The value of L_S determines the low-frequency response of the input impedance as shown in Fig 5. For a fully input matched design, the value of L_S is set such that a real impedance of 50Ω is achieved. Fig 6 illustrates the variations in input impedance as a function of cascode transistor size. Obviously for larger cascode transistors, the effect of C_{gd} becomes more evident as the impedance seen at the source of the cascode transistor decreases.

B. Proposed Input Matching Technique

To exploit the three-phase behavior of the imaginary part of the input impedance, a fully matched LNA can be designed by adding a relatively small inductor to the transistor gate. As the gate inductor (L_G) is placed in series with the input impedance of the LNA, the imaginary part pf the input impedance in the second phase is leveled at an absolute value close to zero. For a proper LNA design, an input impedance with a relatively constant real part and a close-to-zero imaginary part over a

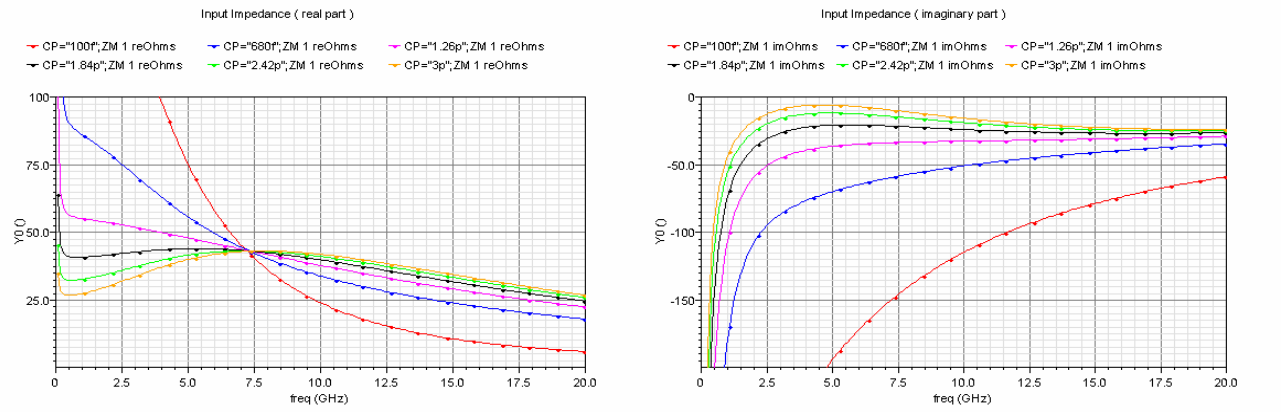

Fig. 3. Input Impedance of LNA as a function of C_P.

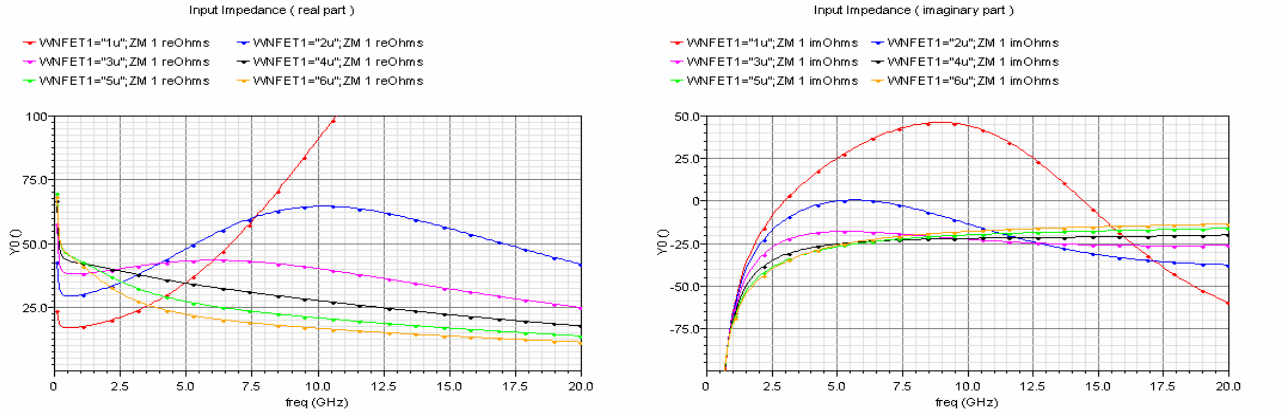

Fig. 4. Input Impedance of LNA as a function of M1 width (WNFET1).

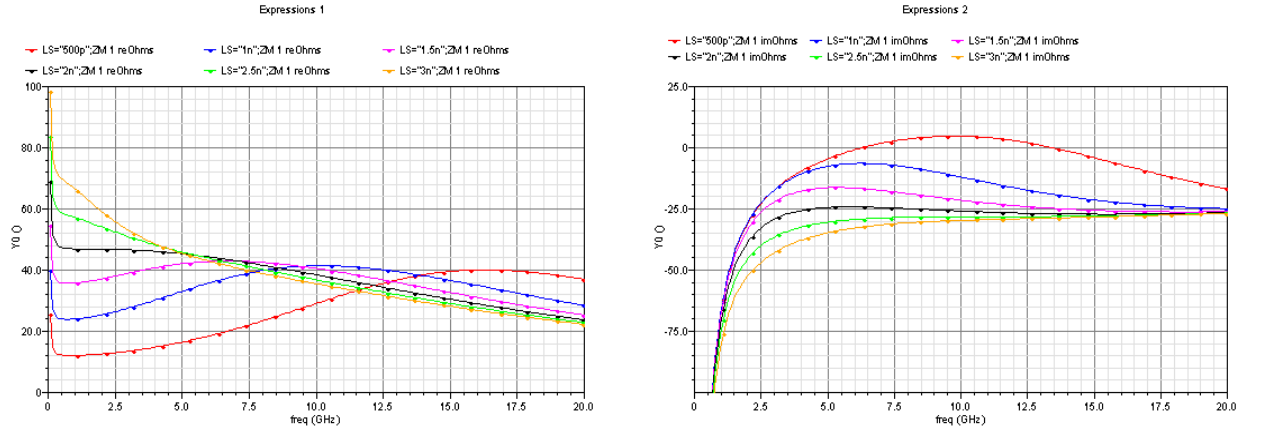

Fig. 5. Input Impedance of LNA as a function of L_S.

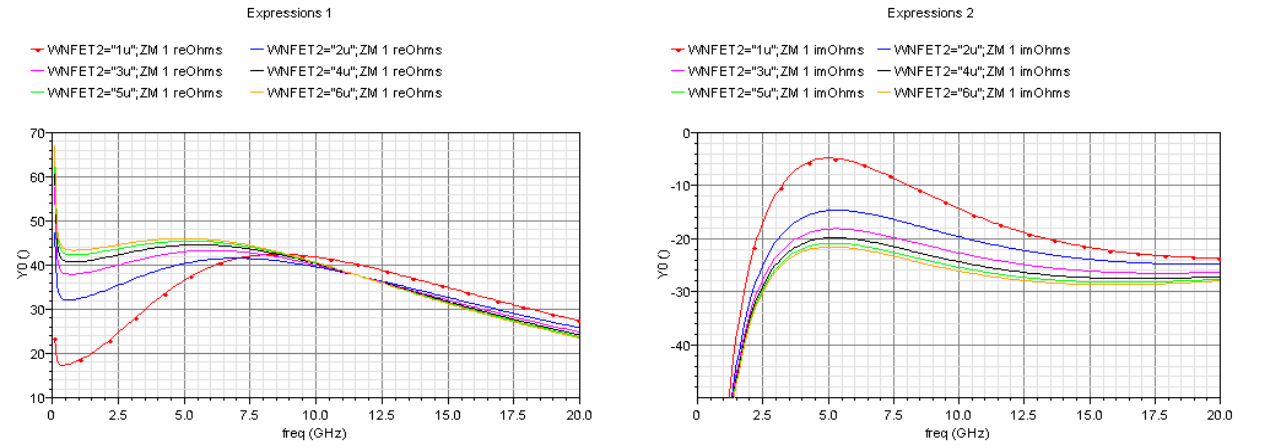

Fig. 6. Input Impedance of LNA as a function of M2 width (WNFET2).

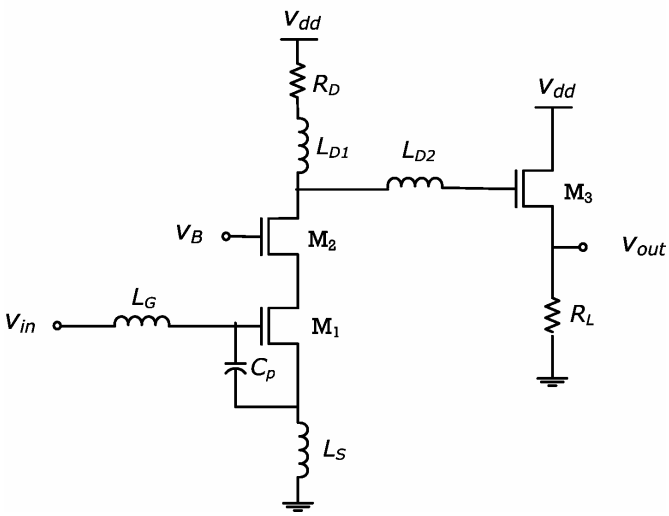

Fig. 7. Complete schematic diagram of LNA excluding biasing circuitry.

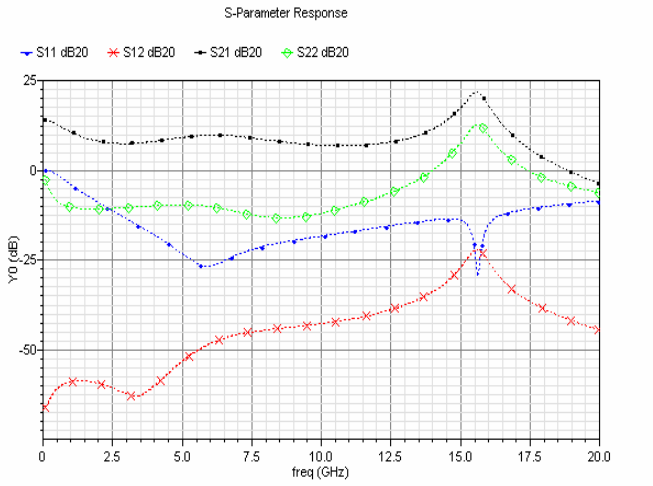

Fig. 8. Proposed UWB LNA S-Parameters

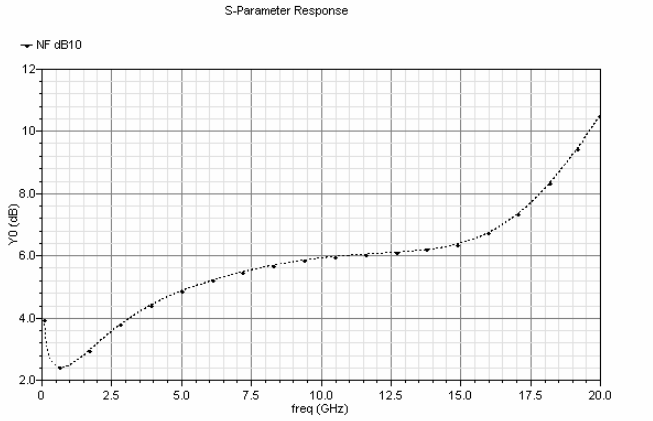

Fig. 9. Proposed LNA Noise Figure

broad frequency band is needed. This inductor is different from the gate inductor for narrowband design, which is devised to lower the resonance frequency. Because the proposed broadband matching can be achieved using a small size inductor (usually less than 500 pH), the noise performance of the LNA is not adversely affected.

C. Flat Gain

An inductive peaking technique [4] is usually employed in narrowband designs to compensate for LNA gain decline because of the source inductor. It is implemented by placing an inductor in series (L_D) with the drain resistor. This technique is not effective in this design, as a relatively large parallel capacitor (C_P= *2 pF*) is used. To achieve a flat gain over the 3-to-10 GHz band, a triple resonance circuit is used. This circuit is reported in [5] for broadband amplifiers in optical communications systems. The complete LNA circuit is illustrated in Fig 7. The LNA is simulated in a fully RF-characterized 0.13 µm CMOS technology. Optimized design parameters are listed in Table 1. S-parameter simulation results are demonstrated in Fig. 8. The maximum input and output return loss is 14 dB and 10 dB within a 3-to-10 GHz band, respectively. The average power gain of the LNA is 8 dB, while the reverse coupling is less than -40 dB in the band. The minimum noise figure is 4 dB, yet averaged at 5 dB for the entire band as depicted in Fig. 9.

IV. CONCLUSIONS

This paper has reported on the design of LNAs for UWB applications. The design employs a small inductor to compensate for the decline in the imaginary part of the LNA's input impedance to achieve a broadband input matching. The proposed UWB LNA is simulated in 0.13 µm CMOS technology achieving a power gain of 8 dB, and good input and output matching (S_{11}< -14 dB and S_{22} < -14 dB) over a 3 to 10 GHz band.

L_S	L_{D1}	L_{D2}	R_D	W_{M1}	W_{M2}	*WM3*	C_P
1.6 nH	3 nH	3 nH	100	*150* µm	150 µm	50 µm	2 pF

Table 1. Final Design Parameters

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