A Novel Loss Compensation Technique for Broadband CMOS Distributed Amplifiers

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***Abstract*—This paper presents a novel loss compensation technique, an active negative resistor produced by a capacitively source degenerated configuration, to improve the gain flatness and bandwidth of CMOS distributed amplifiers (DAs). This configuration provides the desired isolation from the transmission line at lower frequencies, and a frequency-increasing negative conductance that can fully compensate for the loss of the on-chip inductor over a broad frequency band. A 40 GHZ three-stage 0.13 μm CMOS DA is devised that outperforms previously published CMOS DAs by providing a large gain-bandwidth product of 200 GHz-dB with an improved gain-flatness of ±0.2 dB. The proposed loss compensated DA dissipates 24 mW from a 1.2 V DC supply.**

I. INTRODUCTION

Broadband amplifiers are the fundamental building blocks of high data-rate wireline and wireless telecommunication systems. Distributed amplification is considered a preferred circuit topology for broadband amplification [1] because of its unique advantage of having the input and output matching networks embedded in its circuit structure, whereas other techniques, like inductive or capacitive peaking, require additional circuitry to satisfy the matching conditions. CMOS technology has recently become the technology of choice for the implementation of high speed broadband communication circuits because of the significant improvement of transistors' intrinsic speed owing to the technology's aggressive scaling [2]. Offering N-channel devices with cutoff frequencies up to 100 GHz, submicron CMOS technology has lower fabrication costs than conventional high speed semiconductor technologies (GaAs, SiGe, InP, and GaN). In addition, CMOS technology enables the integration of all analog and digital building blocks of broadband transceivers on a single chip (system-on-a-chip), reducing the overall cost of the systems even further. Several successful implementations of CMOS DAs are reported in the literature [3-8]. These designs are distinguished from each other by different on-chip inductor implementations in CMOS process and gain cell circuit topologies.

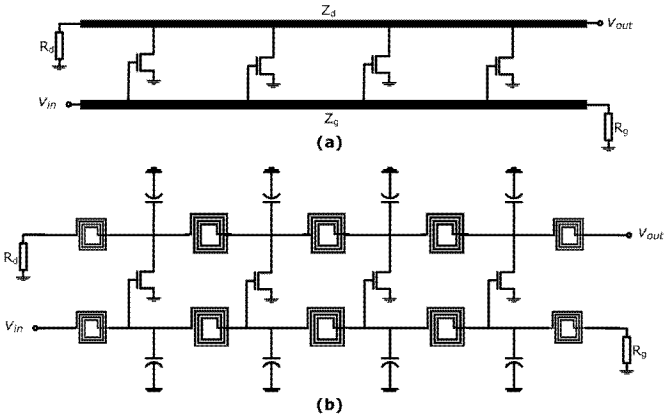

Fig. 1. Schematic diagram of (a) microwave DAs, and (b) CMOS DAs incorporating on-chip square spiral inductors.

Ideally, lossless DAs provide a flat gain over their bandwidth. Taking into the account the loss of on-chip inductors, the bandwidth and the gain of DAs are deviated from the ideal conditions. This paper presents a novel loss compensated DA design that uses negative resistors to compensate for the resistive loss of the on-chip spiral inductors.

II. DISTRIBUTED AMPLIFIER DESIGN

Conventional microwave DAs are constructed of two TLs that connect the drain and gate terminals of several field-effect transistors (FETs), as depicted in Fig 1(a). Since CMOS interconnects with typical length – less than a few hundred μms – are not considered to be TLs at frequencies up to 40 GHz, the TLs are artificially constructed of a ladder of lumped-element inductors and capacitors, as portrayed in Fig 1(b). The intrinsic capacitors of transistors – the main cause of bandwidth limitation – are separated by series on-chip inductors to form a lowpass filter topology. This structure provides a relatively low gain due to the additive nature of its paralleled gain cell, but achieves wideband amplification due to distribution of the parasitic capacitors

in a lowpass LC circuit topology. The main drawback of DA topology is its large die area because it incorporates several area-consuming spiral on-chip inductors.

A. Transmission Line Design of a DA

The fist step in the design of a distributed amplifier is to find the values of the capacitors and inductors of the gate and drain transmission lines. The bandwidths of the gate and drain transmission lines are given by

$$BW_{gate} = \frac{2}{\sqrt{L_g C_g}} \quad and \quad BW_{drain} = \frac{2}{\sqrt{L_d C_d}}. \quad (1)$$

where L_g, L_d, C_g, and C_d are the inductor and capacitor of the gate and drain transmission lines. The characteristic impedance of the gate and drain transmission lines are obtained using

$$Z_{gate} = \sqrt{\frac{L_g}{C_g}} \quad and \quad Z_{drain} = \sqrt{\frac{L_d}{C_d}}. \quad (2)$$

To ensure proper matching at input/output ports, the characteristics impedance of the gate and drain transmission lines, Z_{gate} and Z_{drain}, must be chosen equal to or close to the terminating resistors of the lines, R_g and R_d, respectively. Since a proper DA design requires equal signal delays on the gate and drain transmission lines, the gate and drain transmission lines' bandwidths are required to be equal. If the input and output ports are terminated with the same resistors, then this condition necessitates that the values of the inductors of capacitors of both lines be equal, that is L_g=L_d and C_g=C_d. Note that C_g and C_d are the total capacitance seen from the corresponding nodes of the circuit, including the parasitic capacitors of the transistors and on-chip inductors. Therefore, the parasitic capacitors set the minimum values of C_g and C_d and, consequently, the maximum achievable bandwidth of the transmission lines.

B. Lossy Transmission Lines

A lossless LC transmission line terminated in its image impedance transmits total incident power from its input to the load within its bandwidth and blocks the incident power outside the band. If the transmission line is terminated in its characteristic impedance in the vicinity of the cutoff frequency, the matching condition of the transmission line is significantly impaired. An m-derived section can be placed at both the input and output port of the transmission line to improve the matching condition. If the loss of the transmission line's components, especially on-chip inductors, is taken into account, the power gain of the transmission line is reduced. Since the resistive loss of the on-chip inductors increases with the frequency, the power gain no longer remains constant within the DA's band. In addition, series resistors of the inductors reduce the bias voltage as the transistor is placed further from the DC supply. In the next section we present a novel loss compensation technique to compensate for the resistive loss of the transmission lines and provide a flat gain over all the bandwidth.

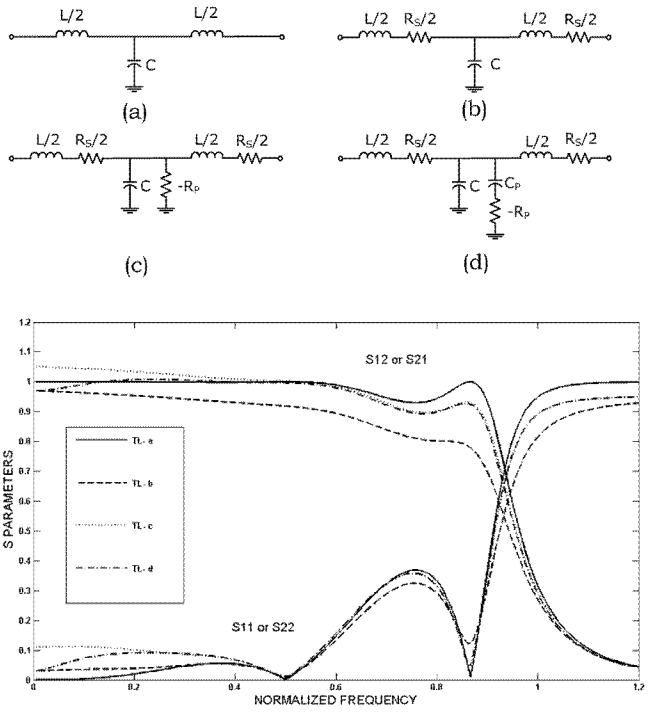

Fig. 2. Schematic diagrams of (a) ideal LC transmission line, (b) lossy LC transmission line compensated with parallel negative resistors (R_P), and (c) lossy LC transmission line compensated with parallel high-pass negative resistors (R_P), and their simulated S parameters.

III. Compensation Technique

A. Attenuation Compensation of Lossy Transmission Lines

Because of the low quality factor of the CMOS on-chip inductors, artificial transmission lines attenuate the signal as it travels through the gate and drain transmission line. The loss of on-chip inductor increases with frequency, reducing the gain of the amplifier as the frequency increases. Negative resistors are extensively used to compensate for the resistive loss so as to improve the quality factor of inductors. Fig. 2(a) shows an ideal LC transmission line terminated in its characteristic impedance. Bringing into the picture the series resistor of the on-chip inductors, the transmission line is redrawn in Fig. 2(b). Shunt negative resistors are incorporated in the circuit to compensate for the transmission line's loss, as portrayed in Fig. 2(c). Note that for a lossless transmission line, the propagation constant is purely imaginary ($\gamma = \alpha + j\beta = jw\sqrt{LC}$); therefore the attenuation constant (α) is zero as expected. To find the value of the negative resistance required to fully compensate the attenuation of the transmission lines, we use the basic transmission line theory to calculate the propagation constant of lossy transmission lines with attenuation compensation networks (-G) as follows:

$$\gamma = \alpha + j\beta = \sqrt{(R + jwL)(-G + jwC)} = \sqrt{-(RG + w^2 LC) + jw(RC - LG)}. \quad (3)$$

To make the attenuation constant of the compensated transmission line equal to zero, the propagation constant must be purely imaginary, requiring in turn that the imaginary term inside the square root in (3) be equal to zero; therefore the values of the negative shunt conductance can be obtained as

$$G = \frac{RC}{L}. \tag{4}$$

On the other hand, the characteristic impedance of the transmission line is also affected by the series resistor and shunt negative conductance as follows:

$$Z = \sqrt{\frac{(R + jwL)}{(-G + jwC)}} \tag{5}$$

For a fully compensated transmission line, the characteristic impedance can further be simplified to:

$$Z = \sqrt{\frac{(R + jwL)}{(-R + jwL)}} \times \sqrt{\frac{L}{C}}, \tag{6}$$

where $\sqrt{L/C}$ is the characteristic impedance of a lossless transmission line. At low frequencies, the characteristic impedance of the loss compensated transmission line is different from that of a lossless transmission line, leading to some variation in the gain of the amplifier. Though at higher frequencies, the value of the characteristic impedances is approaching that of lossless line. In this study, we propose that the compensating negative resistor be isolated from the transmission line by a series capacitor, depicted in Fig. 2(d), a configuration that can lead to the following improvements in the operation of the circuit:

- Negative resistance circuit does not affect the DC biasing of the circuit since it does not draw any DC current that passes through the transmission line components.
- Negative resistance circuit does not change the characteristic impedance of the transmission lines at lower frequencies, and, therefore, there will no gain variation at low frequencies.
- Negative resistance is present only in the circuit at relatively higher frequencies when the effect of a series resistor on the gain of the DA is more evident and can be fully compensated.

B. Negative Resistnace Implementation

The negative resistors can be implemented using transistors and passive components in CMOS technology. Three negative resistor circuits and their equivalent small signal circuits are depicted in Fig. 3. The negative resistance can be implemented using a capacitively source degenerated configuration, Fig. 3(a). If the transistor model includes only the transistor's transconductance (g_m) and the gate-source capacitor (C_{gs}), the equivalent circuit of a common gate transistor with an inductor in its gate is a frequency-dependent negative resistor in parallel to a frequency-

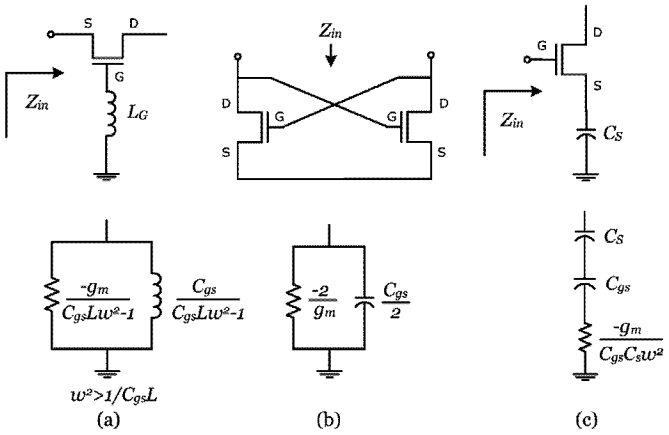

Fig. 3. Schematic diagrams of three negative circuits and their equivalent small signal input impedance of (a) a common gate configuration with inductor connected to gate, (b) cross coupled pair, and (c) capacitvely degenerated common source configuration.

dependent inductor, as shown in Fig. 3(a). Although this circuit topology is employed for loss compensation of the transmission lines [10], it fails to provide isolation for the transmission line at lower frequencies. This circuit also occupies a larger die area than the two other negative resistor circuits because it incorporates an on-chip inductor. The second circuit, depicted in Fig. 3(b), is a cross-coupled differential pair. The cross-coupled transistors produce a negative resistor of a value of $-2/g_m$ in parallel to a capacitor of $C_{gs}/2$. The cross-coupled negative resistor circuit is commonly used in circuits operating in differential mode. The cross-coupled differential pair is extensively used to improve the quality factor in differential LC-tank VCOs. The third negative resistor circuit is a capacitvely source degenerated circuit. The input impedance seen from the gate of the transistor is equivalent to a negative resistor with a value of $-g_m / w^2 C_s C_{gs}$ in series with two series capacitors, C_{gs} and C_s [9]. The configuration is highly favorable to allowing the shunt conductance of the negative resistor to increase with frequency because the resistor loss of on-chip inductors behaves similarly with respect to the frequency; therefore, the loss of on-chip inductors can be compensated for a wide frequency range. Among the three negative resistor circuits presented, the capacitively source degenerated amplifier provides the favorable configuration needed for effective compensation of transmission line losses – that is a negative resistor in series with a capacitor. Since C_s blocks the DC current, it is necessary to parallel a resistor to this capacitor in order to provide the DC path required for biasing the common source transistor. The value of the biasing resistor must be several times larger than the impedance of C_s, and small enough to provide the DC current needed for producing the required g_m for compensating the loss of transmission lines at those frequencies in which the negative circuits effectively compensate for the loss of on-chip inductors.

IV. 40 GHz DA Design and Simulation Results

This section presents a summary of the design of a 40 GHz DA in 0.13µm IBM's CMRF8SF CMOS process. CMRF8SF is a fully RF-characterized CMOS technology in which reliable RF models for active and passive components are provided, and accompanied by their equivalent chip layout. Therefore, the simulation results in this environment carry a significant accuracy in the GHz frequency range – unlike the simulation result in a digital CMOS process. To achieve a bandwidth of 40 GHz and a characteristic impedance of 50 Ω simultaneously, the value of inductors and capacitors of the gate and drain transmission lines are computed as 398 *pH* and 159 *fF*, respectively. As discussed earlier, an m-derived network is required at both ends of the transmission lines to improve the matching at the vicinity of the cutoff-frequency. The sum of the parasitic capacitors of transistors and on-chip inductors and additional capacitors at each node of the transmission line should not exceed the calculated value of 159 fF. This condition limits the maximum achievable gain of the amplifier. In order to reduce the capacitive coupling, a cascode configuration is selected for the gain cells. Replacing the on-chi inductor models, the magnitude of the gain (S_{21}) of the DA is reduced as frequency increases, as shown in Fig 4 (dashed lines). To compensate for the reduction in the gain due to the loss of the on-chi inductors, a capacitively source degenerated configuration is selected, as explained in the previous section. An optimization process is employed to find the optimum value for achieving a maximally flat gain for the DA. The final S parameters of the compensated DA are depicted in Fig 4 (solid lines). Both the gain flatness and phase linearity of the amplifier are significantly improved for the loss compensated network.

V. Conclusions

In this paper a novel loss compensation technique is presented that improves considerably the gain flatness and phase linearity of CMOS DAs. It has been proven that a capacitvely source degenerated topology is the most appropriate choice for a negative resistor. A 40 GHz 0.13µm CMOS DA is designed that achieves a gain of 5 dB with a gain variation less than 0.5 dB. As summarized in Table 1, the proposed DA achieves the largest gain-bandwidth product so far among the reported CMOS DAs.

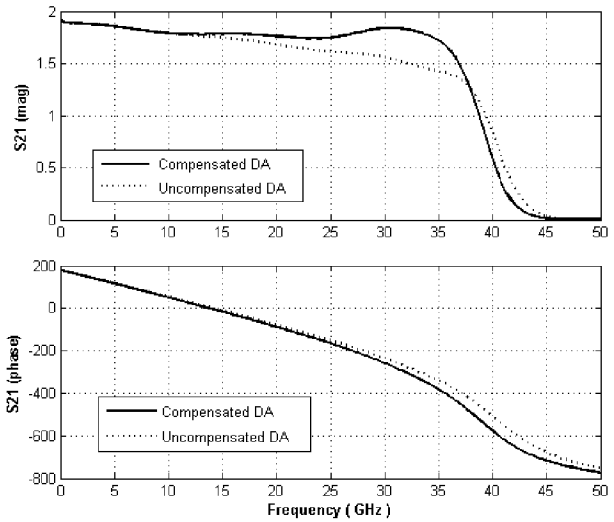

Fig. 4. Magnitude and phase of the gain of lossy CMOS DA (dashed lines) and loss compensated DA (solid lines).

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Table 1. Previously Published CMOS DAs versus the proposed DA.

CMOS Technology Feature Size (µm) & [Reference]	Unity Gain Bandwidth (GHz)	Average Gain (dB)	Power Dissipation (mW)
0.8 [3]	4.7	5±1.2	54
0.6 [4]	5.5	6.5±1.2	83
0.6 [5]	8.5	5.5±1.5	216
0.35 [6]	5.5	20±2.5	86.7
0.18 [7]	15	8±1	-
0.18 [8]	24	7.3±0.8	52
0.18 [This work - conventional DA]	38	5±0.2	15
0.18 [This work – Loss Compensated DA]	38	3.9±1.3	24