A 10-GHz 15-dB Four-Stage Distributed Amplifier in 0.18 µm CMOS Process

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Abstract

This paper presents a four-stage CMOS distributed amplifier (DA) design implemented in standard 0.18 µm CMOS technology. The proposed design eliminates the need for transmission line capacitors and, consequently, uses significantly smaller spiral inductors compared with the previous designs. Using the minimum size inductor, the bandwidth of the amplifiers is extended, and the quality factors of the on-chip inductor are improved. Proposed DA occupies the smallest die area (0.3µm*0.8µm) amongst the DAs reported with the same performance. A unity gain bandwidth of 10 GHz and a gain of 15 dB are measured. DC power dissipation is 56 mW.

1 Introduction

CMOS technology has been adopted recently for the implementation of high speed broadband communication circuits [1]. High performance deep submicron CMOS technology enables the integration of broadband telecommunication transceivers on a single chip (system-on-a-chip). While offering N-channel devices with cutoff frequencies up to 100 GHz, submicron CMOS technology is a low-cost technology compared with other high-speed semiconductor technologies (GaAs, SiGe, InP, GaN, and others). Broadband preamplifier or amplifiers are the vital building blocks of broadband wireline/wireless receivers and transmitters. The designing of broadband amplifiers seems to be the first step toward the integration of broadband transceivers on a CMOS chip. Distributed amplification and inductive peaking are the most commonly used techniques for broadband amplification [3]. The unique advantage of DAs is that they provide the matching network embedded in the amplification network, while other techniques require additional circuitry to satisfy the matching conditions. The main disadvantage of DAs is the large area of DAs, because they include several on-chip inductors. This paper presents a DA design approach that uses the smallest inductor values to achieve the required performance and, consequently, minimizes the die area of the DA significantly. In addition, a fast optimization process is described to accelerate the design of CMOS DAs.

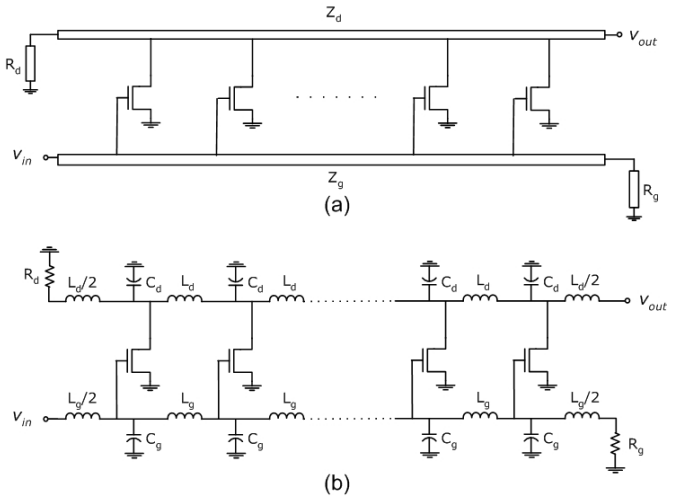

Fig. 1. (a) Schematic diagram of microwave DAs, and (b) schematic diagram of CMOS DAs implemented using artificial transmission lines (LC network).

2 CMOS Distributed Amplification

Distributed amplifiers (DAs) are constructed of two transmission lines that connect the drain and gate terminals of several field effect transistors (FETs) as depicted in Fig 1(a). The intrinsic capacitors of transistors – the main cause of bandwidth limitation – are absorbed into the transmission lines, reducing the characteristics impedance but not the bandwidth of transmission line. Since interconnects with typical length – less than a few hundred µms – are not considered transmission lines at frequencies up to 30 GHz, the transmission lines are artificially constructed of a ladder of lumped-element inductors and capacitors. Therefore, the analysis and design of CMOS DAs differ from those of conventional microwave DAs. Several successful implementations of CMOS DAs are reported in the literature [5-11]. These designs are distinguished from each other through

I. Different implementation of on-chip inductors in CMOS technology, such as square spiral inductors, bond wire inductors, or coplanar waveguides.

II. Different circuit topology for each gain cell, such as common-source, cascode, or differential amplifiers.

To prove the feasibility of implementing the new design, simple common-source amplifiers are used for the gain cells, and on-chip inductors are implemented on the top metal layer in the form of square spiral with no ground shield.

3 CMOS DA Design

This section presents a new approach for the design of broadband CMOS DAs. Since the transmission lines in CMOS technology are artificially constructed of a limited number of inductors and capacitors (see Fig. 1(b)), they do not provide an unlimited bandwidth by acting like a periodical lowpass LC filter. Therefore, the maximum bandwidth of a DA is limited to the cutoff frequencies of artificial gate and drain transmission lines [14]:

$$BW_{\max} \le \min\left(\sqrt{\frac{1}{L_g C_g}}, \sqrt{\frac{1}{L_d C_d}}\right) \quad (1)$$

where L and C are the values of the inductors and capacitors of the artificial transmission lines. In practice, the bandwidth is further limited by the resistive loss of transmission lines and by the output resistance of the amplifier cell gains [2]. Since transmission lines are constructed of a ladder of inductors and capacitors in CMOS technology, designers can take advantage of setting the elements' values individually and independently from other circuit elements – unlike for microstrip lines. To increase the bandwidth of the distributed amplifiers, either the inductance or the capacitance of the artificial transmission line shall be decreased. But if the inductors' values are decreased, the characteristic impedance of the transmission line, $(L/C)^{1/2}$, and, consequently, the value of the matching load at the end of the lines are also reduced. Since the power gain of a lossless DA is quadratically proportional to the transconductance of the transistors (g_m), the load impedance of the transmission lines (Z_L) and the number of DA stages (N) according to [3]

$$G = \frac{1}{4} g_m^2 Z_L^2 N^2 \quad (2)$$

The voltage gain of an amplifier is equal to the square root of the power gain if the input/output ports are perfectly matched. Therefore, a reduction in the matching load of the amplifier decreases the voltage gain of the DA linearly. Reducing the inductance of artificial transmission lines does not appear to be the best option because it also reduces the gain of the amplifier and does not lead to a product improvement in bandwidth-gain. The other design alternative is to decrease the capacitance of the transmission lines. The lowest possible values for transmission lines capacitance are limited to the sum of the parasitic capacitance of MOSFETs and on-chip inductors if the additional capacitors of the artificial transmission lines are set to zero ($C_d=0$ and $C_g=0$). Fig 2 shows that the bandwidth of an LC ladder network increases as L and C decrease proportionally to maintain the characteristics impedance of the artificial transmission line constant, as well as preserve the matching condition of the amplifier.

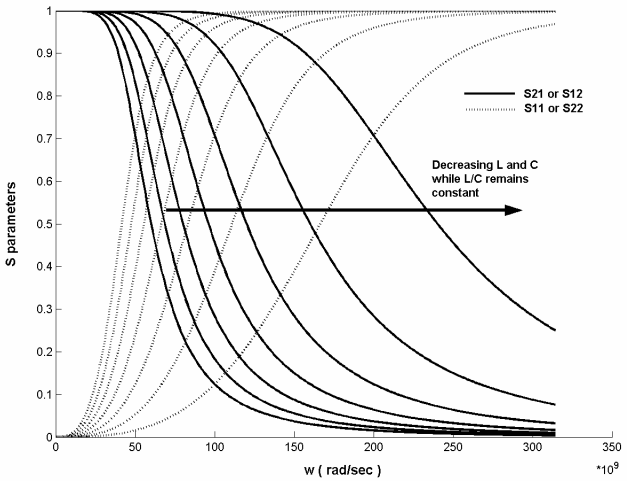

Fig. 2. S-parameters of LC artificial transmission line as L and C decrease proportionally.

4 On-Chip Inductors Optimization

The design and optimization of on-chip inductors is the most critical part of the DA design. On-chip inductors are usually made in the form of a square spiral on the top metal layer available in the technology. The design of a spiral inductor consists of finding the geometry of the spiral inductor, including number of turns (N), outer diameter of the spiral (d_{out}), metal width (w), and metal spacing (s) as shown in Fig. 3(a). The spiral inductors need to be modeled by solving Maxwell's electromagnetic (EM) equations in a three dimensional environment. As an example, ASITIC software is

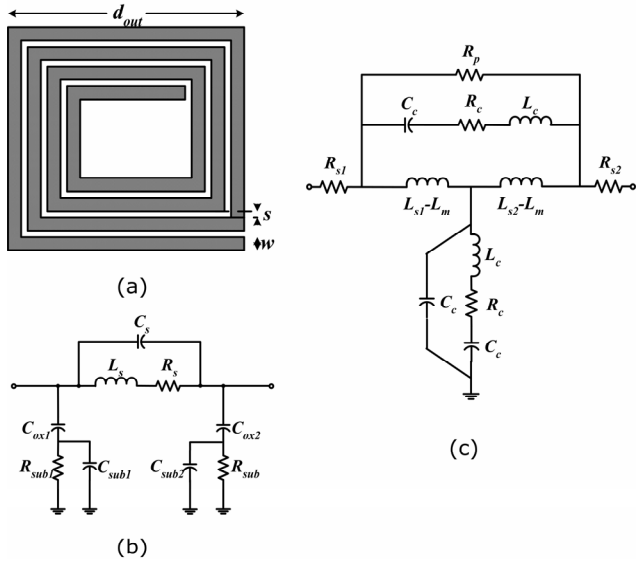

Fig. 3. (a) An on-chip square spiral inductor layout in CMOS technology, (b) equivalent narrowband circuit of the on-chip square spiral inductors, and (c) equivalent broadband circuit of the on-chip square spiral inductors [13].

an EM simulator specifically customized for the simulation, design and optimization of inductors on silicon substrate [12]. A π (pi) equivalent circuit of on-chip inductors is shown in Fig. 3 (b). The π (pi) model is accurate only for a single frequency. One way to obtain a broadband inductor model is to extract with EM simulators the elements of the π model as functions of frequency. However, EM simulation of inductors over a large frequency band is computationally extensive. Researchers have also developed a lumped-element model that can predict the inductor behavior over a large frequency band [13]. In this model, shown in Fig. 3(c), the equivalent circuit elements' values are no longer functions of frequency. Layouts of the inductors are determined though an optimization process. The simplest optimization process is to use the EM simulator engine in every optimization's iteration. In this case, the optimization process takes an extremely long time, and may never converge at reasonable time periods. To accelerate the optimization process, it is divided into two consecutive processes shown in Fig 4. The first process uses a previously prepared lumped-element inductor model library for optimization. The model for inductor values, which are not in the library, is obtained through linear interpolation. Since there is no EM simulation, the first process rapidly converges to the local minimum (optimum values for inductors) based on the interpolated models. The second process is initialized at the final optimum values of the first process, and continues the process of optimization using an EM simulator. Since the initial value is close to the real optimum, the second process converges within a few iterations. If the goal of the optimization is to achieve a 10 GHz unity-gain bandwidth while maintaining a maximum amount of gain flatness, the first optimization engine, initiated at points $L_d = 1000\ pH$ and $L_g = 500\ pH$, converges at $L_d = 245\ pH$ and $L_g = 142\ pH$. A graphical representation of optimization process is shown in Fig. 5.

Since relatively small inductors (< 1nH) are used, it is important to realize that interconnects connecting inductors may introduce some additional inductances that cannot be neglected compared with those of spiral inductors. To use minimum length interconnection between the inductors, the inductors with the turn number of 1.75, 2.75, 3.75, … are preferred. Since the inductors with a lower number of turns exhibit lower series resistance, the number of turn is selected to be 1.75. The metal width is 10 μm and the metal spacing is 2 μm. The channel length of NMOS transistors is set at the minimum feature length of the technology, that is, 0.18 μm. However, the minimum channel length introduces the minimum output resistance for the NMOS transistor, and it is not appropriate for high gain designs; but since the output resistance of the transistor is still several times larger than the characteristic impedance of the gate and drain transmission, this choice does not affect the performance of the DA significantly. For transistor modeling, the RF extensions to BSIM3 models are used.

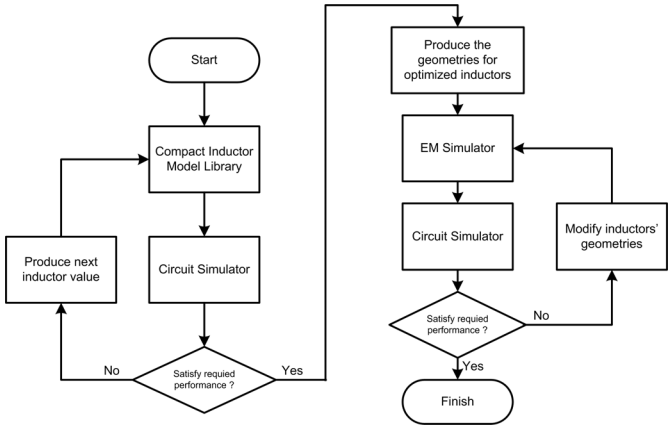

Fig.4. Optimization process flow chart.

Measurement and discussion

The DA circuit is layed out in an area of 400 μm * 800 μm, and fabricated in a standard 0.18 μm CMOS technology with six metal layers. On-chip inductors are implemented on metal 6 layer with thick metal option that extends the metal thickness to 2 μm. A die photograph of a fabricated chip is shown in Fig. 6. The amplifier input and output ports are probed on a wafer using GSG RF probes with a pitch of 150 μm. The S-parameters of amplifiers are measured using an Agilent® 8722ES Network Analyzer. The DC bias voltages (1.8V DC, 1 V DC) are supplied through the RF probes. The S-parameter measurement results are shown in Fig 7. The measured gain (S_{21}) of the amplifier is 15 dB, with a perfect uniformity all over the 10 GHZ bandwidth. Measured values of S_{11}, S_{22} and S_{12} are limited to -7 dB, -7 dB and -20 dB, respectively. These values indicate that the desired matching at input and output ports is achieved and that the reverse coupling of the amplifier is limited. Noise figure does not exceed 4 dB all over the bandwidth. Table 1 compares the performance of

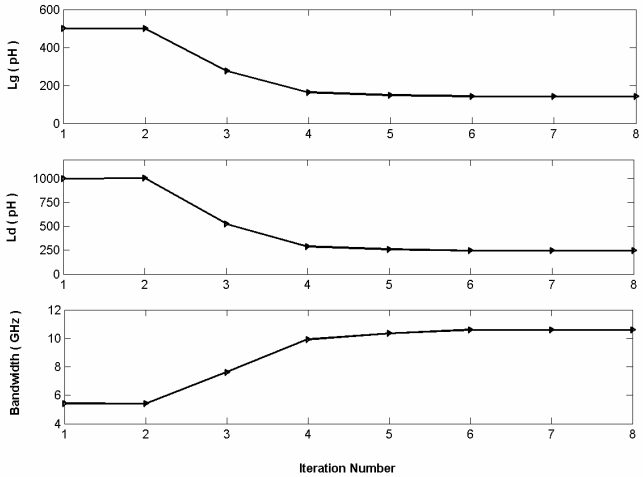

Fig 5. Optimization iterations.

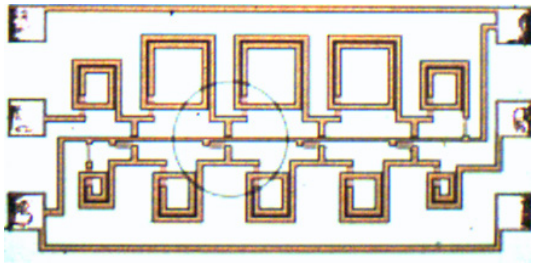

Fig.6. Die Photograph the four-stage CMOS DA in 0.18 µm CMOS technology with six metal layers.

previous DAs with that in this work. The results prove that the ratio of gain-bandwidth product to die area for this work is several times greater than the ratios published for other DA works.

5 Conclusions

A new approach for design and optimization of CMOS DAs is presented. The prposed method results in the design of a four-stage DA in 0.18 µm CMOS technology, with a gain of 15 dB over a bandwidth of 10 GHz. This design requires smaller inductors than those described in pervious research, leading not only to reduced chip area but also to improved quality factor of the inductors. If gain*bandwidth/area is defined as a quality measure of DA design, then this work improves the state-of-the-art of DAs by a factor of 3.57. Based on its performance, this broadband amplifier can be used in 10Gbps OC-192 optical receivers or UWB receivers operating in the frequency range 3 to 9 GHz.

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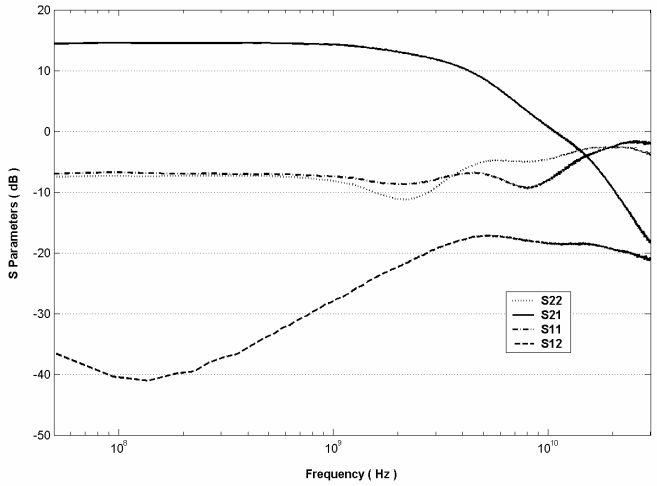

Fig. 7. Measured S-parameter of the proposed four-stage CMOS DA.

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Table 1. Comparison of DA performance for published works.

CMOS Technology Feature Size & Ref	Unity Gain Bandwidth (GHz)	Gain (dB)	P_{DC} (mW)	Area (mm^2)	Gain-Bandwidth Product (dB·GHz)	Gain-Bandwidth Product Area (normalized)
0.8 µm CMOS[9]	4.7	5	54	0.32*0.72	23.5	22%
0.6 µm CMOS [7]	5.5	6.5	83.4	1.4*0.8	35.75	7%
0.6 µm CMOS [6]	8.5	5.5	216	1.3*2.2	46.75	3%
0.35 µm CMOS [11]	5.5	20	86.7	0.95*1.8	110	14%
0.18 µm CMOS [5]	>11	18	54	1*2.2	198	19%
0.18 µm CMOS[10]	15	8	-	1.3*1.8	120	11%
0.18 µm CMOS [8]	24	7.3	52	0.9*1.5	175.2	28%
0.18 µm CMOS [this work]	10	15	56	0.4*0.8	150	100%

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