**Abstract**

- In this paper, a deep belief network is proposed based on stochastic computational methods.
- An approximate SC activation unit (A-SCAU) is proposed to implement different types of activation functions such as the sigmoid, the rectifier linear and the pure line functions.
- The design achieves a smaller area, lower power and energy consumption with a similar accuracy and speed compared to conventional binary implementations.

**Introduction**

Deep belief network (DBN)

A DBN consists of one input layer, multiple hidden layers and one output layer [1].

![Fig. 1. The structure of a DBN.](image)

Multiple activation functions are utilized for different training requirements.

\[ \varphi(x) = \frac{1}{1 + e^{p(-x)}}, \ \text{sigmoid} \]
\[ \varphi(x) = \min(1, \max(0, x)), \ \text{rectifier} \]
\[ \varphi(x) = \min(1, \max(-1, x)), \ \text{pure line} \]

**Stochastic computing**

- In SC, values are encoded by stochastic bit streams.
- Some fundamental computational elements can be implemented by simple circuits [2].

![Fig. 1. A bipolar stochastic multiplier, representing (a) The sigmoid function](image)

- SC achieves significantly smaller area cost and lower power consumption compared to conventional binary designs.
- SC designs require higher latency and large numbers of RNGs, thus may result in higher energy consumption.

**A-SCAU design**

- A-SCAU consists of an APC, a linear approximation unit (LAU), an RNG and a comparator.

![Fig. 5. Design of the A-SCAU.](image)

- The LAU is the core of the A-SCAU, based on binary algorithms, implementing multiple activation functions.

**Accuracy and hardware efficiency**

**Accuracy comparison**

<table>
<thead>
<tr>
<th>Network</th>
<th>Sequence length (bit)</th>
<th>Accuracy (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SC-DBN</td>
<td>128</td>
<td>98.90</td>
</tr>
<tr>
<td>(16 parallelization)</td>
<td>256</td>
<td>99.15</td>
</tr>
<tr>
<td>8-bit fixed point</td>
<td>-</td>
<td>98.10</td>
</tr>
<tr>
<td>32-bit floating point</td>
<td>-</td>
<td>99.27</td>
</tr>
<tr>
<td>Integral stochastic NN [4]</td>
<td>64</td>
<td>97.73</td>
</tr>
<tr>
<td>SC DNN [3]</td>
<td>1024</td>
<td>97.59</td>
</tr>
<tr>
<td>FPGA-RBM [5]</td>
<td>1024</td>
<td>94.28</td>
</tr>
<tr>
<td>FPGA-DBN [6]</td>
<td>4096</td>
<td>94.10</td>
</tr>
</tbody>
</table>

**RNG sharing comparison**

- The SC-DBN achieves high RNG sharing rate, thus significantly reduce the area and energy consumption of the RNGs.
- The proposed design takes 5.27%, 4.49% and 3.31% of the area, power and energy consumption of the 32-bit floating-point design; 26.55%, 27.82% and 29.89% of the 8-bit fixed-point design, with similar accuracy and computation speed.

**Energy efficiency comparison**

<table>
<thead>
<tr>
<th></th>
<th>SC-DBN</th>
<th>Fixed (8 bits)</th>
<th>Floating (32 bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>area (um²)</td>
<td>23062.61</td>
<td>86875.05</td>
<td>437767.22</td>
</tr>
<tr>
<td>power (mW)</td>
<td>1.12</td>
<td>4.01</td>
<td>24.86</td>
</tr>
<tr>
<td>latency (us)</td>
<td>1.90</td>
<td>1.77</td>
<td>2.58</td>
</tr>
<tr>
<td>energy (nJ)</td>
<td>2.12</td>
<td>7.10</td>
<td>64.14</td>
</tr>
</tbody>
</table>

**Conclusion**

- The immune-to-correlation design of the A-SCAU leverages the shared use of RNGs, so significantly smaller area and lower energy consumption are obtained.
- The SC based DBNs can achieve similar accuracy and speed, with significantly smaller area, lower power and energy consumption, compared to conventional binary designs.

**Reference**