A PCM-based TCAM cell using NDR

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***Abstract*— This paper presents a new design of a ternary content addressable memory (TCAM) cell. This design exploits two emerging technology devices: a phase change memory (PCM) as storage element and a negative differential resistance (NDR) device as control element. The PCM stores a multi-value resistance to account for the ternary nature of the equality function to be performed in a TCAM. The CMOS-NDR device uses a macroscopic model made of three transistors to exhibit a very high peak-to-valley current ratio, a single symmetric peak and excellent switching speed. The CMOS-NDR device is embedded in the cell such that specific operational points are placed on the I-V curve for generating the match/mismatch outcome. A common-source amplifier with source degeneration is used for decoding the PCM. Extensive simulation results at nanoscale feature sizes (45, 32 and 22 nm) are presented. These results show that the proposed TCAM cell outperforms a previously presented non-volatile TCAM cell based on MTJ in terms of power dissipation and power delay product (PDP).**

***Index Terms*—TCAM, non-volatile device, PCM, NDR, low power.**

I. INTRODUCTION

Content-addressable memories (CAMs) accomplish storage on the basis of the value of the stored data rather than a physical address location [1]. Among CAMs, the *ternary CAM* (TCAM) has a rich functionality [4]. A major advantage of a TCAM cell over a binary CAM cell is its ability to store and compare with a "don't-care" value (denoted by X). A "don't-care" value acts as a wildcard during the search; the comparison capability of a TCAM is usually referred to as the *equality function*. However, a TCAM requires more circuitry than a normal (storage only) memory cell, so the power dissipation is of concern. Moreover, power dissipation due to leakage current in a CMOS-based cell is significantly increased at the nanoscale feature sizes and a CMOS TCAM is volatile. *Non-volatile memories* have been widely advocated as a major advancement in the technology roadmap. Emerging technologies have the potential to achieve both the non-volatile feature and performance enhancements using novel devices and cell designs. Many memory cells using emerging technologies have been proposed for volatile TCAM design [2][3][5].

Different from previous work, this paper proposes a TCAM design requiring a phase change memory (PCM) that exploits its potential for representing multiple states. The utilization of a single PCM requires a single-peak CMOS-NDR (*negative differential resistance*) device at macroscopic level [6], i.e., a device that shows only one NDR region, instead of the commonly used devices exhibiting multiple NDR regions. The functionality of the proposed design utilizes a modified version of the device in [6] and relies on different so-called *operational points* as related to the match/mismatch outcome, i.e., the operational points are varied according to the storage value of the PCM and the input for the search data. The utilization of a variation of the CMOS-NDR device of [6] permits to distinguish the different operational points in the TCAM equality function and use a PCM to realize the ternary storage at a very low power consumption (as compared to other non-volatile memories such as [7]). Moreover in the proposed cell, the NDR generates a large (small) current flow from the match-line when a mismatch (match) occurs, thus also achieving a significant improvement in PDP.

II. PRELIMINARIES

A. Phase Change Memory

A *phase change memory* (PCM) accomplishes data storage by relying on the reversible phase transformation of the chalcogenide alloy occurring between the amorphous and crystalline states [11]. The *amorphous state* has a high resistance and is commonly referred to as the *reset state*; the *crystalline state* has a low resistance and is referred as the *set state* [11]. A PCM is fabricated by using a thin film chalcogenide layer in contact with a metallic heater. The phase change (PC) process is temperature dependent; a pulse with high amplitude is used to melt and quench the PC element to an amorphous state (Reset State), while a longer pulse with a low amplitude is used to crystallize the PC element (Set State).

B. Negative Differential Resistance

In the past few years, the *negative differential resistance* (NDR) has been widely advocated for many circuit applications. Due to the folding current-voltage (I-V) characteristics, NDR devices have a high functional potential [14]; among them, a multiple-peak NDR device offers a significant promise for multiple-valued logic and the ability to process information with a base higher than binary (i.e. 2). Recently, a new CMOS-based NDR device made of three Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs) and one SiGe-based heterojunction bipolar transistor has been proposed in [6] (Fig.1). Fig. 1 shows the electric circuit model of the NDR device of [6]. Its operation can be described as follows. The total current Is (flowing from Vs) consists of three components, i.e. the drain current of

MN3 (Id3), the gate current of MN2 (Id2) and the drain current of MP1 (Id1),

$$Is=Id3+Id2+Id1 \quad (1)$$

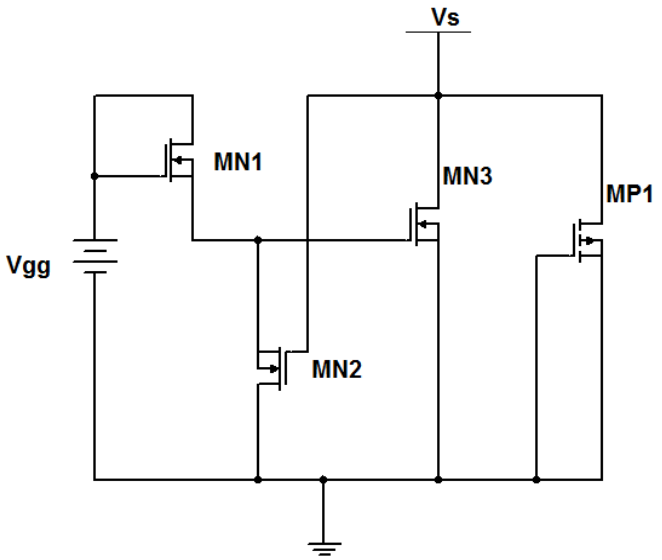

Fig. 1 Circuit-level diagram of NDR device of [6]

If Vgg is fixed to a value larger than the threshold voltage of the NMOS, the operation of this device is characterized by considering three sequentially generated cases, as obtained by gradually increasing the bias voltage Vs in Fig. 1:

1) *First case*: when Vs<Vp (i.e. the peak voltage, as set by the voltage value for turning on the NMOS), MN1 is in the saturation region, MN2 is cut off, MN3 is in the linear region, and MP1 is cut off. The total current Is (that is now equal to Id3) increases linearly with an increase of Vs. This is referred to as the first Positive Differential Region (PDR).

2) *Second case:* when Vs increases, MN1 is in the saturation region, MN2 is in the saturation region, MN3 changes from the linear to the saturation region, and MP1 is in the saturation region. As Vs increases, Id3 decreases considerably and its value cannot be compensated by the slow increase of Id1, because Id3 is a major component of the total current Is, i.e. a negative resistance appears. This is referred to as the Negative Differential Region.

3) *Third case:* finally, when Vs continues to increase, MNI is in the saturation region, MN2 enters the linear region, MN3 is cut off, and MP1 is in the saturation region, Id of MP1 plays a major part in Is; so, as Vgg increases, Is also increases. This region is called the second PDR.

Therefore, the resistance is related to three distinct regions of the I-V plot, i.e. the first PDR region, the NDR region and the second PDR region. Compared to a traditional NDR device, the device of [6] has a small peak voltage and an excellent peak-to-valley current ratio (PVCR). This is caused by the very small turn-on voltage and the high current gain [6]; moreover, the value of Vgg can be utilized to change the peak current (as an important parameter of some logic circuits based on monostable-bistable transition logic elements).

C. *Previous Non-Volatile TCAM Design*

Many articles can be found in the technical literature dealing with memory cells using emerging technologies [2][3], however these designs are volatile [5]. As relevant to the proposed design, a non-volatile TCAM cell has been proposed in [7] [15]. This non-volatile cell consists of two transistors and two MTJs, i.e. 2T2MTJ. The output voltage is determined by the resistance of the comparison logic circuit in the cell. This design however does not fully utilize the multiple value storage capability of a MTJ, so incurring in a considerable power dissipation and a very sensitive circuit operation for the comparison outcome to appear on ML [7] [15].

III. Proposed Cell

In this section, a new TCAM cell that uses a PCM is presented; this cell requires 3 transistors, a resistive load (which can be implemented using a PCM too) and a so-called CMOS-NDR device (Fig. 2). The circuit of this TCAM cell consists of three primary elements: (1) the PCM as storage device, (2) a common-source amplifier with source degeneration (as decoding circuit) and (3) a NDR device with a variation from the one proposed in [6].

The equality operation of the proposed TCAM cell is performed in three phases: write, pre-charge and evaluation phases. The *write phase* involves the PCM as storage element; the resistance of the PCM is determined by the input voltage (this aspect will be discussed in more detail in the next section). Table 1 shows the truth table and related mechanisms of the proposed non-volatile TCAM cell.

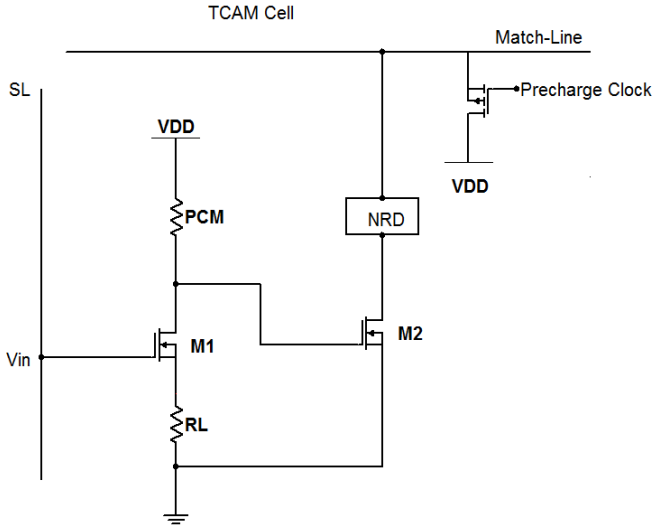

Fig. 2 Proposed TCAM Cell with Search Line (SL) and Match Line (ML).

The *pre-charge phase* starts by pre-charging the Match Line (ML) to Vdd. In the *evaluation phase*, the voltage of ML is varied by the input and the resistance of the PCM to establish the outcome (match or mismatch) of the comparison operation between the stored and search data. This phase consists of the following steps:

TABLE 1: TRUTH TABLE AND MECHANISM OF THE PROPOSED TCAM CELL

Stored data		*Search input*	*Operation outcome*
Stored Value	**Rpcm(Ω)**	**S**	**ML**
0	50k	0	Match
		1	Mismatch
1	180k	0	Mismatch
		1	Match
X	100k	0	Match
		1	Match

Step 1: a decoding circuit is used to establish the resistance stored in the PCM. As shown in Fig. 2, a common-source amplifier with source degeneration is used as decoding circuit. The load resistance RL (that can be also implemented as a PCM) and the PCM connect Vdd to ground (through M1). The drain voltage of M1 is determined by the Search Line (SL) as input and the resistance value stored in the PCM. As reported in Table 1, the PCM range is given by 130KΩ [11] [12], i.e. from 50K to 180KΩ. The resistance values of the PCM (Rpcm) are 50K 100K and 180K Ω to represent the stored values of "0", "X" and "1". The input voltage values from SL are given by 0.6V, 0V and 0.9V to represent the search data values "0", "X" and "1". Fig. 3 shows the I-V curve inclusive of the specific operational points that will be discussed later.

Step 2: following Step 1, the drain voltage of M1 must take six different values, defined as follows. The mismatch operational points are given by "C" and "D"; by using a CMOS-NDR device, the operational points "C" and "D" are located around the peak voltage of the NDR curve to produce a high current flow from ML. The operational points "A"/"B" and "E"/"F" correspond to a match and they generate a low current flow from ML. As shown later in this paper, a substantial difference in current flow from ML to ground is generated to account for the two possible comparison outcomes (mismatch/match).

Step 3: if a match is found (the operational points are A/B/E/F), then a small current flows from ML, causing a small voltage drop in the pre-charged ML. If the operational points are C/D (i.e. a mismatch), then a high current flows from ML, resulting in a large voltage drop at ML.

Hence, the following conditions must be satisfied in the I-V plot of the NDR device. (1) The I-V plot must have only a single symmetrically shaped peak. (2) The mismatch points "C" and "D" must be almost symmetrically placed near the peak voltage of the I-V curve of the NDR device, i.e. at a high current value. (3) The match points "A" "B" "E" and "F" must be placed in the low current portions of the I-V curve of the NDR device. To identify the state stored in the cell (i.e. 0, 1, X), the PCM requires decoding. A common-source amplifier with source degeneration is used for decoding the PCM; as part of the proposed memory cell (Fig. 2), this circuit is shown separately in Fig. 4.

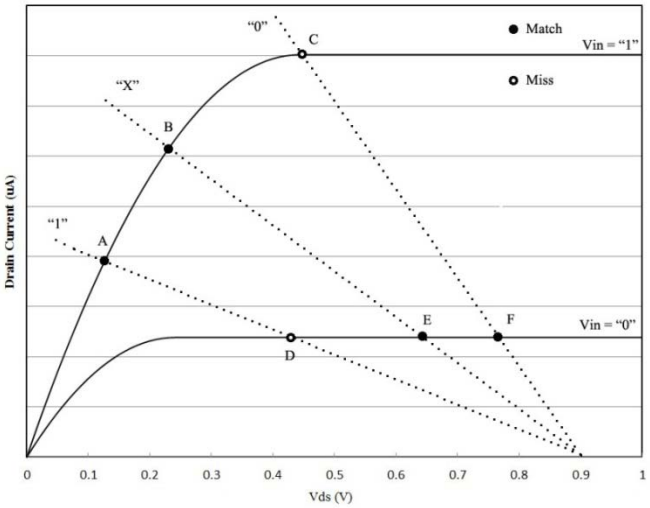

Fig. 3 Operational points of the proposed TCAM cell

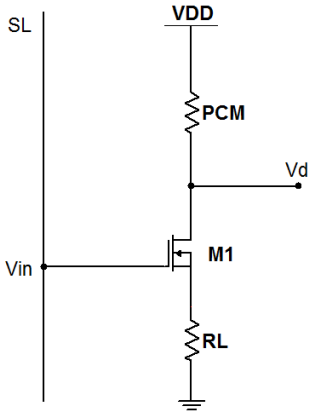

Fig. 4 Common source amplifier with source degeneration

The body of M1 is connected to ground; therefore, the dc body voltage is constant and equal to zero. Its small-signal circuit is given in Fig. 5 for analysis purposes. By applying KCL at the drain node, substituting for V_{gs}, V_{sb} and using $g_{mb} = \eta g_m$, the body effect can be ignored, so

$$\frac{V_d}{V_{in}} = \frac{-g_m R_{PCM}}{1+g_m(1+\eta)R_L} \quad (2)$$

(2) establishes a relationship between the values of the resistance of the PCM (i.e. R_{PCM}) and the SL input voltage, such that the six operational points of the drain of M1 (as shown previously in Fig. 3) can be established and placed on the I-V plot of the NDR device.

IV. MACRO MODELING AND CIRCUIT ANALYSIS

This section introduces the modeling and the circuit analysis of the two major components of the proposed TCAM cell. The macromodel of [13] is used for the PCM; the input and output voltages are provided to the circuit to establish its state (ON or OFF) and resistance. At electrical level and as applicable to this macromodel, the state of the PCM is established (ON, or OFF) when there is a voltage difference across the in and out nodes. Due to lack of space, the interested reader should refer

to [13] for a detailed treatment of the HSPICE macromodeling of a PCM cell as used in this paper.

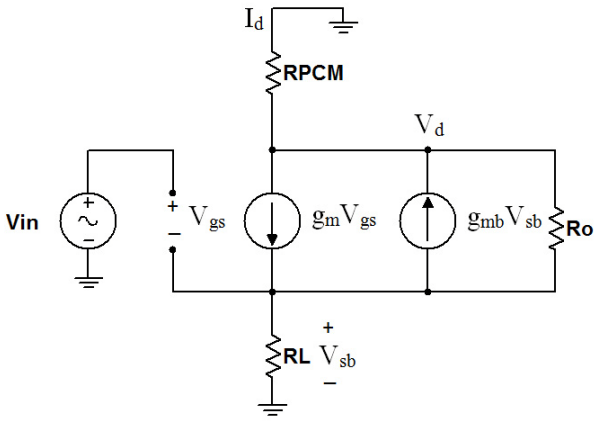

Fig. 5 Common source amplifier with source degeneration

The NDR device of [6] (Fig. 1) does not fully meet the conditions set previously for the operations of a TCAM cell. Fig. 6 shows the new circuit of the macro modeled CMOS-NDR device when it is changed for the proposed TCAM cell; this circuit is a variation of the one of Fig. 1 [6]. MP1 has been removed and the remaining MOSFETs are now embedded in the memory cell (Fig. 2) and connected to the Match Line (ML) and M2. The I-V plot of the CMOS-NDR device reflects a single peak and is given as follows. (1) The current-rising region corresponds to the case when M4 is saturated, M3 is cut off and M5 is saturated. (2) The NDR (current-falling) region corresponds to the case when M4 is saturated, M3 is saturated and M5 is active.

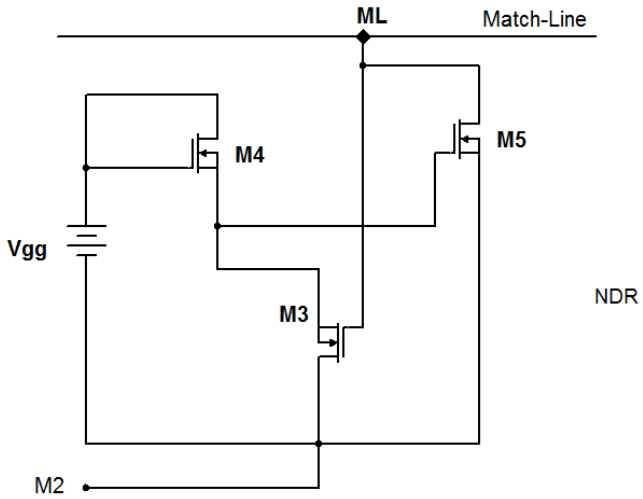

Fig. 6 Circuit of macro modeled CMOS-NDR device in the proposed TCAM cell

Next, features such as the single high peak current and the strong pull up/down characteristics must be appropriately specified for the operational points of the proposed design and their placement on the I-V plot. The three pairs of operational points (described previously and shown in Fig. 3) and their placement on the I-V plot can be found using the widths of M3 and M5 together with the value of Vgg, such that the I-V curve of the CMOS-NDR device can be adjusted.

The following observations are applicable to the proposed TCAM cell and the macro modeled CMOS-NDR device. (1) A change in Vgg will change the peak current of the I-V curve. The voltage source Vgg is used to maintain symmetry in the shape of the I-V curve. (2) The width of M3 controls the peak current and voltage of the NDR device. (3) M5 affects the peak voltage of the I-V curve to match it with the corresponding output of the decoding circuit. If its width is increased, the peak voltage moves to the left and the peak current decreases. M5 also affects the peak current of the I-V curve as an appropriate value for a correct comparison operation; M5 has the reverse effect of M3, i.e. as the width increases, the peak voltage moves to the right and the peak current increases too. An appropriate voltage must be selected for the I-V curve of the CMOS-NDR device such that a high (low) current flow from ML occurs for a mismatch (match). This is shown next using a design at a feature size of 45nm as an example. The transistor widths at 45nm are as follows: 45 nm for M1, M2 and M4, 150nm for M3 and 90nm for M5. (2) establishes the relationship for the amplifier of Fig. 5 to decode the PCM. This process relies on finding specific points on the I-V plot of Fig. 7 as initially derived from Vd of the drain of M1. Let for example RL=50KΩ; as M1 has a feature size of 45nm, the widths of the other transistors are used to attain the required I-V plot with the operational points (Fig. 7), i.e. the mismatch operational points "C" and "D" are placed symmetrically around the peak voltage of the I-V curve, while the match points "A" "B" "E" and "F" are placed in the low current portions of the I-V curve.

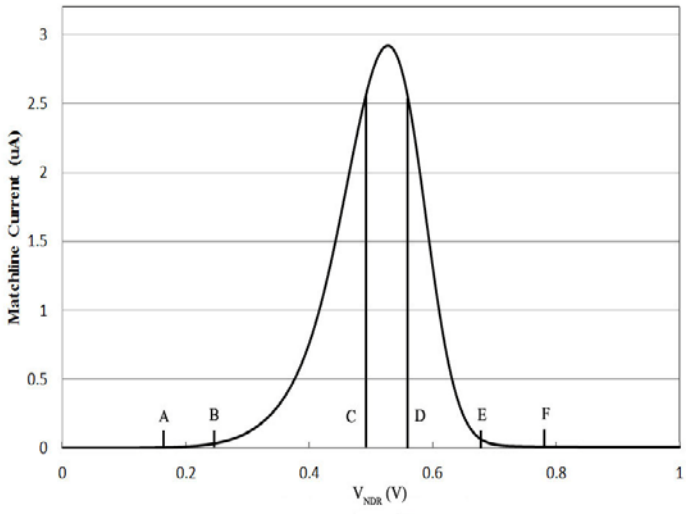

Fig. 7 The operational points in the I-V plot of the CMOS-NDR device

Table 2 shows the voltage at Vd with respect to the three states of the PCM (with the corresponding resistances) and the operational points by considering the equality function between the stored and the search values of the TCAM cell. Previously, the different circuit elements of the proposed TCAM cell have been evaluated individually. Next, simulation

of the complete functionality of the proposed TCAM cell is pursued.

TABLE 2: OPERATIONAL POINTS OF M1 IN FIG. 3

Stored data		*Search input*	*Voltage at Vd (V)*	*Operation outcome*
Stored value	**Rpcm(Ω)**	**S**	**(Operational points)**	**ML**
0	50k	0	0.820 (F)	Match
		1	0.583 (C)	Mismatch
1	180k	0	0.632 (D)	Mismatch
		1	0.271 (A)	Match
x	100k	0	0.736 (E)	Match
		1	0.382 (B)	Match

All simulations are performed using HSPICE with the PTMs at CMOS feature sizes of 22nm, 32nm and 45nm. Consider the ML voltage when the PCM stores "1" (R_{PCM} = 180KΩ), "0" (R_{PCM} = 50KΩ) and "X" (R_{PCM} = 100KΩ); note that in the pre-charge phase, ML is pre-charged to Vdd when the pre-charge pulse is equal to zero. The following cases are therefore applicable to the three stored values. (1) When a "1" is stored in the PCM (i.e. R_{PCM}=180KΩ) then the following subcases are applicable: if SL is high, the operational point is "A", i.e. a match; if SL is low, the operational is "D", i.e. a mismatch. (2) The PCM stores a "0"; so, ML is discharged when SL is high (mismatch), but it remains high when SL is low (match). When SL is 0V (i.e. the "don't care" condition), the NMOS transistors are cut off and ML remains high, because no current is flowing. (3) When an "X" (i.e. "don't care") is stored in the PCM, the operational points are "B" or "E", a small current flows from ML. Since the PCM stores an "X", ML always indicates a match and is not discharged to ground independently of the value of SL. Simulation results have confirmed the correct functionality of the proposed memory cell.

V. EVALUATION AND COMPARISON

In this section, the performance of the proposed TCAM is assessed and compared with the TCAM of [7] [15]. A temperature of 25 ℃ **i**s used as default value in the HSPICE evaluation**.** Vdd is given at the default value of the PTM.

TABLE 3: AVERAGE POWER CONSUMPTION AND DELAY OF PROPOSED TCAM

	45nm	**32nm**	**22nm**
Match power	3.91uw	3.77uw	2.85uw
Mismatch power	4.97uw	3.28uw	2.69uw
Miss Delay	23ps	49ps	66ps

Simulation at different feature sizes (45, 32 and 22nm) in the macromodel by changing the value of RL (as per (2) with 60k, 45k and 35k as values) for the search time and the power dissipation is pursued (Table 3). The decrease in power consumption is related to the decrease in values of the feature size and the resistance RL (reflected also in the operation of the common source amplifier as decoding circuit).

For comparison purposes, the 2T2MJT TCAM design of [7] [15] has also been evaluated at different feature sizes; the simulation results are reported in Table 4. The same trends as for the proposed TCAM cell are observed in the performance metrics. Table 5 shows the comparison of the power delay product (PDP), in which the power consumption is averaged over both cases of outcome (i.e. match and mismatch). The proposed non-volatile cell clearly outperforms [7] [15].

TABLE 4: AVERAGE POWER CONSUMPTION AND DELAY OF 2T2MTJ CAM

	45nm	**32nm**	**22nm**
Match power	28.78uw	21.15uw	13.92uw
Mismatch power	18.21uw	14.1uw	9.94uw
Miss Delay	20ps	31ps	44ps

TABLE 5: POWER DELAY PRODUCT (PDP) COMPARISON

PDP	**45nm**	**32nm**	**22nm**
Proposed TCAM	102.12	172.72	182.82
2T2MTJ TCAM	469.90	546.37	524.92

At nanoscale dimensions, variations may affect circuit-level performance [12]. The analysis of temperature, voltage and process (PVT) variations for the proposed TCAM cell is pursued next at a 32nm CMOS feature size. Table 6 shows the miss delay over a temperature range of 0 to 100℃. As expected, the miss delay increases with temperature.

TABLE 6: MISS DELAY AT TEMPERATURE VARIATION FOR PROPOSED TCAM

Temperature (℃)	**Miss Delay (ps)**
0	45.70
25	49.21
50	51.35
75	63.22
100	76.93

The operational points of M1 will change due to a voltage variation, eventually causing a failure in the equality function of the proposed cell. The miss delay and comparison outcome at different supply voltages are reported in Table 7; these results include both match/mismatch outcomes for all three values, i.e. 0/1/X. Table 8 shows that the supply voltage affects the operational points in Fig. 7 as determining the input resistance of the CMOS-NDR device; if the supply voltage is decreased from 1 V to 0.86V an incorrect result will appear in the equality function (as comparison operation outcome). Table 8 shows the miss delay at different process corners at 32nm feature size. The fast fast (slow slow) corner results in a

process variation of nearly 3%. In both cases, the change in miss delay from the normal corner is nearly 22%. Note that no variation is assumed in the PM itself.

TABLE 7: VOLTAGE VARIATION OF PROPOSED TCAM

Supply Voltage (V)	Miss Delay(ps)	Operation outcome
0.98	47.51	*correct*
0.95	45.28	*correct*
0.92	43.3	*correct*
0.89	41.39	*correct*
0.88	39.76	*correct*
0.87	38.11	*correct*
0.86	37.58	*incorrect*

TABLE 8: DELAY AT DIFFERENT PROCESS CORNERS

Corner	Miss Delay(ps)
Fast fast (-3%)	38.73
Normal	49.21
Slow slow (+3%)	61.29

VI. CONCLUSION

This paper has presented a novel non-volatile TCAM cell; its design is based on utilizing a phase change memory (PCM) as storage devices and a macro modeled CMOS-NDR (negative differential resistance) device to attain accurate control of the cell current for extremely low power dissipation. These two devices exploit different features of emerging technologies. The PCM introduces very low power dissipation, while still reducing the active power for non-volatile operation; moreover different from previous cells, a non-volatile PCM is utilized to provide all three resistance values for the ternary operation of the cell. A further novelty of the cell proposed in this paper is the circuit design of the NDR device. The proposed CMOS-NDR device is a simple variation of [6] with a circuit macro model made of three transistors; when embedded in the proposed memory cell, it generates a single peak symmetric I-V plot that can be controlled by the widths of its MOSFETs. Its features are utilized in the TCAM cell by generating a large (small) current flow from the match-line when a mismatch (match) occurs. A common-source amplifier with source degeneration has been used for decoding the state stored in the PCM cell (i.e. 0, 1 or X); this amplifier also ensures that the TCAM cell operates within the I-V plot generated by the macro modeled CMOS-NDR device. This feature results in significant advantages of the proposed TCAM cell compared with another non-volatile cell [7] [15] in terms of considerable reductions in power consumption and PDP.

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