A System-level Scheme for Resistance Drift Tolerance of a Multilevel Phase Change Memory

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***Abstract*—This paper presents a system-level scheme to alleviate the effect of resistance drift in a multilevel phase change memory (PCM) for data integrity. In this paper, novel criteria of separation of the PCM resistance for multilevel cell storage and selection of the threshold resistances between levels are proposed by using a median based method based on a row of PCM cells as reference. The threshold resistances found by the proposed scheme drift with time, thus providing an efficient and viable approach when the number of levels increases. A detailed analysis of the proposed level separation and threshold resistance selection is pursued. The impact of different parameters (such as the write region and the number of cell in a row) is assessed with respect to the generation of the percentage accuracy. The proposed approach results in a substantial improvement in performance compared with existing schemes found in the technical literature.**

Index Terms*—Phase Change Memory (PCM), Multilevel, Tolerance, Resistance drift.

I. Introduction

The phase change memory (PCM) has emerged in recent years as one of the most promising technologies for future non-volatile solid-state memories with significant implications on the entire storage hierarchy [1]. PCM has attracted considerable attention due to its low latency, good endurance, long retention and high scalability compared to other non-volatile memories. A PCM relies on the reversible phase transformation of the chalcogenide alloy (e.g. $Ge_2Sb_2Te_5$, GST) between the amorphous and the crystalline states. The amorphous state has a high resistance and is commonly referred to as the *reset state*; the crystalline phase has a low resistance and is referred as the *set state* [2]. There is a large resistance margin between the amorphous and the crystalline phases, so a PCM can store multiple bits of information in a single cell; this is accomplished through a multilevel storage implementation based upon incomplete phase transitions. Advantages such as increased storage density and hence lower cost, are of primary importance for the successful development of multilevel memory systems using PCM [3]. However as shown in recent studies [4][5][6], the resistance of a phase change material such as GTS tends to drift over time. The change in resistance severely degrades the margin between adjacent levels of a cell, leading to a serious reliability challenge and loss of data storage integrity [3].

This paper analyzes the multilevel storage (ML) of a PCM under the presence of drift in its resistance. A novel system-level scheme that utilizes as initial step the metric of median value in the selection of the percentage accuracy of every level, is proposed. This is based on the condition that the threshold resistances of the levels are allocated to be very close in values, i.e. flat. This also allows the threshold values to change as the drift occurs, because they are established using a median value found in a row of PCM cells; a detailed analysis of the proposed level separation and threshold resistance selection is pursued. The impact of different parameters (such as the write region and the number of cell in a row) is assessed with respect to the generation of the percentage accuracy. The proposed approach results in a substantial improvement in performance compared with [7]; extensive simulation results are provided to show that the use of the proposed median based technique in a multilevel storage memory using PCM cells achieves these performance improvements.

II. Resistance Drift of Phase Change Memory

The resistance drift of a PCM is believed to be the result of structural relaxation (SR) phenomena that are thermally activated as an atomic rearrangement of the amorphous structure [7]. It has been observed that the drift is significant in the high resistance state (RESET state), in which the phase change material is programmed to the amorphous phase. The low resistance state (SET state) shows a nearly negligible time-dependence of resistance [7]. The rate of resistance increase exhibits a behavior that is strongly related to the time elapsed after programming; this relationship is given by [7].

$$R_T = R_0\left(\frac{T_{off}}{T_0}\right)^{\upsilon_r} \quad (1)$$

where R_T is the resistance of the PCM cell during the drift time T_{off}. T_{off} denotes the time that PCM cell is allowed to drift (i.e. not programming or reading), υ_r is the so-called *drift coefficient* of the PCM resistance and is dependent on the initial resistance value (R_0), i.e. R_0 is the initial PCM resistance at time T_0, where T_0 is a time constant [5]. The resistance drift exponent of the PCM (υ_r) varies depending on R_0, i.e. at a larger value of R_0, the mean value of the drift exponent (υ_r) tends to have a larger value. The relationship between the resistance drift exponent (υ_r) and the initial resistance of the PCM cell (R_0) can be found as follows.

By rearranging (1),

$$\frac{R_T}{R_0} = \left(\frac{T_{off}}{T_0}\right)^{\upsilon_r} \quad (1.1)$$

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$$\ln\left(\frac{R_T}{R_0}\right) = \upsilon_r * \ln\left(\frac{T_{off}}{T_0}\right) \quad (1.2)$$

As T_0 is normalized (for simplicity of analysis, it is made equal to an unitary time) and R_0 is given (as per PCM specifications), then (1.2) can be rewritten as

$$\ln(R_T) - \ln(R_0) = \upsilon_r * \ln(T_{off}) \quad (1.3)$$

Let $\ln(R_T)$ and $\ln(T_{off})$ be constant values (and denoted as A and B respectively); at a specified time, T_{off}, (1.3) is given by

$$A - \ln(R_0) = \upsilon_r * B \quad (1.4)$$

$$\upsilon_r = \frac{A}{B} - \frac{1}{B}\ln(R_0) \quad (1.5)$$

Let α be equal to $-\frac{1}{B}$ and β be equal to $-\frac{A}{B}$, then the relationship between υ_r and $R_0$is

$$\upsilon_r = \alpha \ln(R_0) - \beta \quad (2)$$

Consider as an example the experimental data of [3]; α is equal to 0.0153 and β is equal to 0.1138.

III. MULTILEVEL STORAGE

Multilevel storage is achieved through an accurate programming of the PCM cell into intermediate resistance values, i.e. the values between the SET and RESET states [1]. This scheme however, is susceptible to process and material variability; for example, the temperature that is generated in the PCM by using the same programming pulse, varies from cell to cell. Therefore, a single pulse programming arrangement is not a viable option for multilevel PCM storage, because the resulting resistance level distributions are rather broad and difficult to predict [1]. A possible solution is to employ an iterative programming strategy that starts by reading the most recent resistance value of a PCM and comparing with a reference value; then, a programming current is utilized to bias and adjust the resistance of the PCM cell to the desired value. The PCM cell is then read again to ensure that the new resistance is as expected; if not, the above process is repeated. The process of iteratively programming and verifying a multilevel PCM cell (through multiple read and write operations) is shown in Figure 1 [1].

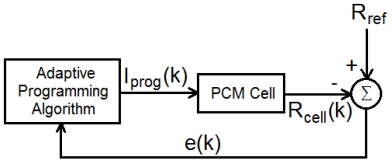

Figure 1. Iterative scheme for programming and verifying a multilevel PCM cell

A *reference resistance* (R_{ref}) is required for each level in the execution of the iterative programming process and the verification of the programmed PCM cell (Figure 1). However, the constant reference resistance degrades data integrity [3]. As shown in Figure 2, the resistance at each level varies according to a Gaussian distribution and accounts for less (more) drift when the PCM is in the (amorphous) crystalline phase. The resistance of each level changes during T_{off} (denoted by T in Figure 2) following the selection of the so-called threshold resistances (as separating the levels). This results in an erroneous output following a read operation due to overlapping levels in a PCM cell.

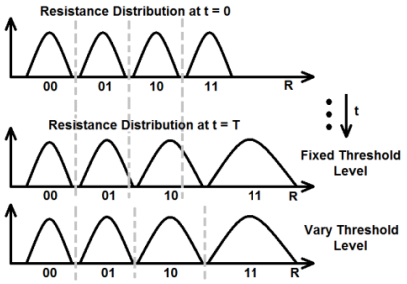

Figure 2. PCM resistance distribution over time

The erroneous effects of the resistance drift in a PCM cell can be alleviated if the threshold resistances could also vary with time. In [3], a time-aware fault-tolerant scheme is used for correcting the resistance drift of a PCM. The drift behavior of the threshold resistance is taken into account by the so-called *lifetime* of the PCM (t_d) in the form of *time tag* bits and using them to find the threshold resistances; however, the lifetime and the threshold resistances require an extensive calculation at an added circuit complexity and overall degradation in figures of merit, such as delay and power dissipation of the memory.

In this paper, the reference resistances of the PCM cell under a drift behavior are generated as follows. A row of PCM cells (Figure 3) is utilized. Initially, the resistance of every PCM cell in a row is set to the threshold value of that level. During a read or write operation, the input current is provided to each line in the so-called row of threshold resistance (denoted by L1, L2, … , LN). The transistor Mth is then turned ON, every PCM cell on the row (Figure 3) is read by monitoring the voltage of each line (i.e. L1, L2, … , LN). The resistance of each PCM cell in the row (Figure 3) is therefore given by

$$R_N = \frac{V_N}{I_{read}} \quad (3)$$

where R_N is the PCM resistance at line N, V_N is the voltage at line N when the read current (I_{read}) is provided to every line.

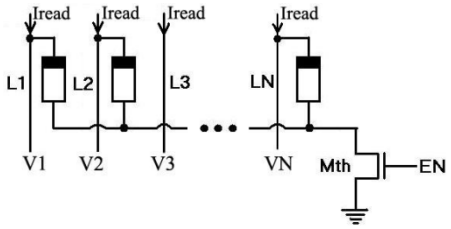

Figure 3. Row of PCM cells for calculating the threshold resistance of a level

After reading the resistances of the lines (Figure 3), the threshold resistance is established by calculating the median value, i.e. the median resistance is selected as the threshold resistance of a level.

The threshold resistances are used to partition the resistance of each PMC cell into *regions* (Figure 4). During a read or write operation, the threshold resistances are used as reference resistances (R_{REF}) and compared to the corresponding resistances of a PCM cell (Figure 1). All resistances however drift; so by selecting the threshold resistance between regions, the drift of the threshold resistances still occurs, but its effects are mitigated.

However, an additional criterion (referred to as *resistance separation*) must be considered too.

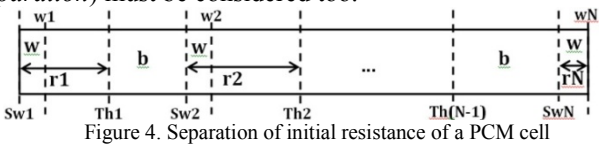

Figure 4. Separation of initial resistance of a PCM cell

Figure 4 shows the resistance separation of a PCM cell used in this manuscript; the initial resistance of the PCM is divided into several so-called *regions*. The following regions are defined for a level: the write region (w), the read region (r) and the blank region (b). The write region (w) is the region for which the PCM resistance can be written at the designated level, the write region starts from swX and ends to wX, where SwX and wX are the starting and ending values of the write region of level X respectively. ThXis the threshold resistance of level X. If the resistance of the PCM is higher than swX and less than ThX, this region is referred to as the *read region* of level X.

The threshold resistance of a level (ThX) is selected from a row of PCM cells (Figure 3). Since the drift behavior of each PCM cell is different, it is possible that ThX drifts higher than the starting value of the write region of the next level (Sw(X+1)), thus resulting in an incorrect write/read operation. A *blank* region (b) is used to protect this from occurring. As shown in Figure 4, each level of a PCM is separated into 3 regions; the last level (level N) has only a single (write) region, because the PCM is totally amorphous; at this high resistance value, no threshold resistance is needed. Due to the non-linear nature of the resistance drift behavior (as evidenced by (1)), the read and blank regions must be increased at least by the same rate as the PCM resistance drift. The process for finding the level separation is then discussed in the next section.

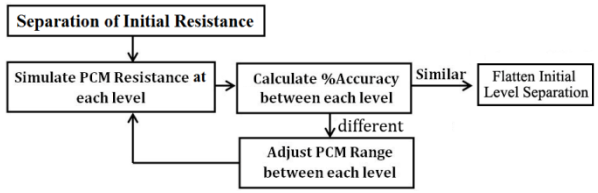

Figure 5. Flowchart of initial resistance separation for a cell with N levels

IV. Level Separation

Figure 5 shows the flowchart of the process for finding the initial level separation of the PCM. The PCM cell is separated into levels; each level is simulated and compared with its value for the read region. If the PCM resistance is in the read region of that level, then the data is valid and retained. However if the PCM resistance is not in the read region of the level, then the data in the cell is erroneous due to the drift behavior. A comprehensive process referred to as the *flat initial level separation* must be undertaken. This is found by calculating the percentage accuracy in each level and adjusting the level resistances till the percentage accuracies are very close.

In this paper, the level separation resistance is given in percentage form, i.e. it is equal to 0% (100%) when the PCM is totally crystalline (amorphous). The percentage resistance of the PCM is converted into the crystalline fraction (C_X) by the following equation

$$C_X = 1 - \frac{\%\text{Resistance}}{100} \quad (4)$$

Example: Consider a PCM cell with 3 levels and assume that the write region is given by 1%, the initial threshold resistances of levels 1 and 2 (Th1 and Th2) are separated by 25% and 75% respectively. The initial level separation (as shown in Figure 4) is generated as follows.

	Sw1	***W1***	***Th1***	***Sw2***	***W2***	***Th2***	***Sw3***	***W3***
%	0	1	25	50	51	75	99	100

Table 1. Initial Percentage PCM Resistance Separation

After partitioning into levels, the drift must be assessed and therefore the PCM cell and its resistance are simulated. The worst case of resistance drift at a level is considered by simulating the lower and higher band errors. The *lower band error* occurs when the threshold resistance of the previous level (Th(X-1)) drifts until its value is higher than the starting value of the write resistance in the current level (SwX).The *higher band error* occurs when the resistance of the current level drifts until its value is higher than its threshold resistance (ThX). The threshold resistances are generated using a row of PCM cells (Figure 3).The initial PCM resistance of every cell in a row is set to the initial threshold value (ThX). After a drift time (T_{off}), the threshold resistance of a level is found from the median resistance among the PCM cells on the row. These values are used as reference resistances (Figure 1) for the read and write operations of the PCM cell.

$$E_{min,i} = \frac{L_i}{M} * 100 \quad (5)$$

$$E_{max,i} = \frac{H_i}{M} * 100 \quad (6)$$

The percentage errors of the lower band (E_{min}) and higher band (E_{max}) are given by (5) and (6) respectively. $E_{min,i}$ is the percentage error of the lower band for level i, L_i is the number of PCM cells at level i for which the threshold resistance of the previous level ($R_{TH(i-1)}$) is higher than the starting write resistance in the current level (R_{Swi}), and M is the number of PCM cells in the memory array. $E_{max,i}$ is the percent error for the higher band when the worst case at level i is considered, H_i is the number of PCM cells at level i such that its resistance is higher than its threshold value. The worst case of the higher band error occurs when the PCM is written to the ending value of the write region (wX).

$$A_{min,i} = 100 - E_{min,i} = (1 - \frac{L_i}{M}) * 100 \quad (7)$$

$$A_{max,i} = 100 - E_{max,i} = (1 - \frac{H_i}{M}) * 100 \quad (8)$$

(7) and (8) give the percentage accuracies of each level of a PCM. $A_{min,i}$ and $A_{max,i}$ are the percentage accuracies of the PCM at level i for the lower and higher band errors respectively. Due to the variation in PCM resistance, the percentage accuracy of a cell is not the same in each simulation run; so, the lower and higher band percentage accuracies ($A_{min,i}$ and $A_{max,i}$) are simulated N_S times to find the average values as well as the average percentage accuracy of each level. The *flat percentage accuracies* for both the lower and higher bands are then established. If the least and highest values of percentage accuracy are

substantially different, part of the resistance for the region with the highest percentage accuracy is allocated to the region with the least percentage accuracy. This effectively balances the percentage accuracies among the levels of the PCM cell; this process is referred to as the *flat initial level separation*.

The percentage accuracies of the lower and higher bands at each level after time T_{off} are found based on the initial percentage resistance of each level (Table 1). The initial resistance range is given by 7kΩ – 200kΩ.

Level	***1***	***2***	***3***
%Lower Band	-	99.0079	80.5079
%Higher Band	100	90.4539	-

Table 2. Percentage accuracies when the PCM resistance is initially separated (from Table 1)

As shown in Table 2, the percentage accuracy of the lower band of level 3 has the least value, while the percentage accuracy of the higher band of level 1 has the largest value. The PCM can better tolerate the drift behavior by adjusting the PCM resistance in each region, so the percentage accuracies of each level separation are closer.

V. Adjustment and Selection

This section presents the adjustment process of a multi-level PCM cell. The level resistances must be adjusted to balance the average percentage accuracies of a PCM. If the values of the least and largest percentage accuracies are close together, tolerance to the resistance drift is said to be balanced and the so-called *flat initial level separation* is accomplished. Else, an adjustment must be considered.

The percentage accuracy is dependent on the level separation, i.e. the lower band percentage accuracy is related to the blank region of the previous level, while the higher band percentage accuracy is related to the read region of the considered level. As the write region (w) has a constant value, then the higher band percentage accuracy is related to the resistance difference between the ending value of the write region (Wx) and its threshold value (ThX). If the value of the higher band of the percentage accuracy of level X is the highest (maximum), a portion of the resistance from this region can be allocated to the region with lower percentage accuracy. Also, the reverse scenario can be taken care by such adjustment. The percentage accuracies of the levels of a PCM are made close in value by using this method,.

Example: Based on Table 2, the percentage accuracy of the higher band of level 1 (corresponding to its read region) is the highest. However, the percentage accuracy of the lower band of level 3 has the least value (as the blank region of level 2 is low). So, the initial resistances must be adjusted. If the difference between the least and largest percentage accuracies of the levels (Table 2)is high (i.e. 5%), then the percentage resistance in each region is adjusted by 0.1%; if such difference is less than 2%, then the adjustment is given by 0.01%. However, if the difference is higher than 2% but less than 5%, the percentage resistance is adjusted by 0.05%. So based on the average percentage accuracy of each level (Table 2), the initial percentage resistance of the read region of level 1 is reduced by 0.1%, while the percentage resistance of the blank region of level 2 is increased by the same amount. These adjustments are shown in Table 3.

	Sw1	***W1***	***Th1***	***Sw2***	***W2***	***Th2***	***Sw3***	***W3***
%(Non-Adjusted)	0	1	25	50	51	75	99	100
% (Adjusted)	0	1	24.9	49.9	50.9	74.9	99	100

Table 3. Adjustments to the initial percentage resistance separation

Based on the initial percentage level separation, the percentage resistance of Th1 is changed to 24.9%. For the resistance range of the other regions to be the same, Sw2 must be 49.9, because the blank region of this level is still equal to 25% (50-25 = 49.9-24.9). The percentage for the write region is fixed at 1%, so W2 is 50.9%. Next, the percentage resistance of Th2 is considered, because Sw3 and W3 are fixed at 99% and 100% respectively. The percentage accuracy of the lower band of level 3 has the least value; so the blank region of level 2 must be increased by 0.1%. From the non-adjusted level separation, the resistance difference between Sw3 and Th2 is 24%. By increasing this resistance range by 0.1%, the percentage resistance of Th2 is equal to 74.9% and Sw3 – Th2 = 24.1%. Therefore, the initial level separation is completed. The percentage accuracy is found for each region by simulating again the PCM cell and the initial PCM resistance is adjusted until the percentage accuracies are close in value.

Level	***1***	***2***	***3***
Sw	0	9.15	99
W	1	10.16	100
Th	3.16	22.16	-
%Lower Band	-	99.9346	99.9952
%Higher Band	99.9016	99.8909	-

Table 4.Flat initial percentage resistance separation and percentage accuracy of each level for a PCM cell with 3 levels

Table 4 shows the flat initial level separation when the write region is fixed at 1%; the percentage resistance of each level is adjusted until the difference in percentage accuracy (between the least and the largest values) is close. The threshold resistance of each level must be selected after finding the level separation for flattening the percentage accuracy. The threshold resistance of each level is selected from a row of cells by using the median method. Compared with the mean (average) method for selecting the threshold resistances, the median method selects only one PCM cell in a row as holding the reference resistance; hence, the power dissipation is significantly less, while it is not significantly affected when considering the drift behavior of the threshold resistances.

VI. Simulation Results

In this section, the simulation and discussion of the proposed schemes for flat level separation and threshold resistance selection are pursued at cell-level. The data of [8] is used to simulate the resistance drift of a PCM cell; MATLAB is used as simulation tool. Table 5 shows the parameters used to simulate the level separation, the threshold resistance selection and the percentage accuracy of each level. The resistance drift of the PCM (R_T) is calculated using (1); based upon experimental

measurements [9], [10], the two parameters (R_0 and υ_r) approximately follow a Gaussian distribution and the drift exponent (υ_r) increases as R_0 increases [8].

Parameter	*Value*
Reset Resistance (R_a)	200 kΩ
Set Resistance (R_c)	7 kΩ
α Constant of $\upsilon_r(2)$	0.0153
β Constant of $\upsilon_r(2)$	0.1138
SDMR of υ_r	20%
Time constant (T_0)	1 ns
Percent write region of each level (w)	1%
Number of PCM cell in each row (Nth)	16
Number of PCM cell in the memory array (M)	10,000

Table 5. Parameters for simulating PCM cell

υ_r is calculated from (2) using a constant R_0 and varies according to a Gaussian distribution $\mathcal{N}(\mu_\upsilon, \sigma_\upsilon^2)$, υ_r is used as the mean value of the Gaussian distribution (i.e. μ_υ).The resistance drift is calculated using the flowchart of Figure 6 by assuming that all levels have the same standard deviation to mean ratio (SDMR) [8].

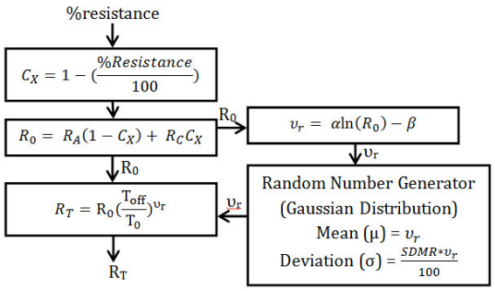

Figure 6.Flowchart of resistance drift calculation

Initially, the percentage resistance (denoted as %resistance) is selected and the crystalline fraction of a PCM cell (C_X) is calculated. The initial PCM resistance (R_0) is then generated. The drift coefficient (υ_r) is calculated using (2); as υ_r varies according to a Gaussian distribution, the mean of this distribution is set to υ_r. Its deviation is given by 0.2*υ_r as required for a 20% SDMR (Table 5) [8]. (1) is used to calculate the resistance drift of a PCM cell (R_T) at time T_{off} (where T_{off} is the time that the PCM cell is allowed to drift). t_0 is the time constant at which R_0 is read, i.e. t_0 is nearly equal to zero, because the initial resistance is read following a write operation (in this paper,t_0 has a value given by 1ns).The resistance drift behavior of the PCM cell is found by simulating and making its variation to follow a Gaussian distribution.

A. Flat Initial Level Separation

In this section, the PCM resistance is divided into 4 levels. The percentage of the write region at every level (w) is constant (1% is assumed).The number of PCM cells in each row for finding the threshold resistances (N) is given by 100 while the number of PCM cells in the memory array (M) is given by 10,000. A flat initial separation of PCM is found by using the proposed method. Table 6 shows the flat initial level separation of a cell with 4 levels at a 1% write region. Based on the simulation results of Table 6, the percentage accuracies of both the lower and higher bands are close together at nearly 98%. The tolerance of every level due to drift is nearly the same.

Level	*1*	*2*	*3*	*4*
sw	0	5.2036	21.85697	99
w	1	6.2036	22.85697	100
Th	2.5	10.66245	41.00371	-
%Lower Band	-	98.424	98.9862	99.136
%Higher Band	98.8204	98.2047	97.9745	-

Table 6.Flat initial PCM level separation, 4 levels/cell and write resistance is 1%

B. Write Region

This section considers the effects of the write region (w) (as found in the flat initial level separation) and the average percentage accuracy level when the PCM resistance is initially separated using the proposed technique.

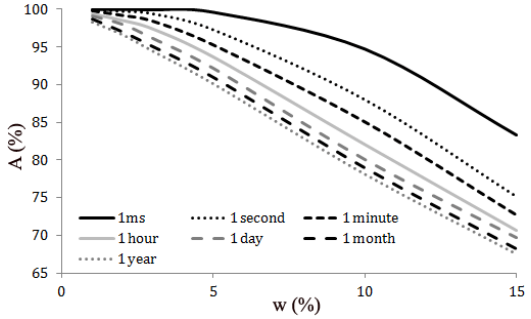

Figure 7. Average percentage accuracy of PCM (4 levels per cell and T_{off} at 1 ms, 1 second, 1 minute, 1 hour, 1 month and 1 year)

As shown in Figure 7, the average percentage accuracy at higher percentage write region is lower due to the adjustment in resistance among regions. Moreover, the average percentage accuracy at a lower value of T_{off} is higher.

C. Threshold Resistance

In this section, the number of PCM cells in a row (Figure 3) for finding the threshold resistance of each level is considered. As shown in Figure 8, the relationship between the average percentage accuracy (A) and the number of PCM cells in a row (N) is found.

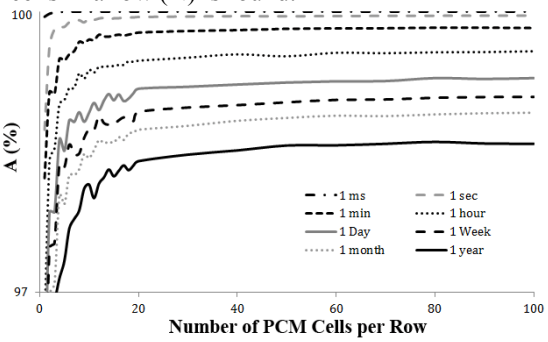

Figure 8.Average percentage accuracy of a PCM cell with 4 levels, 1% write region (T_{off} time of1ms, 1second, 1 minute, 1 hour, 1 day, 1 week, 1 month and 1 year)

Figure 8 plots N versus A when finding the threshold resistances by using the proposed median method (at a constant write region percentage of 1%); when N is reduced, A is also substantially reduced, thus showing that the

proposed method is viable for large memory arrays. However, at a higher number of PCM cells per row, the found median value is likely to be appropriate to account for the resistance drift. Moreover, N does not significantly affect A, because it reaches a saturated value (albeit at different T_{off} values).

D. Lifetime

In this section, a comparison of the so-called lifetime is pursued using the proposed flat PCM level separation and the resistance margin scheme [7]. The resistance margin between any adjacent states is increased in [7] to prevent the post-drift resistance levels to overlap. The margins between any two adjacent states are non-uniform and increase significantly; for example a 5 fold resistance difference between any pair of adjacent states (i.e. $R_{state00}/R_{state01} = R_{state01}/R_{state10} = R_{state10}/R_{state11} = 5$) allows data to be valid for 2 years at room temperature [7].

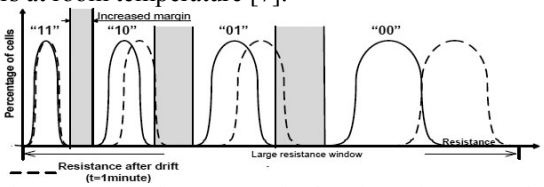

Figure 9. PCM resistance separation by using resistance margin [7]

The resistance margin scheme of [7] incurs in few disadvantages. One of the most evident disadvantages is with respect to the lifetime, i.e. the time for the PCM to be viable as storage (and its stored data is correct); the lifetime of a PCM cell is dependent on the resistance margin. If the resistance margin is set at a high value, the lifetime of the PCM cell is also high. The tolerance to drift of the proposed method is excellent and different from [7]. It does not show a significant dependency on T_{off}. For a T_{off} of 15 years, a PCM cell (with 4 levels and a 1% write region) has an average percentage accuracy of 98.047% using the proposed method. This is significantly better than [7] in which the same PCM cell can tolerate the drift behavior of only 2 years. One of the reasons for this improvement is that the threshold resistance in the proposed scheme increases with time, while the threshold resistance of [7] remains unchanged.

E. Comparison

Next, the proposed threshold resistance selection method is compared with the time aware fault-tolerant scheme of [3]. [3] monitors the PCM memory and its lifetime using time tags; the lifetime information is utilized to adjust the quantization of the memory cell resistance and for ECC decoding. The quantization and analysis of the PCM resistance at each level require to consider the lifetime (t_d) and to perform complex calculations. Additional circuits are needed to calculate t_d, establish the relationship between the lifetime and the resistance drift and finally calculate the new values of the resistance for each PCM cell. Moreover, the lifetime of a PCM [3] is limited by the number of bits that are used to represent the time tag, i.e. if the number of bits is low, the lifetime estimate of [3] is not very accurate. The proposed method uses the PCM resistance as lifetime of the whole PCM array, only the median circuit is required to find the threshold resistances.

VII. Conclusion

This paper has proposed a system-level scheme for alleviating the resistance drift in a multilevel phase change memory (PCM). The proposed scheme relies on separating the levels of a PCM cell and checking the correctness of the stored data in the presence of drift. The effects of time are assessed and a solution based on calculating the median value is proposed. The resistance of a PCM cell is initially divided into three regions (write, read, and blank) to account for the correct write/read operations as well as the drift. The percentage accuracy of a level of the PCM has been considered and balanced between levels to generate the so-called *flat initial level separation*. Compared to the other approaches found in the technical literature [3][7], it has been shown that the proposed method is significantly simpler than [3], because only the median calculation circuit is required to find the PCM resistance at each level. Moreover it is significantly better than the approach of [7] in which the margin of PCM resistance at each level is predefined, thus having a limited tolerance to the resistance drift.

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