An Ultra-Low-Power Imperfect Transmission Gate Flip-Flop for Near-Threshold Voltage Operation

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***Abstract*—Flip-flops (FFs) are essential building blocks in digital circuits, contributing a significant portion of dynamic power while impacting performance, area, and robustness under process, voltage, and temperature (PVT) variations. Among various designs, the transmission gate flip-flop (TGFF) composed of two latches is widely used for its reliability and static operation; however, its dual-phase clocking system operates with high dynamic power even when data remain unchanged. In this paper, an Imperfect Transmission Gate Flip-Flop (ITGFF) is proposed to reduce redundant clock transitions and the transistor count by removing the keeper circuits in both latches. A selective clock optimization technique is introduced to deactivate the inverted clock when the input and output are identical. The ITGFF consists of 16 transistors, including 6 clock transistors. Post-layout simulations in a 45-nm CMOS technology show that the ITGFF achieves a 74.86% (or 77.78%) reduction in the power-delay product compared to the TGFF at a supply voltage of 1 V (or 0.6 V) and a 1 GHz (or 50 MHz) clock frequency, with a 10% data activity ratio. The application in a 32-bit shift register illustrates its effectiveness in low-activity sequential circuits with regular clock operation. This design also demonstrates robust operation under PVT variations, enabling reliable functionality at a supply voltage as low as 0.4 V without any functional failure.**

***Index Terms*—Flip-flop, Near-threshold voltage, Selective clocking**

I. Introduction

Flip-flops (FFs) are fundamental in digital integrated circuits, providing temporary data storage in register files and the control logic of microprocessors. They are also an integral part of the clock system, responsible for 60% of the overall power. Specifically, FFs and latches account for 84% of the clock power or 50% of the total power in a chip [1] due to their clock-driven switching activity. Since energy efficiency is one of the primary design objectives for edge computing and Internet of Things (IoT) devices, near-threshold voltage (NTV) operation has become a potential solution for low-power circuit design. However, NTV operation is sensitive to process, voltage, and temperature (PVT) variations, making conventional FFs unreliable at low supply voltages.

To reduce power, several circuit-level strategies have been applied, including lowering the supply voltage, reducing the number of clock transistors, eliminating redundant internal transitions, and minimizing contention between the pull-up and pull-down networks. However, each strategy comes with different trade-offs. Fully static and contention-free FFs, such as the Transmission Gate FF (TGFF) and Static Contention-Free Single-Phase-Clocked FF (S2CFF) [2] run robustly at lower voltages; however, the keeper circuits and additional transistors introduce a large effective clock load (i.e., increased clock capacitance) and cause redundant toggling even when the input (D) and output (Q) are not changing [3]. On the other hand, FFs with reduced transistor counts, such as the 18-transistor True Single-Phase clocked FF (18TSPC) [4], Topologically-Compressed FF (TCFF) [5], and Very Low-Power FF (VLFF) [6], rely on ratioed logic and cause contention issues, which degrade their performance in NTV operation under PVT variations.

No single approach can simultaneously meet all the following conditions: (1) a low clock load, (2) a low transistor count, (3) robustness at NTV, and (4) minimal internal switching activity. Fully-static FFs are robust in NTV; however, they require a large number of transistors to deliver a static operation. Dynamic designs fail to deliver a robust performance in NTV, although they require fewer transistors to operate. Hybrid approaches partially reduce internal switching activities but still suffer from reliability issues at NTV. Hence, a balanced approach is needed to meet all these potential requirements, and at the same time, to lower the power consumption.

On the other hand, approximate computing has emerged as an energy-efficient paradigm for applications, in which some errors can be tolerated for substantial gains in performance or energy efficiency [7]. While approximate combinational circuits (e.g., adders and multipliers) have been extensively investigated, approximate sequential circuits remain largely unexplored, including FFs. The exploration of imperfect FFs provides another approach to the reduction of redundant internal switching activities within FFs, while maintaining functionality with a great potential for clock power and energy reduction.

Motivated by these observations, we propose an ultra-low-power imperfect TGFF (ITGFF), in which the feedback circuits in both latches of the TGFF are removed to create an imperfect energy-efficient structure. A selective clock optimization logic reduces the redundant clock inversions, similar to charge-sensing and redundancy-eliminating FFs [8], but implemented in a simplified way in the transmission gate architecture. Despite having six clock transistors, higher than some static FFs except the TGFF, the ITGFF achieves a significant reduction in power by optimizing the clock

network. To the best of the authors' knowledge, this work introduces the first imperfect TG-based FF design, targeting low-activity sequential circuits with regular clock operation for potential applications in image-processing hardware, low-power sensor systems, and deep-learning accelerators.

The rest of the paper is organized as follows: Section II briefly reviews the background and state-of-the-art single-edge triggered FFs. Section III outlines the design and operation of the proposed Imperfect TGFF. Section IV discusses the simulation results, and Section V concludes the paper.

II. State-of-The-Art FFs

There are several methods for the design of energy-efficient FFs through voltage scaling, transistor minimization, and clock optimization. Each method offers different benefits and introduces various design trade-offs. One of the major approaches to power reduction is to reduce the supply voltage to NTV. The operational robustness at NTV has become a performance measure for circuit design. However, operating at NTV becomes a major challenge for FFs. The FF needs to be static and contention-free. The redundant transistors of the internal nodes should be minimized as the clock transistors [3].

The TGFF remains a widely accepted NTV-compatible industrial design since it provides full-swing robustness, predictable timing, and PVT resilience. However, the dual-phase clock inversion of the TGFF produces redundant clock switching even when the data remains unchanged. In low-activity designs, where the data activity ratio is between 10% and 25% [5], the redundant inversion introduces a substantial dynamic power overhead.

Researchers have used three major techniques to reduce power. One is to reduce the clock transistor count. Lowering the number of clock transistors can reduce the clock load and clock power. The Adaptive Coupling Flip-Flop (ACFF) [9] reduces the clock transistor count to 4; however, it suffers from contention in the secondary latch. Also, the ACFF uses only PMOS or NMOS transistors on the transmission path, which is dynamic in nature. In the VLFF [6] and Three-Clock Transistor True Single Phase Clocked FF (3CTSPC) [10], ultra-low power is achieved by reducing the clock transistors to two and three, respectively. However, these FFs are susceptible to PVT variation in NTV.

Since data activity is low in modern chips, the second method to reduce power in an FF is to eliminate the redundant clock transitions. Removing the unnecessary toggling of internal clocked nodes can dramatically reduce the power consumption of an FF. Both the SC2FF [2] and 18TSPC FF [4] partially remove redundant transitions. However, the 18TSPC FF suffers from contention and the dynamic behavior of internal nodes. The Robust Redundant-Free Flip-Flop (RRFF) [11] and Fully Static Contention-Free Flip-Flop [12] rely on extra transistors to fully remove internal transitions to achieve ultra-low power consumption.

The third method is to eliminate the redundant transistors through both topological and logical optimizations, as in the TCFF [5] and the Redundancy Eliminated FF (REFF) [13]. The TCFF reduces the transistor count to 21; however, charge-sharing and contention affect the reliability at NTV. The REFF removes redundant transistors and transitions to improve power efficiency and achieve a full-static NTV operation, but with noticeable circuit overhead.

III. Imperfect TGFF Design

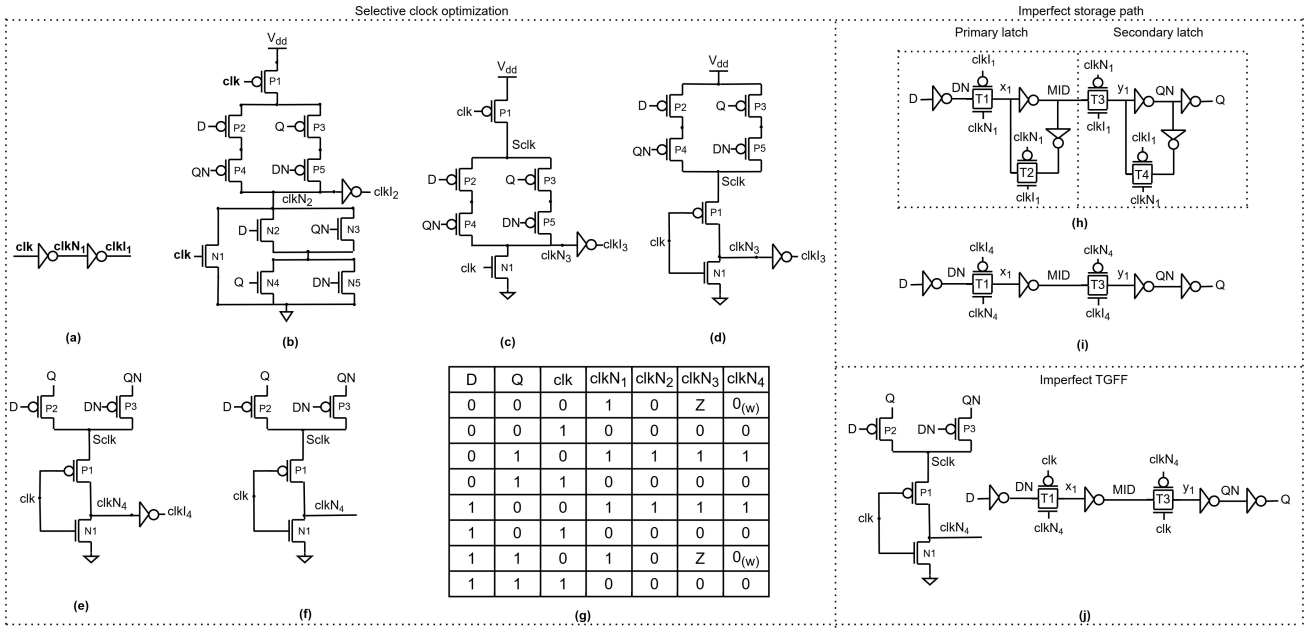
The conventional TGFF consists of a data storage structure and a clock inversion network. Approximations in the TGFF can be done in several ways. In this paper, we focus on reducing the keeper circuit in the data storage structure. Furthermore, a selective clock-optimization circuit is proposed to reduce the unnecessary switching of inverted clock signals in the TGFF.

A. Selective Clock Optimization

The conventional TGFF employs dual-phase inverting clock signals ($clkN_1$ & $clkI_1$) to control the transmission gates in the storage path (Fig. 1(a)). Due to a low data activity ratio in most cases, the FF remains idle. Therefore, the unnecessary switching activity of complementary clock signals becomes a major drawback of the TGFF. To address this issue, a selective clock optimization technique is proposed in Fig. 1 (b-f). In this technique, clock inversion is disabled when the input and output signals remain unchanged. To achieve this, an XOR-based detection circuit is used to check the relation between D and Q. When the D and Q signals of the FF are the same, clock-signal inversion is disabled. When D and Q are different, the *clk* signal is inverted, allowing the normal data propagation through the FF. Fig. 1(b) illustrates a CMOS implementation of the selective clock optimization technique according to the Boolean expressions below:

$$\begin{aligned} clkN_2 &= (D \oplus Q) \cdot \overline{clk} \\ &= (\overline{D} \cdot Q + D \cdot \overline{Q}) \cdot \overline{clk} \\ &= (DN \cdot Q + QN \cdot D) \cdot \overline{clk}, \quad [QN = \overline{Q},\ DN = \overline{D}] \\ clkI_2 &= \overline{clkN_2}. \end{aligned} \tag{1}$$

The CMOS selective clock optimization is fully static and ensures a full swing output. However, it incurs high dynamic power and requires 10 transistors to generate $clkN_2$. The pull-down network (PDN) of the clock optimization is activated when *clk* is high. Since the clock-controlled path shows higher switching activity than the other parallel PDN paths, an intentional imperfection is introduced to simplify the PDN. Specifically, some selected discharge paths are removed to reduce the complexity of the circuit. The simplified structure is shown in Fig. 1(c). In the original PDN structure, the clock transistor *N1* forms a parallel conduction path with *N2*-*N4* and *N3*-*N5*. In the pull-up network (PUN) in Fig. 1(c), $clkN_3$ will be logic 1 only when D and Q are different. When the clock is logic 1, $clkN_3$ will become logic 0. By eliminating redundant parallel branches (*N2*-*N4* and *N3*-*N5*), the number of stacked devices in the discharge path is reduced, resulting in a smaller and faster PDN. With this imperfection, four transistors are



D	Q	clk	clkN$_1$	clkN$_2$	clkN$_3$	clkN$_4$
0	0	0	1	0	Z	0$_{(w)}$
0	0	1	0	0	0	0
0	1	0	1	1	1	1
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	1	0	1	0	Z	0$_{(w)}$
1	1	1	0	0	0	0

Fig. 1. Proposed ITGFF with selective clock optimization: (a) The clock network of TGFF. (b) A CMOS implementation of the selective clock optimization technique. (c) A reduced pull-down network with a lower transistor count. (d) Reordered PMOS structure using series equivalence. (e) Modified structure eliminating high-impedance states at node S_{clk}. (f) The final simplified clock optimization structure with reduced clock inversion circuitry. (g) Functional verification of internal clock signals for different input conditions (Z: a high-impedance state, 0_w: weak 0). (h) Data storage structure of the conventional TGFF. (i) Proposed ITGFF data storage structure. (j) Proposed ITGFF.

eliminated, simplifying the overall circuit. However, in this structure, the clock transistor *P1* is directly connected to V_{DD}. When *clk* is low, *P1* turns on and precharges the intermediate node S_{clk}. Since *D* and *Q* are identical most of the time, the precharged value neither produces a transition at $clkN_3$, nor contributes to a functional output change, resulting in excessive switching energy. To mitigate this issue, the position of the clock-controlled PMOS transistor is rearranged, as shown in Fig. 1(d). In the modified structure, the branches *P2-P4* and *P3-P5* are connected in parallel, with their sources connected to V_{DD}. As a result, the internal node S_{clk} is no longer precharged in every clock cycle. Instead, the node is precharged when *D* and *Q* are different, improving power efficiency. Although the circuit in Fig. 1(d) preserves the intended logical functionality with imperfection, $clkN_3$ enters a high-impedance state when *clk* = 0 and *D* = *Q*. In this state, neither PUN nor PDN drives the node, causing the $clkN_3$ node to float. Floating nodes in FF can lead to several undesirable effects, including leakage-induced voltage drift, increased noise susceptibility, and potential logic uncertainty; therefore, they are avoided in FF design. To eliminate them, the circuit is further refined as shown in Fig. 1(e). In this design, the XOR evaluation network is reorganized so that the S_{clk} node is actively driven through data-controlled pass-transistor paths. The circuit selects *Q* and *QN* signals directly depending on the value of input *D*. The logical expression of S_{clk} can be written as:

$$\begin{aligned} S_{\text{clk}} &= \overline{DN} \cdot QN + \overline{D} \cdot Q \\ &= D \cdot QN + DN \cdot Q = D \oplus Q. \end{aligned} \tag{2}$$

This modification ensures that the S_{clk} node is always driven during operation, which eliminates the floating nodes and maintains a simplified circuit. The inverted clock signal for this modification is denoted $clkN_4$ in Fig. 1(e). However, this simplified version introduces imperfections, as a PMOS transistor is not ideal for driving logic 0. Therefore, $clkN_4$ may deliver a weak logic 0 under certain conditions. The final modification can be made by removing the $clkI_4$ signal from the circuit (Fig. 1(f)). Since $clkN_4$ already produces the required inverted clock, the $clkI_4$ signal can be removed without affecting functional correctness. This reduces the number of clock transistors, thus lowering clock-related dynamic power consumption and decreasing propagation delay.

B. Imperfect Data Storage Structure

The data storage structure of TGFF contains two latches, referred to as primary and secondary latches (Fig. 1(h)). Each latch includes a storage path implemented by a transmission gate (TG) and an inverter as well as a feedback path composed of an inverter and an additional TG. In both latches, TGs are controlled by complementary clock signals ($clkI_1$ and $clkN_1$). For a positive-edge-triggered FF, the primary latch conducts data transmission when *clk* is low and holds the intermediate value *MID* when *clk* is high. The secondary latch transmits the data when *clk* is high and keeps the signal when *clk* is low.

At high clock frequencies, the primary latch holds the *MID* signal for a short duration. For instance, at a clock frequency of 1 GHz (*clk period* = 1 ns), the primary latch transfers the data from *D* to *MID* within 500 ps and holds the *MID* signal for the remaining 500 ps, allowing correct

transmission to the secondary latch. This short duration makes the function of the keeper circuit less important in modern circuits. In the proposed design, the keeper circuit in the primary latch is simplified to reduce the circuit complexity and improve performance. Instead of using a strong feedback loop, the data is temporarily stored by the parasitic capacitance of the intermediate storage node (Fig. 1(i)) for *MID*. The data storage structure is further simplified by reducing the feedback loop of the secondary latch, specifically eliminating the transmission gate *T4* and its associated keeper inverter. During the opaque phase, the secondary latch relies on the capacitive storage at node *y1* for half a clock cycle. Although this introduces an imperfect storage behavior compared to the conventional TGFF, the circuit remains functional because the internal node retains its state for only half a clock cycle before being refreshed, while the subsequent inverter stages restore the signal to a full swing. Additionally, $clkI_4$ is replaced by the *clk* signal, reducing unnecessary transitions. The main clock signal periodically refreshes the internal nodes before significant leakage-induced drift affects the output. This structural simplification significantly reduces the total transistor count, leading to lower switching capacitance and improved power efficiency. The overall transistor count is 16 for ITGFF, including 6 clock-controlled transistors.

C. Operation of the ITGFF

Fig. 1(j) shows the schematic of the ITGFF. When the data input D changes from logic 1 to logic 0 while the previously stored output $Q = 1$ and $clk = 0$, the selective clock network detects a data transition ($D \oplus Q$) and drives $clkN_4$ to become logic 1. The TG *T1* is on, and the input data propagates through the primary latch, making the internal node *MID* become logic 0. The secondary latch is in the opaque stage, which means *T3* is off and the node *y1* holds its previous value (logic 1) for a half clock period. At the rising edge of the clock, $clkN_4$ becomes logic 0. *T1* turns off, and the primary latch is in the opaque stage for a half clock period. At the same time, the TG *T3* turns on, allowing the *MID* signal to propagate to node *y1* and subsequently to the output Q. The output Q transitions from logic 1 to logic 0.

When the input and the stored output are the same ($D = Q = 0$), the $clkN_4$ signal remains at logic 0. The PMOS transistors in the TGs in both primary and secondary latches will be turned on. Hence, the TG is partially on and will be passing strong logic 1 and weak logic 0. However, since both the input and output are with the same logic value, no functional error occurs. The weak logic 0 having passed through *T3* is restored to full swing through the subsequent inverter stages. At the rising edge of the clock, *T1* will turn off while *T3* turns fully on. The node *y1* will be refreshed by the stored *MID* signal, and the output Q will remain unchanged.

When $D = 1$ and the previously stored output $Q = 0$, the selective clock network detects the data transition. When the clock is logic 0, the $clkN_4$ signal will become logic 1. *T1* will be turned on, and the *DN* signal will propagate to node *x1*. During this period, *T3* remains off, and node *y1* holds its previous value through parasitic capacitance. At the rising edge of the clock, $clkN_4$ becomes logic 0. *T1* turns off and holds the value at the node *x1* and the *MID* signal. Simultaneously, *T3* turns on and transfers the updated *MID* signal to node *y1*, causing the Q output to change from logic 0 to logic 1.

When D and the previously stored output Q are both logic 1, $clkN_4$ will become a weak logic 0 while the clock remains low. Under this condition, both *T1* and *T3* are partially conducting. However, since both input and output nodes already hold the same value, this configuration does not introduce any error. At the rising edge of the clock, *T3* turns on and refreshes *y1* from *MID*. The output, therefore, remains at logic 1.

IV. Simulation Results

All post-layout simulations are conducted in Cadence using a 45-nm CMOS technology. For a fair comparison, all flip-flop designs listed in Table I are implemented and evaluated using the same technology node and simulation setup. The PMOS-to-NMOS width ratio is kept at 2:1 unless design-specific sizing optimization is required. For the testbench, the inputs (D and *clk*) are connected to two chained inverters, and the output node is connected with four parallel inverters to simulate a real-time scenario. The supply voltage is varied from 1 V to 0.4 V to evaluate the circuit performance across different voltage regions. The temperature is set to 27°C. Additionally, the clock frequency is variable with regard to the supply voltage. At a nominal voltage, the clock frequency is 1 GHz, while at an NTV (0.6 V), the clock slows down to 50 MHz. At a sub-threshold voltage (0.4 V), the clock frequency is set to 1 MHz for optimal performance for most of the FFs.

Table I presents an overall post-layout comparison of the considered FFs and the proposed ITGFF. The comparison includes structural characteristics such as the transistor count, the number of clock transistors, contention-free operation, and layout area, followed by timing and power metrics under two operating conditions: nominal (1 V, 1 GHz) and NTV (0.6 V, 50 MHz) at the typical-typical (TT) process corner. The ITGFF consists of 16 transistors, one of the lowest transistor counts among all the FFs, while maintaining a contention-free operation. Although the ITGFF uses more clock-controlled transistors than several static FFs, the proposed selective clock optimization technique suppresses unnecessary clock transitions, thereby reducing clock-related dynamic power. In addition, the layout area of the proposed design is 8.2 μm^2, which is smaller than most conventional designs, such as the TGFF, ACFF, REFF, ULPFF, and RRFF. Although LTCFF and ITGFF have the same transistor count, the ITGFF occupies a slightly larger layout area due to additional routing requirements and fewer opportunities for source/drain diffusion sharing.

Under nominal operating conditions, the ITGFF achieves a clk-to-Q delay of 179.5 ps, shorter than the 189.5 ps delay of the TGFF. Due to imperfections and the selective clock optimization network, the ITGFF needs a long setup time, which increases the D-to-Q delay. However, the measured

TABLE I
OVERALL COMPARISON OF ALL CONSIDERED FLIP-FLOPS

FF designs	TGFF	S2CFF [2]	ACFF [9]	18TSPC [4]	REFF [13]	LTCFF [3]	ULPFF [3]	RRFF [11]	FCFF [12]	Proposed ITGFF
Transistor counts	24	24	22	18	25	16	22	25	25	16
Clock transistors	12	5	4	4	4	4	4	4	5	6
Contention-free	Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Area (μm^2)	9.12	8.8	9.64	8.18	9.88	7.8	9.72	10.06	9.96	8.20
Voltage 1 V, Clock Frequency 1 GHz (TT, 27°C)										
clk-to-Q delay (CQ) (ps)	189.5	203	221	210.5	214.5	187.5	227	191	243.5	179.5
D-to-Q delay (DQ) (ps)	258.89	330	522	316	411	318	384.5	368.578	484	364.96
Setup time (ps)	60.57	117	290	96.31	187	120	160	167.75	229.77	180.2
Hold time (ps)	-13.27	-84.56	-54.34	130	-79.29	23.67	10.79	-83.41	125.51	-32.15
Average power (μW) (DA = 10%)	7.85	2.43	2.37	1.82	1.63	2.17	1.44	1.51	1.69	1.4
PDP_{CQ} (aJ) (DA = 10%)	1487.6	493.3	523.8	383.1	349.6	406.9	326.9	288.4	411.5	251.3
PDP_{DQ} (aJ) (DA = 10%)	2032.3	801.9	1237.1	575.1	669.9	690.1	553.7	556.6	817.96	510.9
Voltage 0.6 V, Clock Frequency 50 MHz (TT, 27°C)										
clk-to-Q delay (CQ) (ns)	2.61	2.33	2.099	2.51	2.43	2.12	2.69	2.13	2.89	1.9
D-to-Q delay (DQ) (ns)	3.91	3.66	5.94	3.72	5.12	3.82	4.46	4.2	5.65	4.22
Setup time (ns)	1.3	1.23	3.8	0.995	1.23	1.58	1.9	1.81	2.6	2.3
Hold time (ns)	-0.09	-0.76	-0.66	1.75	-1.15	0.192	0.105	-1.24	1.7	-0.17
Average power (nW) (DA = 10%)	113.5	41.86	36.14	30.86	27.42	36.84	25.83	25.41	28.49	23.36
PDP_{CQ} (aJ) (DA = 10%)	296.23	97.53	75.85	77.45	66.63	78.10	69.48	54.12	82.33	44.38
PDP_{DQ} (aJ) (DA = 10%)	443.78	153.20	214.67	114.95	140.39	140.73	115.20	106.72	160.96	98.57

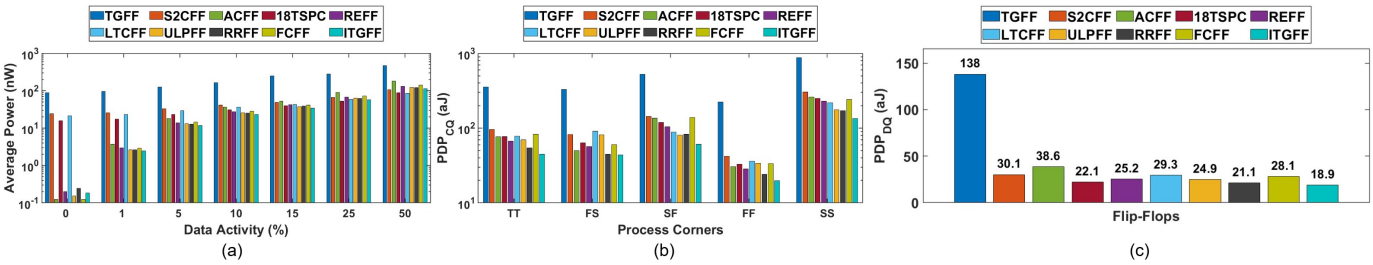


Fig. 2. (a) Average power consumption of various FFs for different data activities at 50 MHz / 0.6 V / TT corner, (b) power-delay product ($\mathrm{PDP_{CQ}}$) of various FFs vs different process corners at 50 MHz / 0.6 V, and (c) power-delay product ($\mathrm{PDP_{DQ}}$) of various FFs at 1 MHz / 0.4 V / TT corner.

hold time of ITGFF is negative, which indicates no hold-time is required after the clock edge; therefore, it is treated as a zero hold time [12]. Moreover, the proposed design consumes the lowest average power (1.4 μW) among all the FFs. Compared with the TGFF (7.85 μW), the ITGFF achieves approximately 82% lower power consumption. In addition, the ITGFF achieves a lower power-delay product (PDP_{DQ}), which represents an approximate 74.86% improvement compared to the conventional TGFF. At NTV, the advantages of the proposed ITGFF become more evident. It consumes only 23.36 nW, which is significantly lower than the 113.5 nW of the TGFF. Moreover, the ITGFF achieves a 77.78% reduction in PDP_{DQ} compared with the TGFF. Overall, compared with the conventional TGFF, the proposed ITGFF reduces the transistor count, average power consumption, and power-delay product while maintaining reliable operation at both nominal and near-threshold voltages.

Fig. 2(a) shows the comparison of the average power of different FFs as a function of data activity factor from 0% to 50%. The average power consumption increases with data activity due to the dynamic switching power. The ITGFF consumes the lowest power on average among all the FFs when the data activity is low. When the data activity reaches 50%, LTCFF, 18TSPC, and S2CFF are more power efficient than the ITGFF. The ITGFF has an internal signal of *DN*, which is an inversion of *D*. When data activity increases, the inversion of *DN* consumes extra power. However, the activity ratio of a modern circuit is less than 25% [5]. Therefore, within

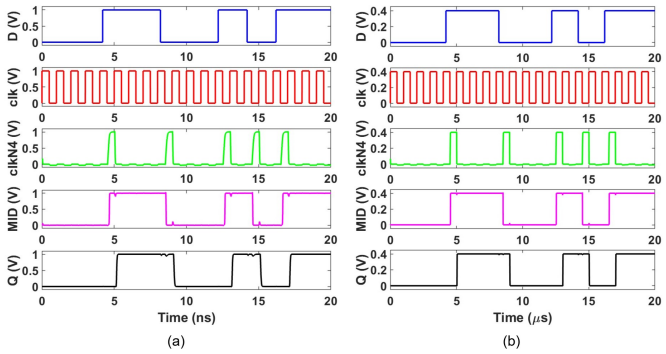


Fig. 3. Transient analysis of the FFs at (a) 1 GHz / 1 V / TT corner and (b) 1 MHz / 0.4 V / TT corner.

this practical operating range, the ITGFF is competitive in power consumption compared to the other designs. Fig. 2(b) illustrates PDP_{CQ} of different FFs across various process corners: TT, Slow-Slow (SS), Fast-Slow (FS), Slow-Fast (SF), and Fast-Fast (FF). The proposed ITGFF shows lower sensitivity to changes in PDP_{CQ} due to process variation, which makes it more reliable across different conditions. Fig. 2(c) shows the PDP_{DQ} of different FFs at the sub-threshold voltage region (0.4 V). The ITGFF achieves an 86.30% reduction compared to the conventional TGFF.

Fig. 3 illustrates the transient analysis of the internal signals, inputs, and output of the proposed ITGFF at the nominal voltage and a sub-threshold voltage. As can be seen from the figure, $clkN_4$ only becomes logic 1 when the *clk* signal is logic

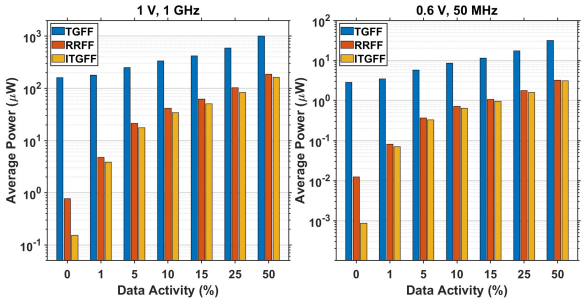


Fig. 4. Average power comparison of 32-bit shift registers implemented using different FFs.

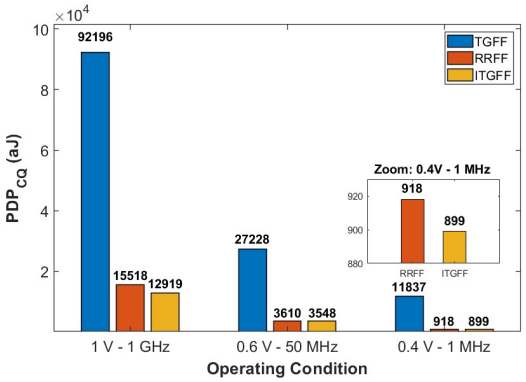


Fig. 5. Power-delay product comparison of 32-bit shift registers under different operating conditions.

0, and D and Q are different. It avoids the redundant clock inversions in the TGFF. The output Q does not contain any voltage degradation at both nominal and sub-threshold voltage conditions. Therefore, it shows a reliable operation at both conditions.

As a practical application of the proposed FF, a 32-bit shift register is implemented using the proposed ITGFF and compared with the conventional TGFF and RRFF. Post layout simulations are performed using extracted netlists in a 45-nm technology at 27°C with variable operating conditions: 1 V / 1 GHz (nominal), 0.6 V / 50 MHz (near-threshold), and 0.4 V / 1 MHz (sub-threshold). Fig. 4 shows the average power consumption of the 32-bit shift register as a function of data activity. We observe that at the nominal voltage, the proposed ITGFF achieves lower power than the TGFF and slightly improves the power compared to RRFF across all data activities. At the near-threshold voltage, all designs show significant improvements in power consumption; however, the ITGFF dissipates the lowest power. Fig. 5 illustrates the PDP_{CQ} of the 32-bit shift register under different operating conditions. At the nominal condition, the ITGFF achieves an 85.9% reduction in PDP compared to TGFF and approximately 16.7% improvement compared to RRFF. At NTV, the ITGFF outperforms the TGFF significantly and provides a marginal improvement over the RRFF. At the sub-threshold voltage, both the ITGFF and RRFF demonstrate a comparable performance, while the ITGFF still achieves the lowest PDP, as shown in the zoomed inset.

V. Conclusion

This paper presents an ultra-low-power, selective clock-optimized Imperfect Transmission Gate Flip-Flop (ITGFF) for operation at near-threshold voltages. In this design, redundant clock transitions and circuit complexity are reduced by leveraging a selective clock optimization network and the removal of the keeper circuits in both latches. Based on a compact structure of only 16 transistors, including 6 clock transistors, the ITGFF achieves a contention-free operation with controlled dynamic behavior. Post-layout simulation shows that it achieves reductions of 74.86% in PDP_{DQ} at the nominal voltage and 77.78% at a near-threshold voltage, compared to the conventional TGFF, while maintaining a reliable operation across process variations. An application using a 32-bit shift register shows that the ITGFF achieves the lowest power consumption and the smallest PDP_{CQ} across nominal, near-threshold, and sub-threshold operating conditions.

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