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On the Restore Operation in MTJ-Based Nonvolatile SRAM Cells

Ke Chen, Jie Han, and Fabrizio Lombardi

***Abstract*— This brief investigates the Restore mechanism of a nonvolatile static random access memory (NVSRAM) cell that utilizes two magnetic tunneling junctions (MTJs) as nonvolatile resistive elements and a 6T SRAM core. Two cells are proposed by employing different mechanisms for the Restore operation once the power is reestablished. The proposed cells use the bitline and supply as mechanisms to initiate the Restore operation, so connecting the two MTJs to different nodes of the NVSRAM circuitry. The cells are extensively analyzed in terms of their operations with respect to different figures of merit, such as operational delays (for the Write, Read, and Restore operations), the static noise margin, power consumption, critical charge, and process variations (in both the MOSFETs and the resistive elements). Simulation results show that the cell with the MTJs connected to the supply offers the best performance in terms of power for the Read/Restore operations; it also achieves the best Read delay, but the worst Restore delay.**

***Index Terms*— Instant-ON, magnetic tunneling junction (MTJ), nonvolatile memory, static random access memory (SRAM).**

I. Introduction

Many programmable chips, such as field programmable gate arrays (FPGAs), use static random access memories (SRAMs) as programming technology. However, a SRAM is volatile, so an additional off-chip nonvolatile storage (often flash memories) is required to store the FPGA configuration data during power-OFF [1], [2]. Data transfer between the FPGA and the external nonvolatile memory is slow, so often resulting in a loss of performance for the startup operation. Moreover, the off-chip stored configuration data is vulnerable to external attacks, thus posing a security concern for many applications [3]–[5].

Scaling of CMOS technology has also resulted in an increase in static leakage power. To decrease power dissipation, gating techniques using magnetic tunneling junction (MTJ)-based nonvolatile circuits have been proposed in [6]. When the processor is in an idle state, the data is stored in the MTJ-based nonvolatile circuits and the power supply is cutoff to stop the leakage current. This type of nonvolatile memory cell can also be used in the applications requiring FPGAs; video surveillance, smart grid sensor, or healthcare monitoring systems are some examples of application areas. These applications share a similar feature, namely, a long idle period followed by a short period of intensive processing. The process of restarting processing (also called as the Restore operation) must be efficient to reduce any latency caused by the idle period. Therefore, this memory requires to execute unique operational sequences; once the data is written to both the CMOS-based volatile SRAM and the MTJ-based nonvolatile elements, the memory is powered down (i.e., by shutting down the power supply). When the power is reestablished, the stored data is written from the MTJ-based nonvolatile elements to the SRAM [7].

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In this brief, two memory cells that utilize a complementary configuration consisting of two MTJs (as nonvolatile resistive elements) and a 6T SRAM core are proposed. These nonvolatile SRAM (NVSRAM) cells have the same number of MOSFETs and MTJs (i.e., they are 6T2R), but they implement the so-called Restore operation using different schemes, i.e., they utilize different access mechanisms to Restore the data from the two MTJs to the storage nodes. These NVSRAM cells are assessed in terms of different figures of merit for the performance (Restore as well as Read/Write), stability [the static noise margin (SNM)], tolerance to a single event upset (SEU) (critical charge), and process variations. Simulation results show that the Restore mechanism plays a significant role in the operations of these NVSRAM cells, it must be properly designed at circuit level depending on the performance metrics to be met.

II. Review

A. Magnetic Tunneling Junction (MTJ)

The MTJ is a device made of two ferromagnets separated by a thin insulator. If the insulating layer is thin (typically a few nanometers), electrons can tunnel from one ferromagnet into the other [8]. The direction of the magnetizations of the ferromagnetic films can be switched individually by an external magnetic field; if the magnetizations are in a parallel orientation, it is more likely that electrons will tunnel through the insulating film than if they are in the opposite (antiparallel) orientation. This junction can be switched between two states of electrical resistance (one with low and one with very high values), hence binary storage is accomplished [8]. The resistance of the MTJ depends on the relative orientation of the magnetization directions of the two ferromagnetic layers due to the spin-dependent tunneling involved in the electron transport process between the majority and minority spin states. The Write operation has three approaches: 1) field-induced magnetic switching (FIMS); 2) thermally assisted switching (TAS); and 3) spin-transfer torque (STT). FIMS consists of two perpendicular currents passing above or below the MTJ to generate a magnetic field to change the magnetization direction. TAS uses two currents to accomplish the switching operations; one current passes through the MTJ and heats the storage layer to assist the switching magnetic field generated by the other current. STT exploits the spin-magnetization interaction and requires one low current passing through the MTJ to switch the magnetization of the storage layer. The change in the resistance of the MTJ is measured by the so-called Tunneling Magnetic Resonance (TMR) ratio; this is defined as $\Delta R/R = (R_{\text{high}} - R_{\text{low}})/R_{\text{low}}$. Using an MgO oxide barrier, the TMR ratio is in a range of 70%–500% at room temperature and 1010% at 5 K [9]. However, a range of 70%–200% has been reported recently for the TMR ratio of MTJ-based memories [17], [18]. A TMR ratio of 150% (i.e., a middle range value [17], [18]) is utilized for the MTJ, whereas the 32-nm Hewlett Packard predictive technology model is used for the CMOS transistors at minimum size. As for area, the MTJs are placed on a different plane than the MOSFETs (using stacking). Turkyilmaz *et al.* [12] have reported a MTJ of 100-nm dimension and with an area of 0.02 μm^2. A 6T SRAM cell requires an area of 0.146 μm^2 at 32-nm feature size [20]. Hence, the 6T SRAM has a larger area and, therefore, it is the limiting factor in the density of a NVSRAM. When used for memory design, the MTJ can be modeled by HSPICE for electrical-level simulation. The HSPICE model of a MTJ device has been first proposed in [10]. In this model, a MTJ is considered as a four terminal device; two of the terminals

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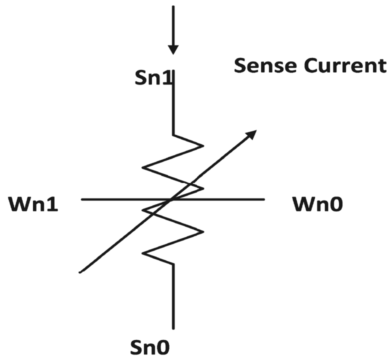

Fig. 1. MTJ.

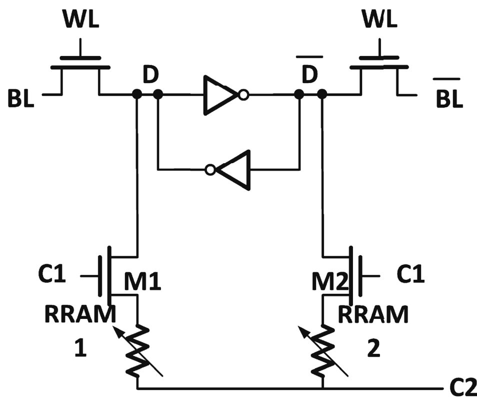

Fig. 2. 8T2R cell of [12].

connect directly to the MTJ resistor (through the sense lines). The other two terminals provide a magnetic bias field for the two basic memory operations (Read and Write), i.e., the word lines. The word and sense lines are not connected; a current through the word line induces a magnetic field on the MTJ, such that its resistance can be changed [and its value is established between the two sense line terminals (Fig. 1)].

The macromodel of [10] has been modified in [11] to solve the so-called convergence problem. This has been achieved by isolating the Schmitt trigger from the input and the output, i.e., the input voltage to the Schmitt trigger is scaled to ensure that its operation is always within a stated limit.

B. Previous Design

Turkyilmaz *et al.* [12] have proposed a memory cell in which two RRAMs are employed as resistive elements (Fig. 2).

The cell of [12] is an 8T2R NVSRAM cell, because it needs eight MOSFETs in a complementary scheme (a conventional 6T SRAM is used as memory core). The two resistive elements are connected to the two data nodes of the SRAM cell through two control transistors (M1 and M2) and are programmed according to the data stored in the SRAM cell. The two elements are always in different resistive states, i.e., when one is in high (low) state and the other is in low (high) state.

During power down, the SRAM loses the stored data, but the two resistive elements store the data due to their nonvolatile nature. When the power is turned ON, the data is written back to the SRAM according to the resistance state of the two RRAMs.

However, its operations are dependent on the type of resistive element that is used; therefore, if a MTJ is used as resistive element, the TMR at room temperature is nearly 150% (5 and 12.5 K are used in this brief), so in the Restore operation, the voltage difference between D and $\bar{D}$ is relatively small.

For the Restore 1 operation of the 8T2R cell [12] at 16-nm feature size, the restored values of D and $\bar{D}$ are 419 and 399 mV, respectively; they are very close and, therefore, the cell is susceptible even to a small amount of noise to change the stored data. The scheme of [12] suffers from many potential problems, hence different complementary schemes are proposed next, when MTJs are utilized as resistive elements.

III. Proposed Cells

The cell of [12] employs two MTJs to implement the Restore operation as well as eight transistors (six for the SRAM core and two additional transistor for access/control); Turkyilmaz *et al.* [12] use a complementary scheme by which the Restore signal is handled through two disjoint RRAMs (each consisting of a MOSFET and a MTJ), i.e., two control signals (C1 and C2) are provided to control the operation of this cell.

Therefore, in this section, different NVSRAM cells that still utilize two MTJs as nonvolatile elements connected to a SRAM core are proposed; these cells differ in the arrangements of the MOSFETs in the circuit, whereas keeping the number of transistors constant to 6. Similar to [12], the scheme is complementary, but the circuitry for a Restore operation and the access mechanism for the MTJs are different in each proposed cell.

In this section, two different types of a 6T2R cell are proposed and analyzed. They are denoted as follows:

1) 6T2R-B [Restore by bitline (BL)];
2) 6T2R-S (Restore by supply).

In these cells, the Restore operation is implemented by different mechanisms, whereas retaining the same number of MOSFETs (i.e., six in the volatile core) and resistive elements (i.e., 2R) in a complementary circuit arrangement.

In this brief, FIMS-based MTJs are employed in the proposed designs; this device is utilized because it does not use a passing current for programming. For example, in the proposed 6T2R-S cell, the MTJ is connected to the SRAM core; in this circuit it is difficult to program a MTJ using a passing current, such as a STT-based MTJ, because the current path is difficult to generate. Moreover, no programming operation can occur in parallel. In the proposed NVSRAMs, both the CMOS SRAM and the MTJs can be written simultaneously by employing FIMS-based devices.

A. 6T2R-B Cell

This cell employs a 6T SRAM core, the two MTJs are connected to the Q and QB nodes of the SRAM through the access transistors T5 and T6 (Fig. 3). The 6T SRAM forms the volatile storage (core) circuit and the MTJs are used to retain the data during power-OFF. Each MTJ is programmed according to the data stored in the SRAM. When the power is turned ON again, the data is written back to the SRAM through BL and $\overline{\text{BL}}$. This cell utilizes the BL as equivalent to an external Restore line; therefore, the BL has two functions: 1) to Write to the SRAM the desired data value and 2) to operate as the external Restore signal.

In the Restore operation, both BL and $\overline{\text{BL}}$ are changed as a single control condition of this cell (so different from [12] in which two external lines are used for access control).

This cell operates according to the following operational features: 1) Write SRAM; 2) Write RRAM; 3) power-OFF; 4) Restore; 5) power-ON; and 6) Read SRAM.

1) In the Write SRAM operation, Write Line (WL) is high to turn ON the access transistors. BL and $\overline{\text{BL}}$ are 1 or 0 according the scenario of writing a 1 or 0.

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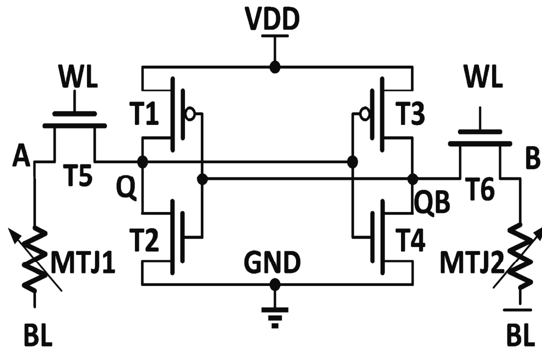

Fig. 3. Proposed 6T2R-B cell.

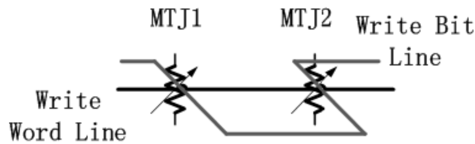

Fig. 4. FIMS MTJ Write circuit.

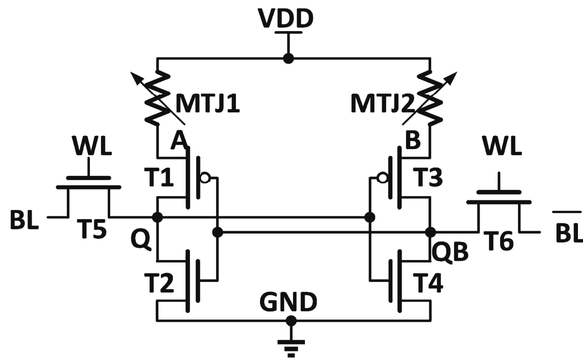

Fig. 5. Proposed 6T2R-S cell.

2) In the Write RRAM (MTJ) operation, the external magnetic field is generated to program the MTJs based on the values of BL and $\overline{\text{BL}}$. As mentioned previously, a FIMS device uses two currents to generate the magnetic field and change the magnetization in the storage layer; therefore, two current sources are required. The two MTJs are in opposite states in the proposed scheme; therefore, one of the two current sources must ensure this condition, whereas providing the appropriate selection in the storage-layer direction, as shown in Fig. 4. When writing a 1, MTJ1 is programmed to a low resistance value state and MTJ2 is programmed to a high resistance value state (the reverse is applicable when writing a 0).
3) During power-OFF, all signals are pulled to the ground.
4) For Restore, both BL and $\overline{\text{BL}}$ are high; WL is turned ON. Since MTJ1 and MTJ2 are in different states, then the voltage values of Q and QB are also different.
5) For power-ON, V_{dd} is again made available; Q and QB are fully restored through the back-to-back inverters.
6) The Read SRAM operation is the same as in a traditional SRAM.

B. 6T2R-S Cell

Another type of a complementary cell is shown in Fig. 5. Its circuit is similar to the 6T SRAM; the difference is that MTJ1 and MTJ2 are connected between the sources of the transistors T1 and T3 and the supply voltage. The difference in resistance values leads to different voltage drops across the MTJs when the power is provided again. The high resistance MTJ has a higher voltage drop than the low resistance MTJ, thus, Q and QB will be restored to the previous correct values. This design has the following objectives.

1) The avoidance in the use of an external control signal. The resistance values of the two MTJs are set during Write operation. If MTJ1 is in a low state and MTJ2 is in a high state, the voltage at the storage node Q rises faster than at QB. The inverse scenario operates similarly for the access transistors. Thus, Restore occurs as soon as the power supply is provided.
2) To reduce power consumption. The operational mechanism of the 6T2R-S cell is similar to a 6T SRAM, the only difference is the addition of the two resistive elements connected to V_{dd}. The Restore operation is directly related to the availability of the supply voltage V_{dd}, thus not consuming additional power.
3) This cell operates according to the following operational features: 1) Write SRAM; 2) Write RRAM; 3) power-OFF; 4) power-ON; and 5) Read SRAM. Therefore, the Restore operation is transparent. All operations are the same as their counter parts in the 6T2R-B cell.

IV. Evaluation

In this section, the two proposed NVSRAM cells are evaluated; delay, power, and process variability are assessed. The default values of the MTJ resistance range are given by $R_{\text{high}} = 12.5$ K and $R_{\text{low}} = 5$ K.

A. Delay

The Read and Write delays are first assessed for the proposed two NVSRAM cells by varying the feature size. Then, the Restore delay is considered, i.e., the delay between the Restore signal and the acquisition of the restored data through the resistive elements. The Restore delay accounts for the latency in the Restore 1 (or 0) operation according to the cell type and the mechanism enabling this operation. For the 6T2R-B cell, the latency between WL and Q is assessed. For the 6T2R-S cell, the latency between V_{dd} and Q is found.

Both proposed cells are symmetrical, so the 1 and 0 operations are the same. The results are shown in Table I. Among the two proposed schemes, the 6T2R-B cell has the larger Write and Read delays, because both MTJ1 and MTJ2 are involved in these operations. For the Restore operation, the delay is caused by the back-to-back inverters; for the 6T2R-S cell, the MTJs are also involved in this operation, thus, the Restore delay of the 6T2R-S cell is larger than for the 6T2R-B cell.

B. Power

The power dissipations of the two proposed NVSRAM cells at different feature sizes and operations are reported in Table II. The 6T2R-S cell shows the best power performance for the Read and Restore operations; the placement of the MTJs between the power supply and the SRAM core transistors reduces dissipation. The 6T2R-B cell requires in general more power, because the two access transistors are always turned ON during the Restore operation, BL (Restore 0) or $\overline{\text{BL}}$ (Restore 1) are discharged by T2 or T4; therefore, the 6T2R-S cell is better for low power applications.

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TABLE I
DELAY OF PROPOSED NVSRAM CELLS

Operation	6T2R-B	6T2R-S
32nm		
Write	63.3ps	28.9ps
Read	46.8ps	23.1ps
Restore	45.9ps	57.7ps
22nm		
Write	55.4ps	23.9ps
Read	34.9ps	20.0ps
Restore	32.6ps	45.8ps
16nm		
Write	48.6ps	20.9ps
Read	28.7ps	16.2ps
Restore	27.2ps	38.6ps

TABLE II
POWER CONSUMPTION OF PROPOSED NVSRAM CELLS

Operation	6T2R-B	6T2R-S
32nm		
Write	5.57μW	5.81μW
Read	2.35μW	1.92μW
Restore	22.9μW	5.81μW
22nm		
Write	3.86μW	4.01μW
Read	1.81μW	1.27μW
Restore	13.3μW	4.01μW
16nm		
Write	2.29μW	2.43μW
Read	1.01μW	0.79μW
Restore	7.6μW	2.43μW

TABLE III
VARIATION PERCENTAGES

Operation	Vth	Leff	Rhigh Rlow		
Write	3%	2%	10%	5%	1%
Read	4%	2.5%	10%	5%	1%
Restore	5%	3%	10%	5%	1%

TABLE IV
VARIABILITY PERCENTAGE ON GLOBAL BEHAVIOR OF NVSRAM CELLS (RESTORE 1 DELAY)

$3\sigma/\mu$(%)		6T2R-B	6T2R-S
32nm			
R	10%	23.5	8.4
	5%	12.4	4.5
	1%	2.2	1.2
Leff		15.0	5.7
Vth		29.8	10.2
22nm			
R	10%	26.3	6.7
	5%	17.4	3.6
	1%	4.4	1.2
Leff		19.6	5.3
Vth		37.8	8.8
16nm			
R	10%	33.9	5.5
	5%	21.5	3.0
	1%	6.5	1.0
Leff		25.7	5.3
Vth		47.2	6.6

TABLE V
VARIABILITY PERCENTAGE ON EACH TRANSISTOR BEHAVIORS OF NVSRAM CELLS (RESTORE 1 DELAY AT 32 nm)

$3\sigma/\mu$(%)	6T2R-B	6T2R-S
Leff		
T1	67.67	5.17
T2	10.32	0.01
T3	45.94	0.65
T4	9.45	0.11
T5	17.93	0.0003
T6	13.62	0.0001
Vth		
T1	67.37	8.27
T2	25.96	0.05
T3	59.21	1.23
T4	15.45	0.33
T5	37.77	0.02
T6	27.41	0.01

TABLE VI
CRITICAL CHARGE OF NVSRAM CELLS (RESTORE 1 DELAY AT 32 nm)

Feature Size	6T2R-B	6T2R-S
32nm	1.06fC	1.12fC
22nm	0.6fC	0.64fC
16nm	0.38fC	0.4fC

C. Process Variations

Process variability for the MTJs and the MOSFETs is evaluated using Monte Carlo simulation. The Restore operations is considered by varying the channel length and threshold voltage as function of the feature size of the transistors [16]; the resistive element resistance is varied according to two percentage values as reported in [13]. The variation percentages are reported in Table III. The simulation results (Table IV) confirm the prior discussion, namely, the 6T2R-B cell has the worst variability. The 6T2R-S cell has the better variability for the resistive elements.

Next, the variability of each NVSRAM cell in every transistor is assessed to establish the so-called critical transistor in the circuit (i.e., the transistor whose variation affects the most a specific performance metric of a cell); as shown previously, the Restore operation for a 1 is considered and Table V shows the simulation results at 32-nm feature size of the MOSFETs.

The simulation results (Table V) show that T1 is the most critical transistor that impacts performance the most during the Restore 1 in both cells. T1 is the transistor that pulls Q to 1 when V_{dd} is reestablished. Conversely, T3 is the critical transistor during Restore 0. The variation of T1 in a 6T2R-B cell causes a percentage variation that is significantly larger than for the remaining transistors. The 6T2R-B cell has the largest variation percentage; the BL connects Q or QB via a transistor and a MTJ (with the MOSFET having a resistance larger than the MTJ). Thus, the variation of the transistor significantly impacts the performance of the cell. The 6T2R-S cell has the least variations in all transistors either than the critical one.

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TABLE VII
NOISE MARGIN OF NVSRAM CELLS

Noise Margin	6T2R-B	6T2R-S
32nm		
WSNM	322.4mV	312.4mV
RSNM	133.9mV	117.3mV
rstSNM	47.2mV	345.3mV
22nm		
WSNM	242.6mV	232.6mV
RSNM	97.6mV	89.3mV
rstSNM	33.5mV	255.6mV
16nm		
WSNM	176.6mV	168.8mV
RSNM	62.2mV	50.9mV
rstSNM	19.8mV	185.6mV

TABLE VIII
8T2R NVSRAM CELL

Metric	32nm	22nm	16nm
Write Delay	27.9ps	22.3ps	17.8ps
Read Delay	23.9ps	20.8ps	16.7ps
Restore Delay	47.2ps	34.2ps	30.5ps
WSNM	332.6mV	261.6mV	185.4mV
RSNM	145.9mV	98.3mV	70.8mV
rstSNM	47.2mV	33.5mV	19.8mV
Write Power	6.51μw	4.93μW	3.03μW
Read Power	2.53μW	1.77μW	1.09μW
Restore Power	24.7μW	15.3μW	7.8μW

D. Critical Charge

The critical charge is a measure to assess the tolerance of a memory cell to a SEU [15], [16]; the critical charge is the least amount of charge at a node of a memory cell, such that the stored data can be changed by a soft error. The storage nodes Q and QB have been found to be the nodes of critical charge in all NVSRAM cells. Table VI lists the critical charge at 32 nm. The worst cases for the two cells occur when there is a current pulse on QB or Q with a specific stored value.

E. Static Noise Margin

Two types of SNM are considered in this brief for the evaluation of the proposed NVSRAM cells: 1) the conventional SNM as applicable to a 6T SRAM core for the Read SNM (RSNM) and Write SNM (WSNM) operations and 2) the noise margins at nodes A and B in the cells are assessed for the Restore operation. This is the noise that a NVSRAM cell can tolerate during the Restore operation and is defined as the Restore SNM, i.e., rstSNM. For the 6T2R-B cells, the rstSNM is the average voltage difference between nodes A and B during the Restore operation.

The simulation results (Table VII) show that the 6T2R-B cell has the weakest Restore operation due to the small range of resistance of a MTJ.

V. COMPARISON

Initially, the 8T2R NVSRAM [12] is evaluated in comparison with the proposed two cells. The simulation results are given in Table VIII. The power dissipation of the 8T2R SRAM cell is the worst among the three cells. The rstSNMs of the 8T2R cell is the same as 6T2R-B, because the Restore operation is same in these two schemes. Compared with the 8T2R SRAM, the 6T2R-S NVSRAM is slower but it dissipates less power, i.e., this is the significant tradeoff between these two schemes. The 8T2R cell has the worst power dissipation; the least power dissipation for the Read and Restore (Write) operations is achieved by the 6T2R-S (6T2R-B) cell.

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