Proposed Approximate Multiplier

- Partial product accumulation
  Each approximate adder can accumulate two rows of partial products into one row.

- Error accumulation
  - Errors can occur at each bit of the tree.
  - The errors are “sparsely” distributed, i.e., very rare to have multiple errors at the same position.
  - At each bit, the errors are accumulated by OR operations, which are approximate with an acceptable accuracy.

- Error reduction
  - The accumulated error vector is added back to the result using an accurate adder.
  - Different number of MSBs of the error signals can be used according to different accuracy requirements.

Delay

- Delay Estimation
  - Using a linear delay model, the delays of a full adder and an approximate adder are 3 and 2 “gate delays.”

  - The delay of the partial product accumulation tree is estimated based on the linear model. There are approximately \( \log_2 n \) layers in the approximate adder and \( \log_2 n \) layers in the Wallace tree.

  \[
  D_{\text{approx}} = [2 \log_2 n + 1] T_g
  \]

  \[
  D_{\text{wallace}} = 3 \log_2 n T_g
  \]

- Experimental Results
  - 16 x 16 approximate and Wallace multipliers are implemented in both FPGA and STM 28nm process.
  - In the FPGA implementation, the proposed design reduces delay by 36.4%.
  - In the ASIC implementation, the proposed design reduces delay by 20%.

Power Consumption

- In the FPGA implementation, the proposed design reduces dynamic power by 44.3%.
- In the ASIC implementation, the proposed design reduces power by 48-69% at 0.1, 0.25 and 1 GHz.

Accuracy Evaluation

- Error rate (ER)

\[
\text{ER} = \frac{M_{\text{RED}} - M}{M}
\]

- Relative error distance (RED) and mean relative error distance (MRED)

\[
\text{RED} = \frac{M}{M_{\text{RED}}}
\]

- Low ER and MRED are achieved if a proper number of bits for error reduction is used.

Conclusion

- A novel approximate multiplier design is proposed using a newly designed approximate adder.
- On a statistical basis the proposed multiplier has a very small error distance and thus a high accuracy.
- The proposed design has a shorter critical path delay and a significantly lower power consumption compared to an exact Wallace multiplier.
- Current work investigates a new error accumulation scheme with higher accuracy and an accurate operation mode with full error recovery.

Acknowledgements

References

[1] Han and Orshansky, 2013, IEEE ETS.