A Novel Gate Grading Approach for Soft Error Tolerance in Combinational Circuits

Mohammad Saeed Ansari
Department of Electrical and Computer Engineering
University of Alberta, Edmonton, Canada
ansari2@ualberta.ca

Ali Mahani
Department of Electrical and Computer Engineering
Shahid Bahonar University of Kerman, Kerman, Iran
amahani@uk.ac.ir

Jie Han
Department of Electrical and Computer Engineering
University of Alberta, Edmonton, Canada
jhan8@ualberta.ca

Bruce F. Cockburn
Department of Electrical and Computer Engineering
University of Alberta, Edmonton, Canada
cockburn@ualberta.ca

***Abstract*— Continuous reduction in the minimum feature size of semiconductor devices and the supply voltages in advanced VLSI logic circuits has made those circuits more susceptible to soft errors. Hence, several fault tolerance techniques have been proposed in the literature to protect combinational circuits against single event transients (SETs). These fault tolerance techniques are based mainly on hardware redundancy and therefore they come at the cost of significant area and power overhead. In this paper, a novel gate grading approach is proposed to prioritize gates based on their influence on the circuit's reliability. Specifically, different masking factors are taken into account and the gates with the lowest masking capabilities are identified so that they can be hardened first. Since the gates with higher priorities affect the circuit's reliability more significantly, protecting those gates increases the circuit's reliability with the least required area and power overhead.**

***Keywords*— Logic Circuit, Soft Errors, Fault Tolerance, Transient Errors, Reliability, Logical & Electrical Masking**

I. INTRODUCTION

As technology scales down, logic circuits consume less power and operate at higher frequencies, while they become more susceptible to transient errors [1-5]. In order to protect circuits against single event transients (SETs), different mitigation techniques have been proposed in the literature. These techniques can be classified into three main categories:

- Fabrication process based techniques such as epitaxial CMOS processes and silicon-on-insulator (SOI): in these approaches, the SETs are not eliminated, but the effects of SETs are reduced [6, 7].
- Architectural techniques: these techniques are based on logic redundancy, such as the triple modular redundancy (TMR), the best known fault tolerant approach. Since these approaches are applicable to most digital circuits, they are frequently used in reliable circuit design [8].
- Recovery based techniques: these are based on recovering the previous fault-free system state after an error has occurred [9].

Among all these techniques, architectural techniques and especially TMR have become the most common methods for protecting a circuit. However, despite the advantages of architectural techniques, they suffer from relatively high area and power cost. Since many applications cannot accept this high cost, there is a growing need for novel low overhead solutions in order to meet the demands of designing highly reliable circuits.

According to the *Pareto* principle (the 80–20 rule) [10], for many events almost 80% of the effects come from only 20% of the causes. Consequently, for an efficient circuit design, only the optimal amount of redundancy should be added. Hence, different partial and selective approaches have been proposed in the literature, where the most vulnerable parts of a circuit are protected such that the greatest improvement in reliability is achieved with minimal extra cost.

A common group of error mitigation techniques are ad hoc techniques that utilize system knowledge such as the built-in redundancy in a circuit [11]. Although they provide good protection level with a more efficient implementation, they require a significant design effort.

Selective TMR is another effective approach for improving a circuit's reliability with the lowest possible overhead [12]. The main concern in this technique is to find the best candidates to be protected. Therefore, different gate grading approaches have been proposed. The authors in [13] propose using progressive modular redundancy to improve a circuit's reliability. In order to find the most vulnerable gates to be hardened using TMR or even higher orders of redundancy, the reliability of each gate is increased by Δq, and then they examine to see which gate results in the largest improvement on the overall reliability. The main drawback of this approach is that the unreliability of other gates changes the effect of each gate on the overall reliability.

Another approach that is capable of finding the most critical parts of a circuit is proposed in [14]. The authors used partial truth tables (called signatures) at each node to compute the effective parameters on the soft error rate (SER). Taking advantage of these signatures, an approach was proposed to find the critical nodes of a circuit. A drawback of this approach is that it does not update the signature at other nodes when redundancy is added to the circuit.

A block grading approach is proposed in [15] in which the authors introduce the use of sensitivity and eligibility measures. Eligibility is determined by increasing the reliability of each block and observing which one has the most significant effect on the global reliability. On the other hand, sensitivity deals with logical masking such that more sensitive gates have lower logical masking capabilities. The two measures introduced in [15] may thus grade a circuit's components differently.

In this paper, we propose a novel gate grading approach by considering both logical and electrical masking factors. The remainder of this paper is organized as follows. Section II introduces the proposed scheme and discusses the grading methodology. Section III gives the simulation results and, finally, Section IV concludes this paper.

II. PROPOSED SCHEME

In general, there are three masking factors: electrical masking, logical masking and temporal masking. In combinational circuits, temporal masking is not applicable, so the other two factors are considered in the proposed approach. The logical masking factor is independent of technology and it only depends on the circuit structure, while the electrical masking factor, as described below, takes into account the effects of technology.

A. Logical Masking

A glitch might not propagate to a circuit's primary outputs (POs) because a gate on its path may prevent a logical transition on the gate's output due to an off-path input. For instance, if an input to an AND gate is 0, then the glitch on the other input is logically masked. To compute the logical masking factor of a gate, we apply all the possible input patterns to the circuit. For each input pattern, we negate the gate's output (i.e., by fault injection) and then we check if any of the POs changes. If all the POs are fault-free, then the fault is said to be masked; otherwise there is an output error. The ratio of the number of masks to the total number of experiments gives the logical masking factor. Thus, the logical masking factor LM is given by:

$$LM = \frac{m}{T}, \tag{1}$$

where m is the total number of masks and T is the total number of experiments. For a circuit with n inputs, T is up to 2^n. Thus, T grows exponentially with n in an exhaustive simulation of the circuit, which restricts the analysis to circuits with a limited number of inputs (say less than 30). However, this is a common issue in circuit reliability analysis. In practice, random sampling of input vectors can be used in the simulation to give estimates of the reliability.

Using the definition in (1) for the logical masking factor, gates with a lower LM should be hardened first. However, this gate ordering may change when the electrical masking factor is taken into account, as discussed next.

B. Electrical Masking

A transistor's slower switching time causes the rise and fall times of the generated glitch to increase, which leads to additional circuit delay. On the other hand, a glitch with a short duration may be attenuated since a slow gate may start to turn off before the output reaches its full amplitude. These two effects reduce the duration of a glitch and make it less likely to cause an SET. It is worth mentioning that this effect cascades from one gate to another such that more gates on the path lead to a higher electrical masking capability [16].

The effects of electrical masking become more important in deep submicron technologies because of the reduction in node capacitances and supply voltages. Hence, we compute the electrical masking rate, EM of each gate and combine the two factors, EM and LM, to obtain a more accurate model.

As discussed in [16, 17, 18], the duration of the generated glitch depends on the delay of the gate that is driving the node. The glitch duration at the output of the gate, w_o, can be approximated as

$$w_o = \begin{cases} 0 & if \quad w_i < d \\ 2 \times (w_i - d) & if \quad d < w_i < 2 \times d \\ w_i & if \quad w_i > 2 \times d \end{cases}, \tag{2}$$

where d is gate delay and w_i is the input SET pulse duration. As can be seen in (2), a faster gate (with a smaller d) behaves worse with respect to glitch propagation. In other words, a slower gate has better glitch attenuation characteristics. Consequently, in order to perform an accurate analysis, we need to consider different gate types. Hence, we implement all the gates in the SPICE simulator to have an accurate value for d. Equation (2) can be interpreted as follows: small SET pulses at the gate inputs are likely to be eliminated and they do not propagate to the output, while large SET pulses are likely to be propagated to the output without any distortion in their probability density function (PDF). Otherwise, a shifted and scaled SET pulse at the inputs will be propagated to the output.

Considering the model of (2), we can perform a thorough analysis for every gate's electrical masking factor. In fact, we can generate SET pulses at the output of each gate and then check if it propagates to at least one of the circuit's outputs or not. Again, the ratio of the number of masked cases to the total number of experiments for different input patterns gives the electrical masking factor EM. To speed up the simulation, the electrical masking analysis is done only on the input patterns that do not logically mask the glitches. Then merging the electrical and logical masking factors more accurately determines the gate's significance in a combinational circuit.

III. SIMULATION RESULTS

Three benchmark circuits were implemented in MATLAB and all 2^n possible input patterns were applied to the circuits to compute each node's logical masking factor. However, not all possible input patterns need to be considered when analyzing

the electrical masking factor. Only if the generated glitch is not logically masked should we check if it is electrically masked or not. Hence, we generate SET pulses only for the input patterns that do not logically mask the SET. In order to generate the appropriate SET pulses, we first implemented all the logic gates in a SPICE simulator using a 32-nm predictive technology model (PTM) to compute each gate's delay. Then using MATLAB, we performed Monte Carlo Simulations (MCSs) with 10000 iterations to increase the accuracy. For each non-logical-masking input pattern, 10000 SET pulses were generated with different durations. To generate these 10000 different SET pulses, we used a normal distribution with the mean value (μ) set equal to the gate delay (d) and a variance (σ^2) of 1.

We note that although the EM factor of each gate changes as μ and σ^2 vary in the normal distribution, the importance of that gate does not change with respect to electrical masking and in relation to those of other gates. We extracted the results of the proposed scheme for the benchmark circuits. Table 1 shows the characteristics of each of these circuits [15, 19].

Table 1. Benchmark circuit characteristics

Circuit	Characteristics		
	Gates	PIs	POs
C17	6	5	2
NAND-only Full Adder	9	3	2
74283	40	9	5

We computed each gate delay in SPICE and used the extracted value in a MATLAB simulation. Note that the gates directly connected to at least one of the POs are not considered in the grading since they cannot mask any error and the SET pulse will be propagated to the output. The hardening of the critical gates at the last layer is discussed in [20]. The masking results and the gate grading for each benchmark circuit are shown below.

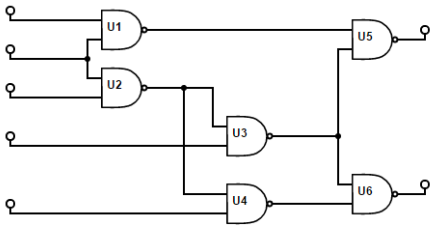

Fig. 1. Schematic of the benchmark circuit C17

Fig. 1 shows the schematic of the C17 benchmark circuit and Table 2 provides the masking factors for each gate in this circuit. The schematic for the NAND-only full adder is depicted in Fig. 2 and Table 3 gives its logical and electrical masking analysis results. Also Table 4 shows the masking factor for different gates in the TTL benchmark circuit 74283, which is depicted in Fig. 3.

Table 2. Gate grading for the benchmark circuit C17

Gate	LM	EM	Priority
1	0.3750	0.0140	3
2	0.2500	0.0204	2
3	0.0625	0.0140	1
4	0.3750	0.0143	4

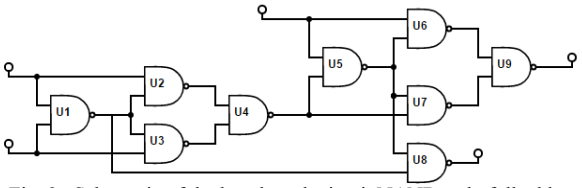

Fig. 2. Schematic of the benchmark circuit NAND-only full adder

Table 3. Gate grading for the benchmark circuit NAND-only full adder

Gate	LM	EM	Priority
1	1.0000	0.0319	7
2	0.3750	0.0301	3
3	0.3750	0.0301	3
4	0.6250	0.0245	6
5	1.0000	0.0118	5
6	0.7500	0.0111	2
7	0.3750	0.0111	1

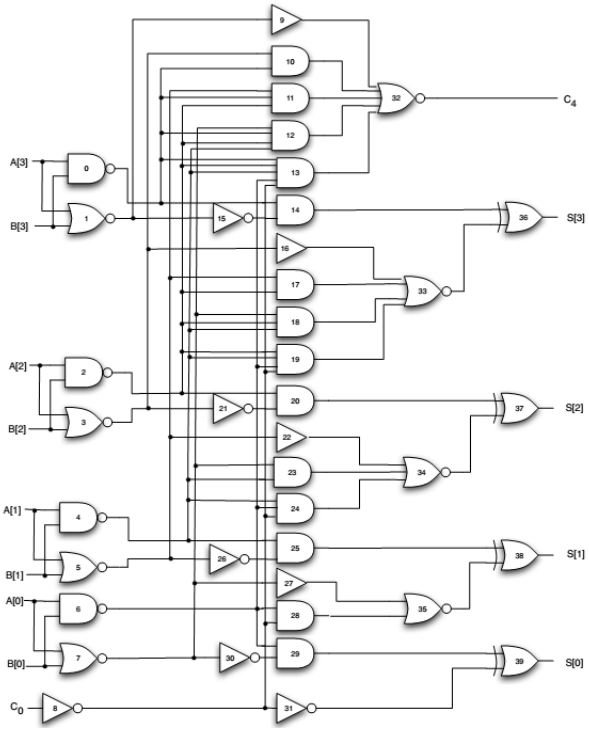

Fig. 3. Schematic of the benchmark circuit 74283

In Tables 2, 3 and 4, three different gradings are reported. One is based on logical masking, one just considers electrical masking, and the last one merges the two masking factors and gives a more accurate combined grading. Moreover, the SET pulses are generated on each node using a normal distribution to compute the electrical masking factor. Hence, the electrical

masking is a function of the mean and the variance of the distribution. In our simulation, different means and variances are considered for each circuit, but they do not influence the result in so far as these values are fixed for all of the nodes in a circuit.

Although the considered benchmark circuits are small, the proposed approach is scalable to the analysis of large benchmarks. This will be addressed in future work.

Table 4. Gate grading for the benchmark circuit 74283

Gate	LM	EM	Priority
0	0.2500	0.0178	14
1	0.0000	0.0224	10
2	0.2500	0.0178	14
3	0.0000	0.0224	10
4	0.2500	0.0178	14
5	0.0000	0.0224	10
6	0.2500	0.0245	27
7	0.0000	0.0224	10
8	0.0000	0.0202	9
9	0.3750	0.0123	21
10	0.4375	0.0123	22
11	0.4687	0.0123	23
12	0.4843	0.0123	26
13	0.4687	0.0123	23
14	0.0000	0.0154	1
15	0.2500	0.0178	14
16	0.3750	0.0237	28
17	0.4375	0.0237	32
18	0.4687	0.0237	35
19	0.4375	0.0237	32
20	0.0000	0.0154	1
21	0.2500	0.0178	14
22	0.3750	0.0237	28
23	0.4375	0.0237	32
24	0.3750	0.0237	28
25	0.0000	0.0154	1
26	0.2500	0.0178	14
27	0.3750	0.0237	28
28	0.2500	0.0237	25
29	0.0000	0.0154	1
30	0.2500	0.0178	14
31	0.0000	0.0154	1
33	0.0000	0.0154	1
34	0.0000	0.0154	1
35	0.0000	0.0154	1

IV. CONCLUSIONS

In this paper, a novel gate grading approach is proposed to consider both logical and electrical masking factors. The proposed approach is more accurate than existing techniques. The gates in a combinational circuit are prioritized and higher weights are assigned to those with lower masking capabilities. This indicates that such gates should be hardened first in order to increase hardware usage efficiency and, at the same time, to minimize area overhead.

REFERENCES

[1] J. Han, H. Chen, E. Boykin and J. Fortes, "Reliability evaluation of logic circuits using probabilistic gate models," *Microelectronics Reliability*, vol. 51, no. 2, pp. 468-476, 2011.

[2] S. Rezaei, S. G. Miremadi, H. Asadi, M. Fazeli, "Soft error estimation and mitigation of digital circuits by characterizing input patterns of logic gates", *Microelectronics Reliability*, vol. 54, no. 6, pp. 1412-1420, 2014.

[3] H. Zandevakili, A. Mahani, M. Saneei, "An accurate and fast reliability analysis method for combinational circuits", *International Journal of Computation and Mathematics in Electrical and Electronics Engineering (COMPEL)*, vol. 34, no. 3, pp. 979-995, 2015.

[4] V. H. Vaghef, A. Peiravi, "Node-to-node error sensitivity analysis using a graph based approach for VLSI logic circuits", *Microelectronics Reliability*, vol. 55, no. 1, pp. 264-271, 2015.

[5] H. Chen and J. Han, "Stochastic computational models for accurate reliability evaluation of logic circuits," *20th IEEE/ACM Great Lakes Symposium on VLSI*, Providence, Rhode Island, USA, pp. 61–66, 2010.

[6] Y. Moreau, S. Duzellier, and J. Gasiot, "Evaluation of the upset risk in CMOS-SRAM through full three dimensional simulations," *IEEE Transactions on Nuclear Science*, vol. 42, no. 6, pp. 1789–1796, 2009.

[7] F. Irom, F. F. Farmanesh, A. H. Johnston, G. M. Swift, and D. G.Millward, "Single-event upset in commercial silicon-on-insulator PowerPC microprocessors," *IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pt. 1, pp. 3148–3155, 2002.

[8] O. Ruano, J. A. Maestro, P. Reviriego, "A fast and efficient technique to apply selective TMR through optimization", *Microelectronics Reliability*, vol. 51, no. 12, pp. 2388-2401, 2011.

[9] L. Sterpone and M. Violante, "A new partial reconfiguration-based fault-injection system to evaluate SEU effects in SRAM-based FPGAs," *IEEE Transactions on Nuclear Science*, vol. 54, no. 4, pp. 965–970, 2007.

[10] K. Woo, M. Guthaus, "Fault-tolerant synthesis using non-uniform redundancy", *IEEE International Conference on Computer Design*, pp. 213-218, 2009.

[11] P. Reviriego, J. A. Maestro, O. Ruano, "Efficient protection techniques against SEUs for adaptive filters: an echo canceller case study", *IEEE Transactions on Nuclear Science*, vol. 55, no. 3, pp. 1700-1707, 2008.

[12] O. Ruano, J. A. Maestro, P. Reviriego, "A fast and efficient technique to apply selective TMR through optimization", *Microelectronics Reliability*, vol. 51, pp. 2388-2401, 2011.

[13] T. Ban, L. Naviner, "Progressive module redundancy for fault tolerant designs in nano-electronics", *Microelectronics Reliability*, vol. 51, pp. 1489-1492, 2011.

[14] S. Krishnaswamy, S. M. Plaza, I. L. Markov, J. P. Hayes, "Signature-based SER analysis and design of logic circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 1, pp. 74-86, 2009.

[15] T. Ban, "Methods and architectures based on modular redundancy for fault-tolerant combinational circuits", PhD Thesis, *Paris Institute of Technology (ParisTech)*, 2014.

[16] M. Hosseinabady, P. Lotfi-Kamran, J. Mathew, S. Mohanty, D. Pradhan, "Single-event transient analysis in high speed circuits", *International Symposium on Electronic System Design*, pp. 112-117, 2011.

[17] Q. Zhou, K. Mohanram, "Gate sizing to radiation harden combinational logic", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 1, pp. 155-166, 2006.

[18] Y. S. Dhillon, A. U. Diril, A. Chatterjee, A. D. Singh, "Analysis and optimization of nanometer CMOS circuits for soft-error tolerance", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 5, pp. 514-524, 2006.

[19] J. Han, H. Chen, J. Liang, P. Zhu, Z, Yang, F. Lombardi, "A stochastic computational approach for accurate and efficient reliability evaluation", *IEEE Transactions on Computers*, vol. 63, no. 6, pp. 1336-1350, 2014.

[20] J. Han, E. Leung, L. Liu and F. Lombardi, "A Fault-Tolerant Technique using Quadded Logic and Quadded Transistors," *IEEE Transactions on VLSI Systems*, vol. 23, no. 8, pp. 1562-1566, 2015.