A Ternary Content Addressable Cell Using a Single Phase Change Memory (PCM)

Pilin Junsangsri, Fabrizio Lombardi
Department of Electrical and Computer Engineering
Northeastern University
Boston, MA 02115, USA
(1) 617-373-4854
Junsangsri.p@husky.neu.edu, lombardi@ece.neu.edu

Jie Han
Department of Electrical and Computer Engineering
University of Alberta
Edmonton, Alberta T6G 2V4, Canada
(1) 780-492-1361
jhan8@ualberta.ca

ABSTRACT
This paper presents the novel design of a Ternary Content Addressable Memory (TCAM); different from existing designs found in the technical literature, this cell utilizes a single Phase Change Memory (PCM) as storage element and ambipolarity for comparison. A memory core consisting of a CMOS transistor and a PCM is employed (1T1P); for the search operation, the data in the 1T1P memory core is read and its value is established using two differential sense amplifiers. Compared with other non-volatile memory cells using emerging technologies (such as PCM-based, and memristor-based), simulation results show that the proposed non-volatile TCAM cell offer significant advantages in terms of power dissipation, PDP for the search operation, write time and reduced circuit complexity (in terms of lower counts in transistors and storage elements).

Categories and Subject Descriptors
B.7.1 **[Integrated Circuits]**: Types and Design Styles – *Advanced Technologies, Memory Technologies, VLSI (Very Large Scale Integration).*

General Terms
Design

Keywords
Ternary Content Addressable Memory (TCAM), Phase Change Memory (PCM), Ambipolar Transistor, Emerging Technology

1. INTRODUCTION
A Ternary Content Addressable Memory (TCAM) is a fully associative memory that implements a lookup-table function using a dedicated comparison circuitry within usually a single clock cycle. It compares the input search data against a table of stored data; the address of the matching data (if any) is then returned [1]. The memory cell in a TCAM stores three states (i.e. '1', '0', '2'). The additional state '2' is also referred to as the "mask" or "don't care" state; it is used for matching to either a '0' or '1' in the input search data process. TCAM is used for applications that allow both exact and partial matches [2], it is mostly used for specific application tasks, such as the longest prefix matching in network search engines. However, the utilization of a TCAM comes at the cost of increased area and power consumption; these are two of the design parameters that chip designers usually strive to reduce in the nanometric scales. Moreover with an ever increasing number of applications, TCAMs of increasing larger size are often required, thus further exacerbating power consumption [1].

This paper introduces a TCAM cell that is different from the designs found in the technical literature, it employs only a single phase change memory (PCM) as non-volatile storage element and a CMOS transistor as control element in the memory core, i.e. 1T1P. For the search operation, the data in the 1T1P memory core is read and its value is established using differential sense amplifiers. Ambipolar transistors are employed in the circuit for comparing the stored with the search data. The advantage of ambipolarity is that the state of a transistor (ON/OFF) is controlled by the voltage at the polarity gate and can be implemented by a single device (such as a CNTFET) [3]. The proposed ambipolar-based comparator circuit requires two ambipolar transistors for TCAM operation. Simulation results show that the proposed TCAM cell offer significant advantages in terms of write time, search time, power dissipation and reduced transistor count compared to other non-volatile memories when compared with other non-volatile TCAM cells (such as PCM- and memristor-based).

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2. REVIEW AND PRELIMINARIES
2.1 Phase Change Memory (PCM)
The phase change memory (PCM) is regarded as one of the most promising alternatives among emerging technologies for non-volatile memory design. PCM has a high density, good speed, low operating voltage, excellent scaling capabilities and compatibility with a complementary metal oxide semiconductor (CMOS) process [4]. Data storage in a PCM is related to the phase transformation of the chalcogenide alloy (e.g. $Ge_2Sb_2Te_5$, GST) that exhibits amorphous and crystalline phases. In the amorphous phase, the resistance of the PCM is high and is commonly referred to as the *reset state*; in the crystalline phase, its resistance is low and is commonly referred to as the *set state* [4]. To program data into a PCM, a pulse with high amplitude is used to melt and quench the PCM to an amorphous phase (*Reset State*), while a longer pulse with low amplitude is used to crystallize the PCM to a crystalline phase (*Set State*) [4].

2.2 Ambipolar Transistor
Different from a traditional (unipolar silicon CMOS) device whose behavior (either p-type or n-type) is determined at fabrication, ambipolar devices can be operated in a switched mode (from p-

type to n-type, or vice versa) by changing the gate bias [4] [5]. Ambipolar conduction is characterized by the superposition of electron and hole currents; this behavior has been experimentally reported in different emerging technologies such as carbon nanotubes [3], silicon nanowires [4], graphene [6], and organic semiconductor heterostructures [7]. An ambipolar transistor can be used to control the direction of the current based on the voltage at the so-called *polarity gate*. The second gate (referred to as the Polarity Gate, PG) controls its polarity, i.e. when PG is set to logic '0', the ambipolar transistor behaves like a NMOS; when PG is set to logic '1', it behaves like a PMOS [8]. In the technical literature and to the best knowledge of the authors, there is no HSPICE compatible model to simulate the behavior of an ambipolar transistor; therefore, in this paper, the model of Figure 1a is utilized at macroscopic level for simulating the characteristics of an ambipolar transistor by using four transmission gates and two MOSFETs.

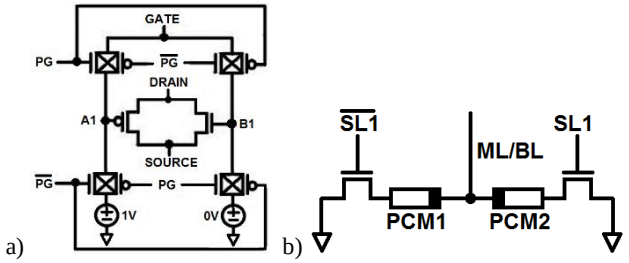

Figure 1. a) Model of an ambipolar transistor b) TCAM [9]

2.3 Existing TCAM Designs

TCAM designs using emerging technologies (such as the memristor and PCM) and CMOS have been extensively analyzed in the technical literature [2] [9] [10]. A CMOS-based TCAM cell employs two SRAMs as storage core [9] and requires 16 transistors. A TCAM with a larger number of transistors [8] incurs in a high power dissipation [10]; moreover, the relatively high leakage current encountered at nanoscale CMOS feature sizes [10] and the volatile nature of operation, are of concern. A memristor-based TCAM cell has been proposed in [2]. Six transistors are employed as control elements, while two memristors are used as storage elements. Since no additional supply voltage is required [2], its power dissipation is less than a CMOS TCAM cell. The TCAM cell of [2] requires a smaller number of transistors; however its write and read times [2] are slower than for a CMOS TCAM cell and a refresh operation is also needed when the cell is consecutively read many times. PCM is another emerging technology that can be employed as storage element in a TCAM cell. The resistance of a PCM remains unchanged if the voltage drop across it is less than the threshold voltage, i.e. no refresh operation is required. In [9], a TCAM cell is proposed by using 2 PCMs and 2 CMOS transistors (Figure 1b). By storing data in the form of PCM resistances, the search operation of a TCAM [9] starts by setting the match voltage (V_{ML}) to 0.4V, while the voltage at the search lines (SL and $\overline{SL}$) is based on the search data. The output of the search operation is presented in the form of a match line current (I_{ML}). The size of the transistors (M1 and M2) of this TCAM [9] must be adjusted until the resistances during the set and reset states are close to the PCM resistances of state '1' and '0' respectively; therefore, the design of this TCAM cell [9] is complicated and difficult to attain in the presence of variations as encountered in the nano scales. Moreover, the output of the search operation [9] is given as a match line current (I_{ML}), a *current sense amplifier* is required. Moreover, the match line current of the TCAM cell [9] during a search operation is very small, i.e. a high-performance current sense amplifier is needed.

3. PROPOSED CELL

This section presents the basic principles of the proposed cell. The basic memory core consists of a phase change memory (PCM) as storage element and a CMOS transistor as control element, i.e. this is a 1T1P memory core. The write and read operations of this 1T1P memory core are established by controlling the voltages at the bitline (BL) and the word lines (WL) as shown in Figure 2a.

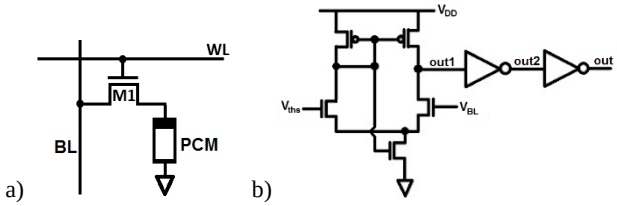

Figure 2. a) The proposed 1T1P core b) Differential sense amplifier [11]

3.1 Write Operation

To write data into the memory core, the write voltage is obtained as input from BL, while WL is used as selection line. When the word line voltage (V_{WL}) is at V_{DD}, M1 is ON, the voltage of BL (V_{BL}) passes through M1 and drops across the PCM. The 1T1P core can be written based on the value of V_{BL}. State '0' corresponds to the amorphous phase of the PCM (high resistance value) while state '1' corresponds to the crystalline phase (low resistance value). State '2' or *don't care* state is given by an intermediate resistance of the PCM (intermediate phase i.e. between the amorphous and the crystalline phases).

3.2 Read Operation

Initially, the bitline is precharged to the Vread value; as the word line is at V_{DD}, M1 is ON. So V_{BL} flows through M1 and drops across the PCM; the data stored in the core is found by checking the value of V_{BL}. If a '1' (low PCM resistance) is stored in the 1T1P core, V_{BL} is easily passed to GND, because for a '1' the value of PCM resistance is very low. However if a '0' is stored, the value of VBL is higher than for state '1'. Therefore, the data stored in the memory core is correctly read.

The value of the read voltage (V_{read}) of the core is limited to V_h because holding voltage is the minimum threshold voltage of PCM. The change from the OFF to ON states (or vice versa) during read operation does not occur in this memory core.

4. CIRCUIT DESIGN

The proposed cell consists of few circuits (in addition to the core) that are analyzed and discussed next.

4.1 Differential Sense Amplifier

The match or mismatch outcome of the proposed TCAM cell is generated by using two differential sense amplifiers for estimating stored data and by employing ambipolar transistors to compare the stored and the search data. A differential sense amplifier [11] (Figure 2b) finds the difference between V_{BL} and the threshold voltage of the differential sense amplifier (V_{ths}), then inverters are employed to drive the voltage difference to the output (V_{out}). If V_{BL} is higher than V_{ths}, then the voltage at node out is at GND, otherwise the voltage at node out is given by V_{DD}.

The values of the threshold voltages of the differential sense amplifiers (V_{ths1}, V_{ths2}) are given between the '0' and '2' and the '2' and '1' states respectively, while the output voltages are given at nodes O1 and O2 (Figure 3a). If a '0' ('1') is stored in the 1T1P core, V_{BL} is high (low). The voltages at O1 and O2 are at GND (V_{DD}) and GND (V_{DD}). However if a '2' is stored in the memory

core, V_{BL} takes the intermediate value, i.e. the voltages of nodes O1 and O2 are given by GND and V_{DD} respectively.

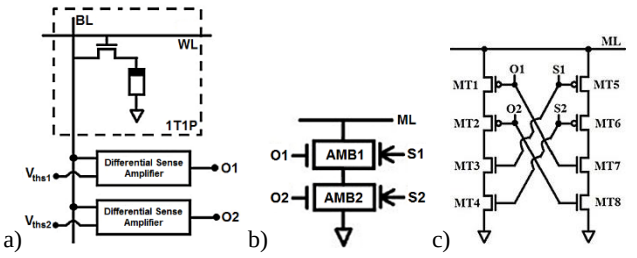

Figure 3. a) 1T1P core and differential sense amplifiers b) Ambipolar-based TCAM comparator circuit c) CMOS-based TCAM comparator circuit

4.2 Comparator Circuit

After the data stored in the 1T1P memory core is adjusted by the differential sense amplifiers and observed as voltages at nodes O1 and O2, a comparison circuit is used to compare the stored with the search voltages.

The *match* or *mismatch* outcome of the proposed TCAM cell is generated using the match line voltage (V_{ML}) for the output of the comparator circuit. An ambipolar-based comparator circuit for TCAM operation (Figure 3b) employs 2 ambipolar transistors. The match or mismatch outcome of the proposed TCAM cell is based on precharging the match line voltage (V_{ML}) to V_{DD}, while the search (stored) data is provided as voltage at lines S1 (O1) and S2 (O2) to the polarity gates of the ambipolar transistors.

Table 1. Voltages at nodes O1, O2, S1, S2, and match line voltage of proposed TCAM comparator circuit

Search	V_{S1}	V_{S2}	*Stored*	V_{O1}	V_{O2}	V_{ML}	*Outcome*
0	0	0	0	0	0	V_{DD}	*Match*
	0	0	1	1	1	GND	*Mismatch*
	0	0	2	0	1	V_{DD}	*Match*
1	1	1	0	0	0	GND	*Mismatch*
	1	1	1	1	1	V_{DD}	*Match*
	1	1	2	0	1	V_{DD}	*Match*
2	0	1	0	0	0	V_{DD}	*Match*
	0	1	1	1	1	V_{DD}	*Match*
	0	1	2	0	1	V_{DD}	*Match*

Table 1 shows the operation of the proposed TCAM comparator circuit. An ambipolar transistor is ON only when the voltages at its gate and polarity gate are different. When two ambipolar transistors are connected in series (Figure 3b), the match line voltage discharges only when a '0' (as data) is stored in the cell and searching for a '1' (or vice versa). This matches with the search operation of a TCAM. The circuit in Figure 3b is used as comparator circuit of the proposed TCAM cell. Consider a CMOS-based comparator circuit for TCAM (Figure 3c); similar to the ambipolar-based comparator, the match or mismatch outcome of a TCAM cell is accomplished by precharging the match line voltage (V_{ML}) to V_{DD}, while delivering the search (stored) data as voltages at lines S1 (O1) and S2 (O2).

5. SIMULATION RESULTS

The simulation results of the proposed TCAM cell are presented in this section. HSPICE is used as simulation tool and the model of [4] is employed for the PCM; its resistance range is initially given by 7kΩ – 200kΩ. The macroscopic model of Figure 1a is utilized for the ambipolar transistor; its transistor sizes are adjusted to generate the symmetric conduction between the PMOS and NMOS behaviors. Simulation is initially performed at a CMOS feature size of 32nm and a supply voltage (V_{DD}) of 0.9V. The performance of the memory cells is obtained by combining the performance of the different circuits.

5.1 1T1P Memory Core

The two basic operations (read and write) of the 1T1P core are considered first. For the write operation, the bitline voltage (V_{BL}) must be controlled when the word line voltage (V_{WL}) is set to V_{DD}, V_{BL} is passed through M1 and is dropped across the PCM. The PCM resistance is switched to the ON-state value, and its crystalline fraction (C_x) is changed. The write time (i.e. from the amorphous to a crystalline phase) linearly increases when increasing the range of the PCM resistance. For the read operation, the bitline voltage (V_{BL}) must be precharged to V_{read}; when V_{WL} is at V_{DD}, the data in the memory core is read and detected from the bitline voltage. The relationship between the read time and V_{BL} is plotted in Figure 4.

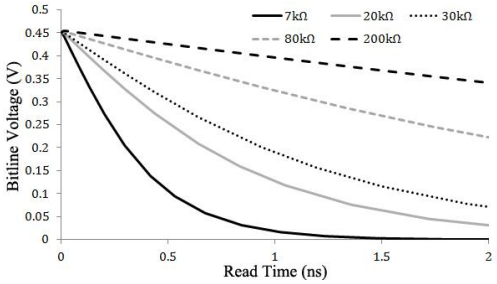

Figure 4. Bitline voltage of 1T1P memory core for a read operation (bitline capacitance is 0.03pF)

As shown in Figure 4, the bitline voltage is higher at a larger PCM resistance. As the PCM resistance of state '0' is larger than the resistance for either state '2' or '1', the bitline voltage during the read operation for state '0' is larger than the bitline voltage for either state '2' or state '1'. Since ternary data are stored in a TCAM, the value of the intermediate PCM resistance of 1T1P core for the "don't care" state ('2') is considered. The value of intermediate PCM resistance for state '2' is chosen as the resistance such that its bitline voltage is in the middle of the voltages for state '0' (200kΩ) and state '1' (7kΩ). Such a value should be not biased toward none of these two states; therefore for the read operation, voltage difference between state '0' and intermediate state must be nearly equal to the voltage difference between state '1' and intermediate state.

Table 2. Read time and bitline voltage difference (between state '0' and intermediate state and between state '1' and intermediate state) at intermediate PCM resistance values

Intermediate PCM Resistance	*Read Time (ns)*	*Bitline Voltage Difference (V)*
20kΩ	0.378	0.135
30kΩ	0.83	0.19
50kΩ	1.64	0.178
70kΩ	2.514	0.15
80kΩ	3.015	0.14

Table 2 shows the read time of a 1T1P memory core at different values of possible intermediate PCM resistance. At 30kΩ, the bitline voltage difference between state '0' and the intermediate state (equal to the difference between state '1' and the intermediate state) has the highest value at the least read time. Therefore based also on the simulation results of Table 2, 30kΩ is the appropriate intermediate PCM resistance to represent state '2' of a 1T1P memory core. So the read time is then selected such that the values

of the voltage differences between the states are high and nearly the same; this occurs at 0.83ns.

5.2 Differential Sense Amplifier

After reading the 1T1P core, bitline voltage takes the value of the stored data through two differential sense amplifiers.

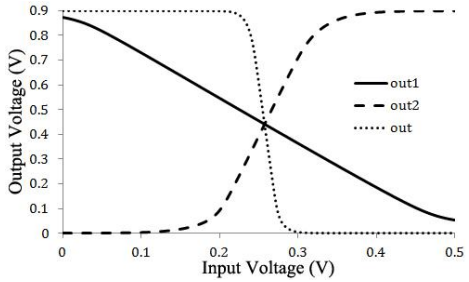

Figure 5. Output voltage of differential sense amplifier when V_{ths} = 0.15V

Figure 5 shows the output voltage of differential sense amplifier when changing the input voltage; the threshold voltage of the differential amplifier (V_{ths}) is given by 0.15V. The output voltage of the differential sense amplifier switches at 0.25V (Figure 5). So when the input voltage of the differential sense amplifier (V_{BL}) is less than 0.25V, the voltage at out is V_{DD}; however if V_{BL} is higher than 0.25V, the voltage at out is at GND (0V). Table 3 presents the voltages at O1 and O2 when the 1T1P core is connected to the differential sense amplifiers in a TCAM (Figure 3a).

Table 3. Bitline voltage of 1T1P core and output voltages of differential sense amplifiers for TCAM operation at read times

State	*PCM (kΩ)*	*V_{BL} (0.83ns)*	*V_{O1} (V)*	*V_{O2} (V)*
0	200	0.407	0	0
2	30	0.230611	0	0.9
1	7	0.0386	0.9	0.9

The switching voltage of the differential sense amplifier is different from the threshold voltage of the differential amplifier (V_{ths}). Figure 6 shows that the switching voltage changes linearly with the threshold voltage of the differential sense amplifier.

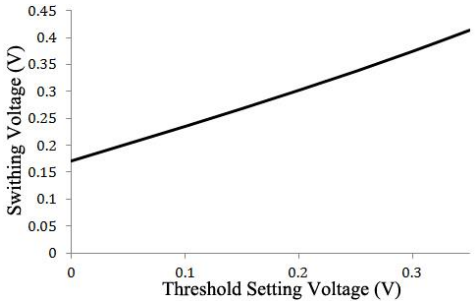

Figure 6. Threshold voltage of differential sense amplifier (V_{ths}) and its switching voltage

Consider the delay of the differential sense amplifier; when the input voltage of the differential sense amplifier is changed from GND to the holding voltage (V_h), the voltage at node out does not suddenly change, i.e. there is a delay in the switching process. The delay of the differential sense amplifier at a 32nm CMOS feature size is given by 0.067ns.

5.3 Comparator Circuit

The data stored in the 1T1P core must be changed to a two-valued voltage by the differential sense amplifiers; so for the search operation of a TCAM cell, a circuit is required for comparing the stored data with the search data. In this paper, the ambipolar-based (Figure 3b) and CMOS-based (Figure 3c) comparator circuits are assessed. The model in Figure 1a is employed to simulate ambipolar-based comparison circuit of TCAM. The initial values for the voltages at nodes A1 and B1 in the model for the ambipolar transistor are given by V_{DD} and GND respectively; the characteristics of the ambipolar transistor are then generated and the delay of the comparison circuit is established.

Table 4. Search time of the CMOS and ambipolar-based TCAM comparator circuits at a supply voltage (V_{DD}) of 0.9V

Search	*V_{S1}*	*V_{S2}*	*Stored*	*V_{O1}*	*V_{O2}*	*Search Time (ns)*	
						CMOS	*Ambipolar*
0	0	0	1	1	1	4.814	0.347
1	1	1	0	0	0	4.814	1.55

The match line voltage (V_{ML}) is discharged only when the stored and search data are mismatched, so only the mismatch delay is considered. As shown in Table 4, the comparison circuit based on ambipolar transistors is faster than the CMOS-based circuit. Also it should be noted that the ambipolar-based comparison circuits requires a significantly lower number of transistors (at most two, if the ambipolar transistors are implemented by CNTFETs for TCAM operation [3]).

5.4 Delay

By adding the delay of each circuit in the cell, the total delay for the search operation is reported in Table 5.

Table 5. Delay of proposed TCAM cell for a search operation

Circuit	*Delay (ns)*
1T1P Memory Core	0.83
Differential Sense Amplifier [11]	0.067
Comparison Circuit	1.55
Total Delay	2.447

So, the total delay of the ambipolar-based TCAM cell is 2.447ns (Table 5). However, if an ambipolar transistor is implemented by utilizing a SB-CNTFET [3] (as equivalent to the macromodel of the ambipolar transistor of Figure 1a), the delay of the comparison circuit can be significantly reduced because [3] has shown that the inverter delay of a SB-CNTFET at a diameter of 1nm, is nearly 1ps [3].

5.5 Power Dissipation

Only the power dissipation during a search operation is considered. Table 6 shows the average power dissipation, average miss delay and power delay product (PDP) of each circuit in the proposed ambipolar-based TCAM cell. State '1' of the 1T1P cell consumes the highest power, while state '0' consumes the least due to the high resistance value (200kΩ). Moreover, in state '1' (7kΩ), the bitline voltage can be passed easier to GND, thus dissipating more power than for the other two states with larger PCM resistance values. For the average power dissipation of the comparison circuit, the macromodel of the ambipolar transistor is used; this is a very pessimistic value, because the power dissipation in Table 6 accounts for the 10 transistors used in this macromodel (Figure 1a) rather than the power dissipation of a fabricated device (using for example a single CNTFET [3]). The average power dissipation and the PDP of comparator circuit made of a single CNTFET should be even lower than the values obtained for the macromodel of the ambipolar transistor (Figure 1a).

Table 6. Average power dissipation, average miss delay and power delay product of each circuit in the proposed TCAM cell

Circuit	*State /outcome*	*Average Power (µW)*	*Average Miss Delay (ns)*	*PDP (fJ)*
1T1P	0	1.3542	0.83	1.1240
	1	4.4175	0.83	3.6726
	2	3.4963	0.83	2.9019
Differential Sense Amplifier	N/A	22.3939	0.067	1.5004
Comparator	*mismatch*	24.696	1.55	38.2788

5.6 PCM Resistance Range

In this section, the influence of increasing the PCM resistance range (i.e. by varying the resistance of the highest value) is assessed for the read/write times as well as the PDP. The resistance for state '0' is changed to 100kΩ and 300kΩ.

Table 7. 1T1P core performance under different PCM resistance ranges; at 32nm feature size and 0.9V supply voltage

PCM Resistance Range	*Write time (ns)*	*Read time (ns)*	*PDP (fJ)*
7kΩ-100kΩ	94.81	1.046	3.693
7kΩ-200kΩ	199.34	0.83	3.6726
7kΩ-300kΩ	301.78	0.795	3.6666

Table 7 shows the write time of the 1T1P core (when the data in the memory core is changed from '0' to '1'), the read time and the power delay product (PDP) of the 1T1P core (for the read '1' operation). As shown in Table 7, the write time of the 1T1P core changes depending on the PCM resistance range. As for the read time of the TCAM, the read time of a smaller PCM resistance range results in a larger value. The same effect is observed for the PDP.

5.7 1T1P Cores/Bitlines

In this section, the number of 1T1P cores connected to a single bitline is initially considered at a read time of 0.83ns for TCAM operation as described previously. Figure 7 shows that the bitline voltage of states '1' (7kΩ) and '2' (30kΩ) increases when the number of 1T1P cores connected to it is increased. However for state '0' (i.e. the PCM resistance is high at 200kΩ), the bitline voltage is almost constant, because its value is close to V_h (as precharged during the read operation). The difference between the bitline voltages of each state are still large, hence the read operation can be still executed correctly.

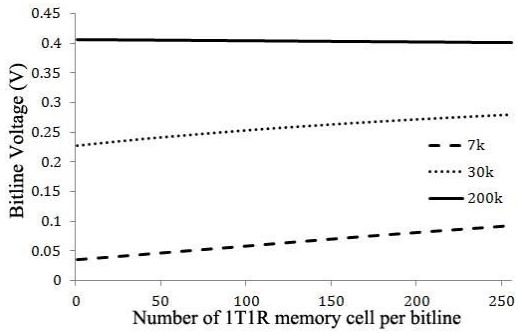

Figure 7. Bitline voltage vs number of 1T1P cores per bitline, (read time of 0.83ns and TCAM operation)

5.8 CMOS Feature Size

Previously, the CMOS feature size of the proposed TCAM design has been fixed to 32nm. Next, the design is also assessed when different HP (high performance). PTMs are utilized at the lower feature sizes of 22 and 16nm. Table 8 shows the delay of the proposed TCAM cell for the search operation when the supply voltage is either kept constant or varied as per PTM specifications. Smaller features sizes show a significant reduction in total delay at the constant supply voltage (i.e. 0.9V). As the values in the PCM resistance are still the same, a reduction in power supply is not as beneficial to the search time as the feature size.

Table 8. Delay of proposed TCAM cell for the search operation when varying CMOS feature size and supply voltage

Circuit	*CMOS Feature Size (nm)*					
	16	*22*	*32*	*16*	*22*	*32*
1T1P Memory Cell	0.738	0.78	0.83	1.023	0.93	0.83
Differential Sense Amplifier	0.024	0.045	0.067	0.039	0.053	0.067
Comparator	0.334	0.53	1.55	0.698	0.87	1.55
Total Delay	1.096	1.355	2.447	1.76	1.853	2.447
Voltage Supply(V)	0.9			0.7	0.8	0.9

6. COMPARISON

In this section, the proposed TCAM cell is compared with different schemes found in the technical literature employing PCM, memristor and CMOS.

6.1 PCM-Based TCAM Cell [9]

As presents in Figure 1b, the cell of [9] employs 2 PCMs and 2 CMOS transistors to store data in a TCAM. The PCMs are used as storage elements. The search operation of a TCAM [9] starts by setting the match voltage (V_{ML}) at 0.4V, while the voltage at the search lines (SL and $\overline{SL}$) is based on the search data. The output of the search operation is presented in the form of a match line current (I_{ML}). The *match* or *mismatch* outcome of the TCAM requires the adjustment of the search voltage V_{SL} as function of I_{ML}. Hence, a *current differential amplifier* [9] is required.

Table 9. Comparison between proposed 1T1P TCAM and TCAM [9] at 32nm CMOS feature size and 0.9 supply voltage

Circuit	*TCAM*	
	[9]	*Proposed*
Write Time (ns)	209.53	199.34
Search Time (ns)	1.346	2.447
Number of Transistors/Core	2	1
Number of PCM s/Core	2	1
Power Dissipation (µW)	35.9658	17.757
PDP of Search Operation (fJ)	48.41	43.4518

Table 9 shows the comparison results; the write time of the proposed TCAM cell is faster than the TCAM of [9] due to the higher number of resistive elements per core. As for the search time, the search time of the proposed TCAM cell is slower than the TCAM of [9]; this occurs, because in the proposed TCAM cell, the search time is based on the selection of the time at which the values of the bitline voltage differences between state pairs of the TCAM are closest. Moreover, the comparison circuit of the proposed TCAM consists of two ambipolar transistors, so the discharging rate of the match line is slower. The proposed TCAM cell employs less transistors and PCM devices than the TCAM of [9], so the area of the proposed TCAM cell is lower. Furthermore, as for power dissipation and PDP, the proposed cell is better than

[9]. Hence, the proposed TCAM is better suited in low power applications.

6.2 CMOS Based TCAM Cell

In this section, a comparison between the proposed TCAM cell with a CMOS-based TCAM [9] and a NAND Flash-Based TCAM [12] is pursued at 32nm feature size. The non-volatile circuit of [12] is utilized for the NAND flash-based memory to store data; a comparison circuit is then employed for the TCAM operation.

Table 10. Comparison of the proposed and CMOS-based TCAM cell (in which a 6T SRAM is used as storage core)

Circuit	*TCAM*		
	PCM	***CMOS***	***NAND-Flash***
Write time/Erase time	199.34ns	0.033ns	300μs/2ms
Search Time	2.447ns	0.562ns	25μs
Write Operating Voltage (V)	0.9	0.9	3
Read Operating Voltage (V)			3
Number of Transistors/Core	1	16	4

Table 10 shows the simulation results; as expected, the deterioration in write and search times of the proposed cell with respect to a CMOS cell is compensated by the lower number of transistors required for implementation and the non-volatile nature of the proposed memory cells. The proposed cell is however significantly better than the other non-volatile scheme, i.e. the NAND flash-based TCAM cell of [12].

6.3 1T1M Memristor-Based Cell

The proposed memory cell using a PCM is compared with the 1T1M (memristor-based) memory cell. Simulation has been performed by using the same resistance range (7kΩ - 200kΩ) and supply voltage (0.9V) for both cores. The (programming) temperatures of the PCM during the write operation from state '0' to state '1' and state '1' to state '0' are fixed to 705K and 1200K degrees respectively [4], while the threshold resistance of the memristor for a refresh operation is given by 96.5kΩ.

Table 11. Write time, read time and number of read operations prior to refresh for 1T1P and 1T1M cores

	Core	*CMOS Feature Size (nm)*		
		16	***22***	***32***
Write time ('0' to '1')	PCM	198.66ns	198.93ns	199.34ns
	Memristor	1.837μs	2.023μs	2.202μs
Write time ('1' to '0')	PCM	6.49ns	6.50ns	6.51ns
	Memristor	1.263μs	1.385μs	1.435μs
Read time (ns)	PCM	0.738	0.78	0.83
	Memristor	0.738	0.78	0.83
Number of Reads prior to refresh ($*10^3$)	PCM	N/A	N/A	N/A
	Memristor	3.08	3.17	3.24

Table 11 shows that the 1T1P core has a faster write time than the 1T1M core, because the changing rate of the PCM resistance is faster than the changing rate of the memristance. The read times of the 1T1P and 1T1M cores are the same, because in both cases data is stored in terms of resistance (of equal value and range). When the CMOS feature size is reduced, the write and read times for both the 1T1P and 1T1M cores decrease. Moreover the number of (successive) read operations that the 1T1M core can undertake prior to a refresh operation is also considered. A memristor based core requires a refresh operation to be performed following a number of consecutive read '0' operations; this is required to prevent the stored value of the memristance to reach the threshold value. When reducing its CMOS feature size, the number of consecutive read operations prior to the refresh operation of a 1T1M core is also reduced, i.e. at a lower CMOS feature size, the bitline voltage is transferred easier to the memristor, so the read time is faster. Note that for the proposed 1T1P core, no refresh operation is required because the read voltage is limited to the holding voltage (V_h) and the PCM resistance retains its value.

7. CONCLUSION

In this paper, the PCM-based TCAM cell is proposed. This design utilize a single phase change memory (PCM) as storage element and ambipolarity for comparison. The proposed comparator circuits have been shown to be superior to their CMOS-based counterparts. Also it should be noted that the ambipolar-based comparison circuit requires a significantly lower number of transistors. Compared with other non-volatile memory cells using emerging technologies (such as PCM-based, and memristor-based), simulation results show that the proposed non-volatile TCAM cell offer significant advantages in terms of power dissipation, PDP for the search operation, write time and reduced circuit complexity (in terms of lower counts in transistors and storage elements).

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