# A Memristor-based Memory Cell with no Refresh

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*Abstract*—**This paper analyzes and improves the performance of a hybrid memory cell consisting of a memristor and ambipolar transistors. This work extends a previous design by efficiently biasing the memristor (as controlled by the ambipolar transistors), such that no refresh operation is now required. By utilizing macroscopic models, the features of the cell are characterized for the memory operations and no modification is needed to the cell circuit other than the memristor biasing scheme. A detailed treatment of the memory cell with respect to the new biasing scheme of the memristor is provided. Simulation results show that the proposed memory cell has superior performance compared with the previous memristor-based cell.**

*Index Terms*— **Memory Cell, Ambipolar Transistor, Memristor, Emerging Technology.**

## I. INTRODUCTION

With the continued scaling in the nano ranges, the technology roadmap predicted by Moore's Law is becoming difficult to meet. So-called emerging technologies have been widely reported to supersede or complement CMOS and a new type of design style commonly referred to as "hybrid", has gained considerable attention. A hybrid approach relies on partially utilizing CMOS, while introducing emerging technologies as needed for performance improvement. This is very attractive for memories in which the modular (cell-based) organization of these systems is well suited to new technologies and innovative paradigms for design.

In this paper, the memristor [1] is utilized as a non-volatile storage element, while ambipolar transistors are used for the control of the memristance in the memory operations. The ambipolar transistor (Double Gate MOSFET, or DG-FET) [2] is a type of transistor that can operate in a switched mode (from p-type to n-type, or vice versa) by changing the gate bias [3] [4]. The second gate of the ambipolar transistor (referred to as the Polarity Gate, PG) controls its polarity, i.e. when PG is '0', the ambipolar transistor behaves like a NMOS; if PG is '1', it behaves like a PMOS [2]. The macroscopic model of an ambipolar transistor consists of using two transmission gates and two MOSFETs [5].

The proposed cell is analyzed with respect to the two memory operations (read and write) and the characteristics of the memristor range for determining its on/off states. It has been shown [5] that a refresh is required when multiple consecutive read operations occur; different from [5], a new bias approach is used in this paper. The bias is applied as related to the polarity of the memristor and its effects on the two values of the memristance corresponding to the stored data. An extensive comparative analysis with [5][6] and simulation results using HSPICE are provided to substantiate the improved performance of the memory cell under the new bias; different metrics (read time, write time) are also assessed and substantial performance improvements over [5][6] are reported.

## II. BIASING AND MEMORY OPERATIONS

The basic design of the memory cell of [5] [6] is utilized also in this manuscript; as shown in Figure 1, a memristor is used as a storage element, while ambipolar transistors are used as control elements. Data is sent through the bit line (BL) and the inverse bit line (BL'), while the word line (WL) is used for line selection. When the memory cell is selected, WL is high and data is sent through BL and BL'. BL' and L2 are connected by the transistor NT2; L2 is also connected to the polarity gate (PG) of the ambipolar transistors. Therefore BL' is used for polarity selection during the read/write operation.

- When BL' is '0', the ambipolar transistors behave as NMOS, then the current flows from A to B (as identifying the terminals of the memristor in Figure 1).
- If BL' is '1', the ambipolar transistors behave as PMOS. The current flows from B to A, or from the source to the drain side of the ambipolar transistors.

Hence, the memristor is written along *both directions*, i.e. the write operation is fully bidirectional. The memristance is equal to $R_{ON}$ (low resistance) when the bias of the memristor is toward terminal A (left), and equal to $R_{OFF}$ (high resistance) when the bias is toward terminal B (right).
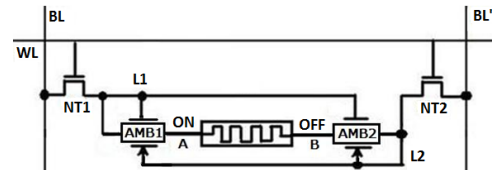


Figure 1. Memristor-based design of a memory cell with ambipolar control [5]

### A. Write operation

The memristor is written with the data on BL and BL'. Due to the nearly symmetric conductance of the n- and p-types of the ambipolar transistors, the currents that flow in and out of the memristor, are nearly equal. The two data cases of the write operation are considered next.

- To write a '0', the memristance must be $R_{OFF}$ i.e. BL at $V_{DD}$, while BL' at GND. So, the ambipolar transistors behave as NMOS (i.e. GND is connected to the polarity gate). As BL is at $V_{DD}$, both ambipolar transistors are ON; a voltage difference exists across the memristor to bias it to the $R_{OFF}$ state.
- The process for writing a '1' is similar to the one for writing a '0', but the inverted logic value. BL is at GND (i.e. 0), while BL' is at $V_{DD}$ (i.e. 1). Therefore, the ambipolar transistors behave as PMOS. The memristor is in the $R_{ON}$ state, because the voltage at B is higher than at A.

### B. Read operation

Recall that the memristor changes its memristance value if there is a current or voltage across it. To prevent this from happening, the read process must be fast [5] [6]; in particular, it should be faster than the threshold time of the memristor that is approximately given by 12ns [7]. The read operation starts by precharging the bit lines (BL and BL') to $V_{DD}$ and GND respectively, then WL is high. Similar to the write '0' operation, both AMB1 and AMB2 are initially ON during the first part of the read operation. The connection between BL and BL' is established through the ambipolar transistors and the memristor. When these lines are connected, the voltages at both bitlines tend to balance the values, i.e. the voltages at BL and BL' gradually become the same. So, the voltage at BL decreases, while the voltage at BL' increases. When the voltage of BL' is increased to a value higher than the threshold voltage, the ambipolar transistors behave as PMOS. Since the voltage at line L1 is still high, AMB1 and AMB2 are OFF and L1 and L2 are disconnected. The data stored in the memory cell is detected from the voltage difference across the bitlines.

- If a '1' is stored in the cell, the boundary of the memristor is biased toward the left (denoted by A) and the memristance is equal to $R_{ON}$. The voltage at BL is transferred to BL' and the voltage difference across the bitlines is very low.
- If a '0' is stored in the cell, the terminal of the memristor is biased toward the right terminal (denoted by B in Figure 1) and the memristance is equal to $R_{OFF}$. The bitline voltage of BL is slowly passed to BL'. When the volatage at BL' increases, the voltage at line L2 is also increased. Both ambipolar transistors behave as PMOS. Since the voltage at line L1 is still high, the ambipolar transistors are OFF. The voltage difference across the bitlines (BL and BL') for '0' is larger than for '1'.

Although the voltage difference across the memristor is present during a read operation, the state of the memristor is not affected by using the new bias. During a read operation, the memristance is biased toward B. Only the data '1' that stored in the cell is affected. However both ambipolar transistors are OFF when the read operation is operated, i.e. the memristor is isolated from the voltage of both bitlines while the voltage difference across the memristor ($V_{mem}$) is very low and drops down to GND at very fast. The read operation does not affect its current state and therefore the memory cell does not require a refresh operation.

## III. SIMULATION RESULTS

HSPICE [8] has been used to simulate the electrical characteristics of the memristor-based memory cell with the new bias; unless otherwise specified, the same default parameters as utilized in [5] are assumed under the memristor model of [9], i.e. a memristance range of 100-19k$\Omega$ and 32nm CMOS feature size [10]. ], The driver of Figure 2 [11] is utilized for the two memory operations (read and write) as in [5].
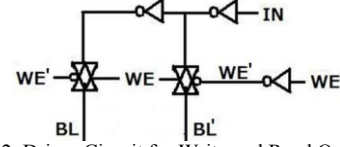


Figure 2. Driver Circuit for Write and Read Operations

### A. Write operation

The write operation is simulated first. The write time is given by the time that the memristance of the memory cell is changed from $R_{OFF}$ to $R_{ON}$ or vice versa. Consecutive write operations are usedto establish find the write time of the memory cell,. A sequence of write '1' and '0' operations is applied to node IN of the driver circuit in Figure 2; the memristance of the memory cell with the new bias is then found (for the considered cell with memristance values of 100-19k$\Omega$, the write time is 236ns).
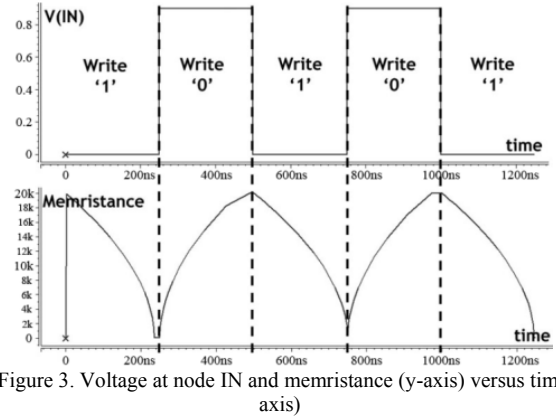


Figure 3. Voltage at node IN and memristance (y-axis) versus time (x-axis)

### B. Read operation

Prior to executing a read operation, the voltages at BL and BL' must be precharged to '1' and '0' respectively. The voltage at node IN in Figure 2 is at $V_{DD}$ and WE is high. Then, WE is low to isolate the input voltage from IN, BL and BL'. So, WL is high to start the read process. However, the model of [9] has the limitation that it does not fully consider the threshold voltage and threshold time of the memristor [12] [13], i.e. the memristance always changes during a read operation even when there is a very small voltage across it for a short time. So, the voltage across the memristor must be analyzed in more detail.

The voltage difference between BL and BL' is initially considered to assess the read time of the memory cell. As expected, the voltage difference across the bitlines for '0' ($R_{OFF}$) is higher than for a '1' ($R_{ON}$). Moreover, the voltage difference of the bitlines in the $R_{ON}$ and the $R_{OFF}$ states is

approximately 0.1V when the read time is 0.06ns. If the read time is increased furthermore, the difference increases reaching a maximum value of 0.772V (at 0.26ns).
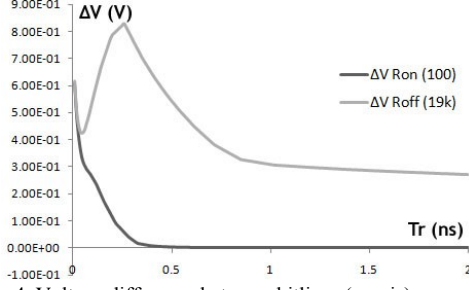


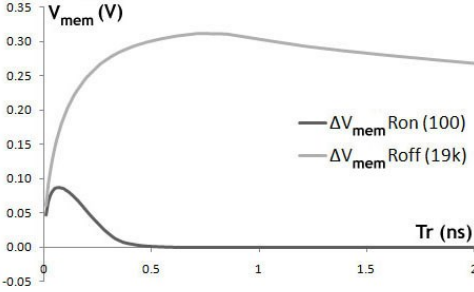Figure 4. Voltage difference between bitlines (y-axis) versus read time (x-axis)



Figure 5. Voltage difference across the memristor (y-axis) versus read time (x-axis)

The voltage difference across the memristor ($V_{mem}$) must be also considered for establishing the memristance state during a read operation. Figure 5 shows that when the memristor is in the $R_{ON}$ state, $V_{mem}$ is very small using the new bias. It slightly increases at the beginning of the read operation; however, it drops to 0V when the read time is approximately 0.5ns, i.e. it takes nearly 0.5ns for this voltage to be reduced to 0V. This is substantially less than the threshold time of a memristor, i.e. the memristor changes its memristance if the time for the voltage drop across it is larger than 12ns (as reported in [7]). So, no change in state is possible for the memristor; moreover, this confirms that $V_{mem}$ during a read operation is very small, especially when the memristor is in the $R_{ON}$ state. By utilizing the new bias, the memristance value is not disturbed during a read operation; therefore, no refresh operation or circuit is required in the memory cell with the new bias (different from [5]).

C. *Threshold Voltage of Ambipolar Transistors*

With the new bias, the memristance of the memory cell is not the sole cause of a memory state change. An erroneous threshold voltage for the ambipolar transistors when operating as PMOS may slightly change $R_{ON}$ during the read operation, because every time the memory cell is read, it is biased to the $R_{OFF}$ state. If the threshold voltage of the ambipolar transistors ($V_{th,AMB}$) is high, the read operation takes more time to switch to PMOS and turns off the ambipolar transistors. The memristance changes value by biasing toward the $R_{OFF}$ state, hence causing an erroneous read operation to occur. So, the value of $V_{th,AMB}$ must be selected to be very low to turn off the ambipolar

transistors faster during the read operation (while the voltage at L1 in Figure 1 remains still high). Therefore, the value of $V_{th,AMB}$ should be matched with the read time.

D. *Memristor range*

The write and read times of the memory cell are analyzed by varying the memristor range. When the memristor range is increased, the write time is also increased [6]. However, the read time is not very dependent on the memristor range. As shown in Figure 6, the read time of the proposed memory cell with a small memristor range and an appropriate $R_{ON}$ value, is small; for example with memristor values of $100 - 1k\Omega$, the write time is 21ns, the read time is 0.15ns, the voltage difference between bitlines when the memristor is in the $R_{ON}$ ($R_{OFF}$) state, is 0.185V (0.604V).
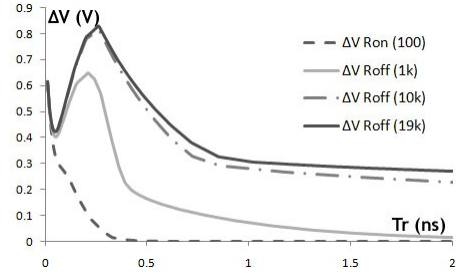


Figure 6. Voltage difference between the bitlines (y-axis) versus read time (x-axis) at different memristor values

IV. COMPARATIVE DISCUSSION

In this section, a comparative discussion between the memory cell with the new bias (i.e. with no refresh operation) and the memory cell of [5] (i.e. requiring a refresh operation) is pursued. In this paper, recall that the bias toward the left (right) terminal A (B) of the memristor corresponds to $R_{ON}$ ($R_{OFF}$); as $R_{OFF}$ has a value larger than $R_{ON}$, during the read operation, $V_{mem}$ for the $R_{OFF}$ state is higher than for the $R_{ON}$ state (as shown in Figure 5). The reverse is applicable to [5].

In [5], the left (A) terminal represents the $R_{OFF}$ value, so during the read operation, $V_{mem}$ is high. This causes the memristance to change to the $R_{ON}$ value, thus resulting in a state change for the memristor after multiple consecutive read operations. However in this paper, at the left (A) terminal, the memristance is given by $R_{ON}$. During the read operation, the voltage difference across the memristor is very low and drops to 0V within 0.5ns (significantly less than the threshold time of the memristor [7] for a state change). So using the proposed bias, the read operation does not disturb the state of the memristor.

The memory cell [5] requires a refresh operation to restore its value. The refresh operation of [5] begins by checking the difference in voltage between the bitlines when the memory cell is read. If the memristance is given by $R_{ON}$, the state is not affected [5]. If in the $R_{OFF}$ state, the read operation disturbs the memristance value. The voltage difference between the bitlines must be compared with the reference voltage to find the memristance of the memory cell.

• If it is higher, no refresh operation takes place.

- If it is equal or near to the threshold, a write '0' operation must be executed to refresh the value.

The read time of the proposed memory cell is significantly faster than for the memory cell of [5], because it completely avoids the needs to check the state of the memristor and its memristance to find the voltage value and to possibly execute the corrective operation (i.e. the write '0' operation).

The refresh time increases with an increase in the memristor range. Since the write '0'operation is employed to restore the '0' data in the memory cell [5], the refresh operation takes more time than the read '1' operation. However, the refresh time is less than the write '0' time in [5], because the threshold level of the memristor is set in the middle of the memristor range, i.e. half of the time required for the write '0' operation is sufficient.

When comparing the write operations, the simulation results in Figure 7 show that the write '0' operation is faster than the write '1' due to the slightly asymmetric nature of the memristor model of [9]. Moreover, the write time of the memory cell is fast when the boundary of the memristor is biased to the left. For '1', the write time of this memory cell is less than [5] due to the higher voltage drop across the memristor. For the write '0' operation, the write time of the memory cell under the new bias is less than the memory cell of [5] [6] when the memristor range is less than 20kΩ; however if the memristor range is higher than 20kΩ, the write '0' time of the memory cell of [5] is faster. This is caused by the not fully symmetric conductance between NMOS and PMOS in the ambipolar transistor macromodel; hence, the write operation from the A to the B terminals (i.e. forward direction) is slower than in the reverse direction (i.e. from B to A).
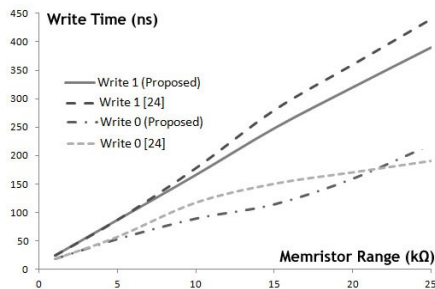


Figure 7. Write times of proposed memory cell and the memory cell of [5] [6] versus memristor range

## V. CONCLUSION

This paper has improved the performance of a previously proposed memory cell whose circuit consists of a memristor and two ambipolar transistors [5][6]. The ambipolar characteristics allow for the fast and accurate control of the memristance of the storage element. In [5], it has been shown that a refresh is required following multiple consecutive read operations. The refresh operation of the memory cell of [5] must be executed when the threshold level is reached and a state change may occur in the stored data; the refresh operation consists of checking the state of the memristor, finding the voltage value and a restoring operation (i.e. the write '0' operation).

Different from [5] [6], a new bias approach has been used in this paper for the ambipolar control of the memory cell. The bias is related to the polarity of the memristor and its effect on the two values of the memristance corresponding to the stored data (by using the ambipolar control). The new bias does not require any change in the circuit of the memory cell of [5]. An extensive comparative analysis with [5] and simulation results using HSPICE have been provided to substantiate the improved performance of the memory cell under the new bias; different metrics (read time, write time) have also been assessed. The new bias results in performance improvements for the read (as no refresh is required) and the write '1' operation; provided the memristor range is below 20kΩ (as commonly found in current designs [2] [7] [14]), also the write '0' operation can be improved over [5] [6]. Moreover, when the proposed memory cell is compared with flash memory (as presented in the [6]) the write and read time of the proposed memory cell is much faster than for the NAND and NOR flash memories.

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