Design and Evaluation of two MTJ-Based Content Addressable Non-Volatile Memory Cells

Ke Chen, Jie Han and Fabrizio Lombardi

Abstract—**This paper proposes two non-volatile content addressable memory (CAM) cells using magnetic tunneling junction (MTJ) devices and nanoscaled CMOS transistors. The first novelty of the proposed non-volatile cells is that their operation and comparison outcome are voltage-based, hence requiring no current sensor. Two types of MTJ CAM cell are proposed; each of them utilizes two MTJs in a voltage divider arrangement. They differ in the number of required transistors, i.e. the first is a NOR type cell requiring six MOSFETs, while the second is a NAND type cell requiring five MOSFETs. Performance metrics (as related to search delay, power dissipation and static noise margin) as well as variation to process, voltage and temperature (PVT) are assessed by simulation at different feature sizes of the MOSFETs. The simulation results show that the proposed designs significantly improve in terms of search delay and power delay product (PDP) over existing non-volatile CAM memory cells utilizing MTJs.**

I. INTRODUCTION

The design and development of the next generation of non-volatile memories are very important milestones in the technology roadmap, because conventional (charge-based) memory technologies (such as flash ICs) in CMOS are reaching their fundamental scaling limits [1]. The continued growth of semiconductor memories will likely rely on advances in both electronic materials and device structures. As per its name, a non-volatile resistive RAM (RRAM) employs resistive switching for storage; one of the most evident advantages of a RRAM is its compatibility with CMOS processes, such that the existing infrastructure can be readily applied to its fabrication/manufacturing. Among RRAMs, magnetic memories are considered as a competitive technology; magnetic memories show several advantages over traditional memory structures such as good write time, greater endurance and radiation tolerance [1] [5]. A magnetic memory usually utilizes a magnetic tunnel junction (MTJ) as basic device. A Content Addressable Memory (CAM) is a fully associative memory which can be classified into two types, binary CAM and ternary CAM (TCAM). The memory cells in a CAM store only two states (i.e. '0' and '1'). The non-volatile nature of a MTJ has been utilized for designing CAM cells [7] [9] [10]; these cells utilize different circuit configurations (2 transistors and two MTJs for [9] and 4 MTJs for [10]). While requiring a low complexity in design, these cells however suffer from the significant disadvantage of their current-based mode, i.e. they require a matching/sensing circuitry that must be very sensitive to current values for correct CAM operation.

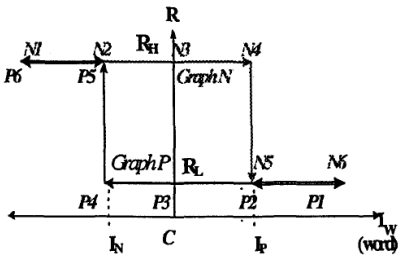
Ke Chen and Fabrizio Lombardi are with the ECE Dept, Northeastern University, Boston, USA {lombardi@ece.neu.edu}, {chen.ke1@husky.neu.edu}.
Jie Han is with the ECE Dept, University of Alberta, Edmonton, Canada {jhan8@ualberta.ca}

The objective of this paper is to provide a comprehensive circuit-level analysis and design of two novel voltage-based CAM cells that utilize two MTJs as resistive elements. In this paper, performance metrics (as related to search delay, power dissipation and static noise margin) as well as variation to process, voltage and temperature (PVT) are assessed by simulation at different feature sizes of the MOSFETs to show superior performance compared to [9] [10].

II. PRELIMINARIES

The MTJ is a device made of two ferromagnets separated by a thin insulator. If the insulating layer is thin (typically a few nanometers), electrons can tunnel from one ferromagnet into the other through a junction[1]. Consequently, such a junction can be switched between two states of electrical resistance (one with low and one with very high values), hence binary storage is accomplished [7]. Memory design requires this device to be part of a cell circuit; therefore, an assessment by modeling and HSPICE simulation of a MTJ at electrical-level is required.

Figure 1. R-I_W plot

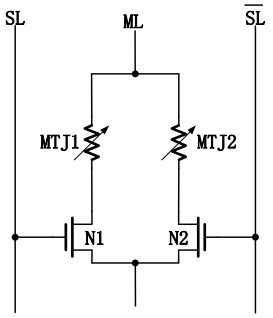


The HSPICE model of a MTJ device has been proposed in [2] [3]. In this model, a MTJ is considered as a four terminal device; two of the terminals connect directly to the MTJ resistor (through the sense lines). The other two terminals provide a magnetic bias field for the two basic memory operations (read and write), i.e. the word lines. The word and sense lines are not connected; a current through the word line induces a magnetic field on the MTJ such that its resistance can be changed (and whose value is established between the two sense line terminals). The resistance (R) of the different states of a MTJ is found in the so-called R-I_W plot (Figure 1) [2]. This figure consists of two graphs, denoted as the P and N graphs. (a) If the word current I_W is increased beyond a value N5 (which is the same as P2), the R-I_W plot is given by the graph P. Any additional magnetization caused by the word current value between P2 (N5) and P5 (N2) causes the R-I_W curve to remain on the graph P only. (b) If the word current value becomes lower than point P5 (N2), the R-I_W curve changes into the graph N. It remains on the graph N for any

value of word current between N2 (P5) and N5 (P2). The hysteretic nature of the R-I_W plot determines the storage capability of a MTJ, i.e. state 0 is assigned to graph N and state 1 to graph P (or vice versa). The memory operations are given as follows. When $I_W > I_N$ the MTJ is said to be "written" into the 1 state; and when $I_W < I_N$, it is "written" into the 0 state. The MTJ can be "read" by the word current between IN and IP (where the sensed resistance depends on the state of the MTJ).

In its simplest form, a RAM cell requires 1 MTJ and 1 transistor; i.e. a 1T1MTJ cell. The read operation is accomplished by applying the sense current through a current source and converting it to a sense voltage; this voltage can be either high or low, as based on the stored state of the MTJ. At a 32nm feature size and using the resistance values specified previously for the MTJ, the voltage at the output node is in a range between 0.54V and 0.84V [4]. While it is suitable for a RAM, it does not suffice for a CAM cell, because the value of 0.54V cannot turn off the NMOS transistor. Therefore, a 2-MTJ cell has been usually employed as implementation [4]. [1] adds a pair of transistors to the voltage divider to amplify the sensing voltage margin.

Figure 2. 2T2MTJ CAM cell [9]



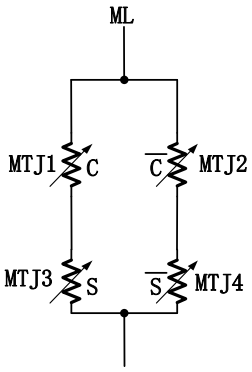
A Content Addressable Memory (CAM) is a fully associative memory which can be classified into two types, binary CAM and ternary CAM (TCAM). A binary or simply CAM is primarily used as instruction or data cache. A CAM cell stores only two states (i.e. '0' and '1') and is suitable for applications that require an exact match between the input data and the stored data. Once a CAM cell compares the input search data against its own content, it returns the address of the stored data that matches (i.e., equals) the input search data. Each stored bit of data is associated with a match line (ML) that reports the comparison result (i.e., match or mismatch). A CAM typically uses a SRAM cell for bit storage, i.e. it usually relies on the two cross-coupled inverters found in a traditional memory cell. After the ML has been charged to a high voltage, the search bit is loaded onto a differential search line and compared in parallel with the values stored in the CAM cells. [9] [10] have proposed two CAM cells; these cells utilize different designs with at least 2 MTJs. The operations of both of them are current-based, thus requiring appropriate sensing circuitry at the output. The CAM cell of [9] (Figure 2) operates as a current-monitored circuit consisting of two MTJs and two transistors; its truth table is given in Table I (I_r denotes the reference current and I_c denotes the cell current). The two MTJs are in a differential mode (MTJ1 in high resistance and MTJ2 in low resistance as "0", and MTJ1 in low resistance and MTJ2 in high resistance as "1"). If a match (mismatch) is found, then the cell current takes a value larger (lower) than the reference current Ir. The outcome (match or mismatch) is determined by comparing the current flowing through the cell with the reference current.

TABLE I. TRUTH TABLE OF 2T2MTJ CAM CELL [9]

Content	MTJ1/MTJ2	Search	Ic	Result
0	High/low	0	Ic>Ir	Match
0	High/low	1	Ic<Ir	Mismatch
1	Low/high	0	Ic<Ir	Mismatch
1	Low/high	1	Ic>Ir	Match

[10] has proposed a 4-MTJ CAM cell (Figure 3). This cell is similar to the 2T2MTJ cell of [9], but the four MTJs are now arranged into two pairs. It also uses a differential pair for storing a "1" or "0", i. e. for "0" ("1"), the left MTJ is high (low) resistance and the right MTJ is low (high) resistance. If the range between the two resistance values is sufficiently large, the difference between R_{match} and $R_{mismatch}$ is also significant, such that by measuring the current flowing through the cell, it is possible to discriminate between a match or a mismatch as outcome of the CAM operation. As this is also a current monitoring cell, the search time is again mostly determined by the current sensor.

Figure 3. 4MTJ CAM cell [10]



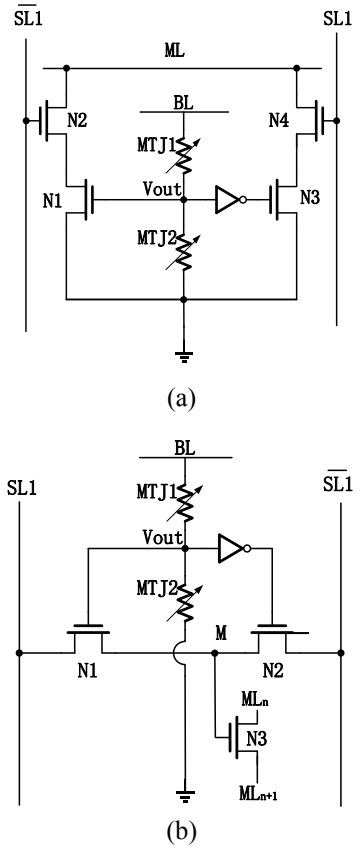
III. PROPOSED CAM CELLS

This paper presents two new CAM cells utilizing MTJs as storage elements; these cells (NOR type and NAND types) are shown in Figure 4. In Figure 4, ML denotes the Match Line for the outcome of the comparison operation (match or mismatch) in the cell. SL and $\overline{SL}$ are the Search Lines, while BL denotes the Bit Line (i.e. the memory cell is enabled only when BL=1).

The two states of both these CAMs are defined as follows.(1) State '1', MTJ1 has a low resistance value and MTJ2 has a high resistance value. (2) State '0', MTJ1 has the high resistance value and MTJ2 has a low resistance value. Both cells utilize two MTJs in a voltage divider arrangement; a number of transistors (6 for the NOR type and 5 for the

NAND type) are utilized to connect the voltage divider to the Match Line and the two Search Lines.

Figure 4. Proposed MTJ-based CAM cells: (a) NOR type; (b) NAND type



A. NOR type CAM

The first proposed CAM is a NOR type cell (Figure 4a). Its operations (phases) are given as follows. *Precharge and Write Phases:* The proposed CAM cell combines the precharge phase and the write phase into a single operation. When the cell is in the precharge phase, the Match Line is pulled high. At the same time, MTJ1 and MTJ2 can be written as follows. (1) For write a '1' operation, MTJ1 is set to the low resistance state and MTJ2 is set to the high resistance state. (2) For write a '0'operation, MTJ1 is set to the high resistance state and MTJ2 is set to the low resistance state. *Search Phase*: The search operation of a CAM checks whether there is a match between search and stored data. Two search lines (SL and $\overline{SL}$ are utilized. All cases of operations are given next. *Search '1':* BL must be initially charged to Vdd. Therefore, SL is '1' and $\overline{SL}$ is '0'. MTJ1 and MTJ2 form a voltage divider. *Mismatch '1':* The voltage at node Vout is high; N1 is turned on and N3 is turned off. Since SL is '0', N2 is on and N4 is off. Thus, N1 and N2 form a path to pull ML to GND. *Match '1':* The voltage of node Vout is high. So, N1 is on and N3 is off. As N2 is off and N4 is on, there is no path to pull ML to GND. The voltage of ML is given by V_{dd}. *Search '0':* It is similar to the Search '1' operation. BL is charged to Vdd. SL is '0' and $\overline{SL}$ is '1'. *Mismatch '0':* The voltage at Vout is low. So, N3 is turned on and N1 is turned off. As SL is '1', N4 is on and N2 is off. Thus, N3 and N4 form a path to pull ML to GND. *Match '0':* The voltage at Vout is low. In this case, N1 is off and N3 is on. However, N2 is on and N4 is off, there is no path to pull ML to GND. The voltage of ML is Vdd.

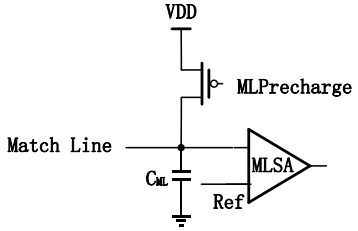
B. NAND type CAM

The different phases of operation for the proposed NAND type CAM cell (Figure 4b) are detailed next. (1) *Precharge and Write Phase:* The precharge and write phase are similar to the NOR type CAM cell, hence its treatment is omitted. (2) *Search Phase:* All cases of operations are considered. *Search '1':* BL must be charged to V_{dd}. SL is '1' and $\overline{SL}$ is '0'. So, MTJ1 and MTJ2 form a voltage divider. *Match '1'*: The voltage at node Vout is high. N1 is on and N2 is off. M is high and turns on N3. ML is discharged. *Mismatch '1':* The voltage at node Vout is high. N1 is on, while N2 is off. Therefore, M is low and turns N3 off. ML maintains the precharged value. *Search '0':* BL is charged to V_{dd}. SL is '0' and $\overline{SL}$ is '1'. *Mismatch '0':* The voltage at node Vout is low. N1 is turned off and N2 is turned on. Node M is low and turns N3 off. ML keeps the precharged value. *Match '0':* The voltage at node Vout is low. In this case, N1 is turned off and N2 is turned on. M is high and turns N3 on. ML is discharged.

IV. SIMULATION RESULTS

The proposed CAM cells are assessed in this section; however prior to the assessment, two features (namely the matching sensor and the resistance of the MTJ) that are the same in both proposed cells, are discussed first. Consider initially the matching sensor. The proposed CAM cells employ a conventional voltage comparator as matching sensor (Figure 5). The simplified circuit models shown in Figure 6 are used to find the time required for evaluating this line for the match and mismatch (or miss) cases.

Figure 5. Match Line sensor structure



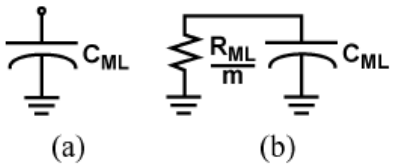
The time to evaluate ML (i.e. the time for this line to fall to 50% of the precharged voltage value) depends on the match line capacitance and the pull-down resistance. As shown in Figure 6, this is given by:

$$\tau_{ML} \approx 0.69 C_{ML} R_{ML} \quad (1)$$

Hereafter as corresponding to current technology [14], the value of 1fF is used for C_{ML}. Consider next the resistance of a MTJ. As reported in [11], the resistance of a MTJ can increase by nearly 500% at room temperature. Usually R_{low} has a value of 2K [3], so the highest value of R_{high} is 12K. These are the

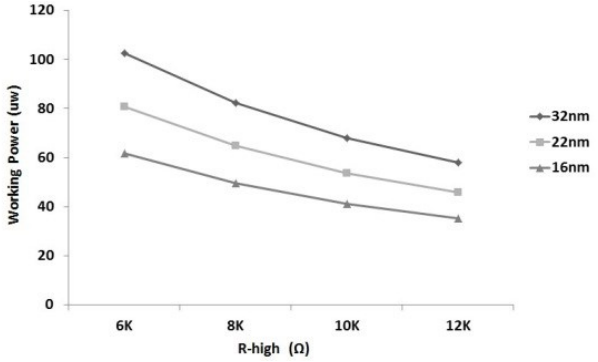
values used throughout this manuscript (unless explicitly mentioned).

Figure 6. Match line circuit model for (a) match and (b) mismatch (miss) states [6]



. In the proposed cells, if the ratio between R_{high} and R_{low} is large, the range of voltage values at node Vout will also increase, thus enhancing the noise margin. In this case, the low and high voltage values of Vout are 125mV and 775mV to control the state of the transistor. Moreover, the proposed cells require a constant operating power, because a constant current flows through the voltage divider. Figure 7 shows the operating power at different values of R_{high}, i.e. the power consumption decreases by increasing R_{high} as well as the feature size.

Figure 7. Operating power



The simulation-based assessment of different metrics as commonly associated with the performance evaluation of CAM memories [6], is presented next.

A. Search Time

The search time depends on the voltage at Vout and the Match Line. The designs of the proposed CAM cells have also been evaluated using different feature sizes. For the NOR type CAM, ML discharges when Miss '1' or Miss '0' occurs; for the NAND type. ML discharges when Match '1' or Match '0' occurs. Thus, only these situations are considered in measuring the search delay. Tables II and III show the search delay for both type at different feature sizes (32, 22 and 16nm). These Tables show that for both values of miss, the NAND type cell has a higher delay than the NOR type. Moreover as expected, the Miss 1 case for both cells incur in a larger delay (the larger delay at reduced feature size is due to the constant values of the resistances of the MTJs in the voltage divider).

B. Power

Both cells consume most power when performing the search and match operations; the simulation results are shown in Tables IV and V.

TABLE II. SEARCH DELAY FOR PROPOSED NOR TYPE CELL

Size	Miss 1	Miss 0
32nm	37.6ps	31.1ps
22nm	45.2ps	35.8ps
16nm	46.8ps	37.4ps

TABLE III. SEARCH DELAY FOR PROPOSED NAND TYPE CELL

Size	Match 1	Match 0
32nm	146.1ps	99.9ps
22nm	168.9ps	116.3ps
16nm	172.2ps	117.9ps

TABLE IV. POWER CONSUMPTION FOR PROPOSED NOR TYPE CELL

Size	search 1	search 0	Miss 1	Miss 0	Match 1	Match 0
32nm	13.3uw	16.6uw	13.8uw	16.0uw	1.85uw	4.66uw
22nm	5.38uw	6.55uw	7.60uw	9.18uw	1.10uw	2.50uw
16nm	1.88uw	2.37uw	5.12uw	6.08uw	0.64uw	1.15uw

TABLE V. POWER CONSUMPTION FOR PROPOSED NAND TYPE CELL

Size	search 1	search 0	Match 1	Match 0	Miss 1	Miss 0
32nm	1.26uw	1.16uw	5.03uw	8.37uw	1.30uw	1.16uw
22nm	618nw	610nw	3.25uw	5.12uw	634nw	628nw
16nm	305nw	303nw	3.20uw	4.30uw	263nw	228nw

These Tables show that the power consumption of the NAND type and NOR type cells are not the same; as most of the power is consumed by the MTJs, the NOR type CAM requires one additional transistor than the NAND type, so there is a small difference in power consumption between these cells.

C. PVT variation

The search times of the proposed cells (for Miss and Match conditions) have been evaluated under PVT (process, voltage and temperature) variations at a 32nm feature size.

Figure 8. Plot of process variation for proposed CAM cells

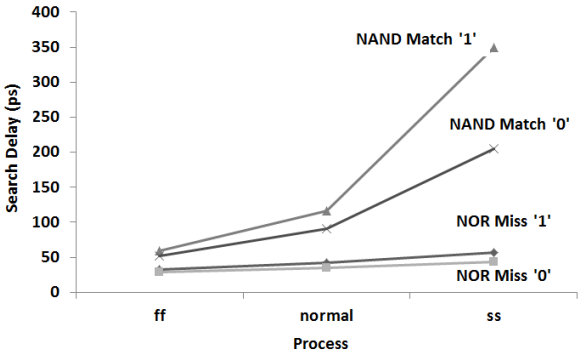


TABLE VI. SEARCH DELAY AT DIFFERENT VOLTAGE FOR PROPOSED CAM CELLS

V_{dd}	NOR type		NAND type	
	Miss 1	**Miss 0**	**Match 1**	**Match 0**
0.81V	46.7ps	37.0ps	236.2ps	143.2ps
0.855V	41.2ps	33.8ps	182.8ps	117.9ps
0.90V	37.6ps	31.1ps	146.1ps	99.9ps
0.945V	34.8ps	29.2ps	122.5ps	87.1ps
0.99V	32.5ps	27.6ps	105.0ps	80.0ps

TABLE VII. SEARCH DELAY AT DIFFERENT TEMPERATURE FOR PROPOSED CAM CELLS

Temp(℃)	NOR type		NAND type	
	Miss 1	**Miss 0**	**Match 1**	**Match 0**
0	33.5ps	27.6ps	142.2ps	89.3ps
25	37.6ps	31.1ps	146.1ps	99.9ps
50	42.8ps	35.5ps	156.5ps	111.2ps
75	48.9ps	40.0ps	167.4ps	124.2ps
100	55.3ps	45.7ps	178.2ps	142.7ps

Process: as process variation of the proposed cell, a 3 standard deviation simulation of the CMOS transistors is employed, such that the values of the MTJ resistances are also changed. The fast-fast ff (slow-slow ss) corner corresponds to a nearly 10 % increase (decrease) of R_{high} and a 10% decrease (increase) of R_{low}. Figure 8 shows the search delay at ff, ss and normal conditions. *Voltage:* under this variation, V_{dd} is changed by at most ±10%. The results are given in Table VI. *Temperature:* Temperature is varied in the range of 0 to 100 degree Celsius. The results are given in Table VII for both proposed cells.

TABLE VIII. PV VARIATION OF PROPOSED NOR TYPE CAM CELL

P / V	ff		normal		ss	
	Miss1	**Miss0**	**Miss1**	**Miss0**	**Miss1**	**Miss0**
0.81V	40.1ps	35.1ps	52.9ps	42.4ps	70.8ps	52.4ps
0.845V	36.2ps	32.1ps	46.7ps	38.7ps	62.5ps	47.8ps
0.9V	33.0ps	29.5ps	42.6ps	35.6ps	57.0ps	44.0ps
0.945V	30.5ps	27.7ps	39.4ps	33.4ps	52.7ps	41.3ps
0.99V	28.5ps	26.2ps	36.8ps	31.6ps	49.2ps	39.0ps

TABLE IX. PV VARIATION OF PROPOSED NAND TYPE CAM CELL

P / V	ff		normal		ss	
	Match 1	**Match 0**	**Match 1**	**Match 0**	**Match 1**	**Match 0**
0.81V	95.1ps	75.4ps	188.1 ps	129.5 ps	564.5 ps	293.2 ps
0.845V	73.6ps	62.1ps	145.5 ps	106.7 ps	436.7 ps	241.4 ps
0.9V	58.8ps	52.6ps	116.3 ps	90.4ps	349.1 ps	204.6 ps
0.945V	49.3ps	45.9ps	97.4ps	78.8ps	292.5 ps	178.4 ps
0.99V	42.3ps	42.0ps	83.6ps	72.3ps	251.0 ps	163.7 ps

The effect of simultaneously assessing process (P) and voltage (V) variations is also considered in this paper for the two proposed CAM cells under the two-value cases of mismatch (i.e. miss); the simulation results for normal, ff and ss corners are shown in Tables VIII and IX by considering both of them at the same time under the previously presented variation values.

V. EVALUATION

Table X shows the simulation results for the current and the power dissipation for the match/mismatch conditions at different feature sizes of the 2T2MTJ cell [9]. This cell requires current monitoring, so its search time is mostly determined by the current sensor. From the results found in a previous section, the 2T2MTJ CAM cell performs well with respect to power dissipation by utilizing small numbers of transistors and MTJs (two of each). However, this cell requires current monitoring. The significant disadvantage of a current monitored CAM is the design of the current sensor. The rather limited current range between match and mismatch (at 16nm case, the current range is only 7uA) of this cell creates further problems, hence requiring a very sensitive comparator.

TABLE X. CELL CURRENT AND POWER DISSIPATION FOR 2T2MTJ CAM CELL

	32nm	**22nm**	**16nm**
Ic Match	30.7uA	22.3uA	18.8uA
Ic Mismatch	18.2uA	13.9uA	11.8uA
Match Power	27.63uW	17.84uW	13.16uW
Mismatch Power	16.38uW	11.12uW	8.26uW

The current comparator structure of [12] [13] commonly used for these memory designs; it employs several inverter amplifiers to detect the current value. To generate the input of the current comparator, a current operational amplifier (opamp) is employed [13]. The output of the current opamp is equal to Ir-Ic. In this paper, the Ir value is given by the mid-level of the match and mismatch Ic range. The delay of the current comparator of [12] is given by 323ps, while its average power consumption is 8.89uW. Therefore, these findings confirm that a sensitive current sensor is complicated and adds considerable delay to the monitored CAM cells of [9] [10]. Moreover, its operation cannot be modularized at array level, i.e. for N cells to share a current comparator, the Match Lines must be connected in series, and thus the current range between match and mismatch is now given by 7/N uA, making comparison more difficult even at modest values of N. [10] has proposed a 4MTJ CAM cell. Table XI shows the simulation results of the current and the match/mismatch power for this cell.

TABLE XI. CELL CURRENT AND POWER FOR 4MTJ CAM CELL OF [10]

Ic Match	**Ic Mismatch**	**Match Power**	**Mismatch Power**
271uA	129uA	243.9uW	116.1uW

The 4MTJ CAM cell of [10] is relatively simpler than other cells, because it only uses MTJs, i.e. no transistor involved in the design. The range between match and mismatch for this cell is larger than for the 2T2MTJ CAM cell, because a pair of MTJs defines the search operation. However, the 4 MTJ CAM cell incurs in significant power dissipation, while still needing a sensitive current monitoring circuit. Tables XII and XIII show the power dissipation and the search delay of the different MTJ-based CAM cells considered in this paper.

TABLE XII. POWER DISSIPATION COMPARISON (32NM FEATURE SIZE)

	Match '1'	**Match '0'**	**Mismatch '1'**	**Mismatch '0'**
Proposed NOR	59.90uW	62.71uW	71.85uW	74.05uW
Proposed NAND	59.35uW	59.21uW	63.08uW	66.42uW
2T2MTJ [9]	36.52uW	36.52uW	25.27uW	25.27uW
4MTJ [10]	124.99uW	124.99uW	252.79uW	252.79uW

TABLE XIII. SEARCH DELAY COMPARISON (32NM FEATURE SIZE)

	Search '1'	**Search '0'**
Proposed NOR	37.6ps	31.1ps
Proposed NAND	146.1ps	99.9ps
2T2MTJ [9]	>323ps	>323ps
4MTJ [10]	>323ps	>323ps

TABLE XIV. COMPARISON OF DIFFERENT CAM CELLS (32NM FEATURE SIZE)

	Non-Volatile?	**Number of Ts and MTJs**	**Average Search Delay**	**Average Power**	**Average PDP**
Proposed NOR	Yes	6T2MTJ	34.4ps	82.1uW	2824uWps
Proposed NAND	Yes	5T2MTJ	123.0ps	63.2uW	7773uWps
2T2MTJ [9]	Yes	2T2MTJ +Sensor	>323ps	22.0uW + 8.89uW	9977uWps
4MTJ [10]	Yes	4MTJ +Sensor	>323ps	180.0uW + 8.89uW	61011uWps

Table XIV shows the comparison among the CAM cells Since the CAM cells of [9] and [10] require current monitoring, their delay is based on the sensor. The delay due to the sensor circuit of [12] [13] is at least 323ps at a 32nm feature size, because an operational amplifier is also required. As non-volatile MTJ-based cells, the proposed designs achieve considerable reductions in average search delay and PDP. Note that a SNM comparison is not applicable to [9] and [10] due to the current sensing operation of these cells.

VI. CONCLUSION

This paper has proposed two non-volatile CAM cells using Magnetic Tunneling Junctions (MTJs). The proposed cells utilize two MTJs (as a voltage divider) with a small number of transistors (6 for the NOR type and 5 for the NAND type) for voltage-based operation. The following conclusions are therefore applicable from the results presented in this paper. (a) The proposed CAM cells operate on a voltage-based mode for ease in the comparison/outcome notification of the CAM operation, thus avoiding the utilization of a current sensing circuitry (as required in [9] [10 (b) The proposed designs incur in an increase (decrease) in average power consumption compared to [9] ([10]); this is caused by the larger number of MOSFETs utilized in the proposed designs. (c) The proposed designs have very small search delay (for both all possible outcomes and average); these cells significantly improve over [9] and [10].

REFERENCES

[1] W. Xu, T. Zhang, and Y. Chen, "Design of Spin-Torque Transfer Magnetoresistive RAM and CAM/TCAM with High Sensing and Search Speed," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* ,vol. 18, pp. 66 – 74, January 2010.

[2] J. Das, B.Black, W.C., Jr., "A generalized HSPICE macro-model for pinned spin-dependent-tunneling devices", *Magnetics, IEEE Transactions on*, vol. 35, pp.2889-2891, September 1999.

[3] S. S. Mukherjee, S. K. Kurinec, "A Stable SPICE Macro-Model for Magnetic Tunnel Junctions for Applications in Memory and Logic Circuits", *Magnetics, IEEE Transactions on*, vol. 45, No. 9, pp.3260-3268, September 2009.

[4] Y. M. Lee, J. Hayakawa, S. Ikeda, F. Matsukura, and H. Ohno; "Giant tunnel magnetoresistance and high annealing stability in CoFeB/MgO/CoFeB magnetic tunnel junctions with synthetic pinned layer", Applied Physics Letters, Volume: 89, Issue 4, pp. 042506-042506-3, Jul, 2006.

[5] Z. Diao, Z. Li, S. Wang, Y. Ding, A. Panchula, E. Chen, L. Wang, and Y. Huai, "Spin-transfer torque switching in magnetic tunnel junction and spin-tansfer torque random access memory," *J. Phys.: Condens. Matter,* vol. 19, p. 165209, Apr. 2007.

[6] K. Pagiamtzis, "Content-addressable memory (CAM) circuits and architectures: A tutorial and survey," *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 712–727, Mar. 2006.

[7] W. D. Renu, "MgO-based tunnel junction material for high-speed toggle magnetic random access memory," *IEEE Trans. Magn*., vol. 42, no. 8, pp. 1935–1939, Aug. 2006.

[8] Qazi, M.; Sinangil, M.E.; Chandrakasan, A.P.; "Challenges and Directions for Low-Voltage SRAM," *IEEE Design & Test of Computers* , vol.28, no.1, pp.32-43, Jan.-Feb. 2011.

[9] Matsunaga, S., Natsui, M., Ikeda, S., Miura, K., Endoh, T., Ohno, H., Hanyu,T., "Implementation of a perpendicular MTJ-based read-disturb-tolerant 2T-2R nonvolatile TCAM based on a reversed current reading scheme", *Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific*, Jan. 30 2012-Feb. 2 2012, pp. 475 – 476, Mar. 2012.

[10] W. Wang, "Magnetic Random Accessible Memory Based Magnetic Content Addressable Memory Cell Design", *Magnetics, IEEE Transactions on*, vol. 46 issue 6, pp.1967-1970, June 2010.

[11] Ikeda,S.; Hayakawa, J. ; Ashizawa, Y.; Lee,Y.M.;Miura, K. ; Hasegawa, H., Tsunoda, M., Matsukura, F., Ohno, H., "Tunnel magnetoresistance of 604% at 300 K by suppression of Ta diffusion in CoFeB/MgO/CoFeB pseudo-spin-valves annealed at high temperature", *Applied Physics Letters,* Volume: 93, Issue: 8, pp. 082508 - 082508-3, Aug 2008.

[12] Tang, X., Pun, K.-P., "High-performance CMOS current comparator", *Electronics Letters*, Volume: 45, Issue: 20, pp. 1007-1009, Sep 2009.

[13] Y. Sun; Y. Ye; F. Lai, "Power efficient high speed switched current comparator", *ASIC, 2007. ASICON '07. 7th International Conference*, pp. 581-584, Oct. 2007.

[14] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits: A Design Perspective (2nd Edition)," Prentice Hall, 2003.