

# On the Drift Behaviors of a Phase Change Memory (PCM) Cell

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**Abstract**—This paper presents a HSPICE macromodel of a phase change memory (PCM) by considering the phenomenon of drift behavior as leading to incorrect operation. The model simulates the behavior due to the drift in the resistance and threshold voltage when the cell is not been read or programmed. It considers not only the resistance change by phase (as corresponding to the two phases, amorphous and crystalline), but also the temperature, the crystalline fraction and the continuous profile of the resistance. This electrical based modeling by HSPICE allows to fully characterizing the holding voltage and the continuous behavior of the PCM resistance, while assessing the impact of the programming time of the drifted parameters. The proposed macromodel generates the I-V and R-I plots of a PCM cell at a very small error compared with experimental data. A detailed sensitivity analysis of the electrical parameters of the PCM cell is pursued to show the robust characteristics of the proposed macromodel to capture the variation in parameters due to drift.\*

## I. INTRODUCTION

With the fast growing market of consumer electronics and the increased demand on large storage, new non-volatile memories (NVMs) are attracting attention to meet the technological challenges of CMOS. Phase change memories (PCM) [1] have been advocated for replacing flash memories, because a PCM cell is not only significantly faster and smaller, but it is also very reliable (up to 100 million write cycles) [2]. The integration of a PCM into an IC requires tool compatibility for simulation, such as HSPICE. HSPICE allows establishing the electrical characteristics of the operation of a PCM cell and facilitating its interface with peripheral circuits and other functional blocks for chip design [1]. A comprehensive assessment of a PCM cell however, remains elusive; many simulation models based on HSPICE can be found in the technical literature. These models are accurate, but they focus on specific parameters, thus often not fully addressing important operational features. Among these features, the drift behavior of a PCM cell is very important for its commercialization. Drift negatively affects two parameters, the resistance and the threshold voltage. Changes in these parameters cause malfunctioning of the memory, thus affecting its correctness and storage capabilities. The drift behavior of a PCM cell is dependent on programming time

and the resistance range. Resistance drift is not significant for a binary PCM cell because its range increases over time; however for multilevel storage, the drift adversely affects cell operation because the distance between adjacent levels is small and over time, stochastic fluctuations of the resistance are likely to cause an overlap [3].

In this paper, the HSPICE-based *macromodel* of a PCM cell of [4] is extended to the drift behaviors. The proposed PCM macromodel is versatile, comprehensive and is used to assess drifts in threshold voltage and resistance by utilizing temperature profiling effects and the crystalline fraction of a PCM cell. This electrical based model by HSPICE allows to *fully characterizing* the holding voltage and the continuous behavior of the PCM resistance. So differently from previous models (such as [1]), the proposed macromodel also incorporates resistance and threshold voltage drifts to comprehensively simulate and assess a PCM. Simulation results are presented; they show that the proposed macromodel is very accurate and robust (following an extensive analysis of parameter sensitivity).

## II. REVIEW

In a Phase Change Memory (PCM), data storage relies on the reversible phase transformation of the chalcogenide alloy (e.g.  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ , GST) between the amorphous and the crystalline phases. The amorphous phase has a high resistance and is commonly referred to as the *reset state*; the crystalline phase has a low resistance and is referred to as the *set state* [5]. The PCM device is fabricated by using a thin film chalcogenide layer in contact with a metallic heater. A pulse with a high amplitude is used to melt and quench the PC element to an amorphous phase (*Reset State*), while a longer pulse with a low amplitude is used to crystallize the PC element to a crystalline phase (*Set State*) [1]. Since switching between the amorphous and crystalline phases is based on the crystalline fraction of the PCM, the *electrical resistance* of the PCM cell is given as

$$R_{\text{PCM}} = (1 - C_x)R_a + C_xR_c \quad (1)$$

Where  $R_c$  and  $R_a$  are the resistances of the PCM when it is fully crystalline and amorphous respectively.  $C_x$  is the *crystalline fraction*: when  $C_x$  is equal to zero, the PCM is fully amorphous; when  $C_x$  is equal to one, the PCM is fully crystalline [5].

Figure 1 shows the I-V characteristics of the PCM cell; the phases of PCM are clearly exhibited. Figure 1 shows that if the PCM is in the Reset state (amorphous) and the voltage across the PCM cell is higher than the *threshold value* ( $V_{\text{th}}$ ), then a snapback behavior occurs and the resistance of the PCM is changed to the  $R_{\text{ON}}$  (ON state) value. If the PCM is in the ON state, its voltage drifts by the holding voltage ( $V_{\text{h}}$ ) and it will switch back to the OFF state

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(set or reset state) if and only if the voltage across the PCM is less than the *ON/OFF Intersection Point* ( $V_X$ ). In Figure 1, the threshold voltage of PCM cell is approximately 0.75V, while the holding voltage ( $V_H$ ) and the ON/OFF intersection point of the PCM cell ( $V_X$ ) are approximately 0.45V and 0.53V respectively.

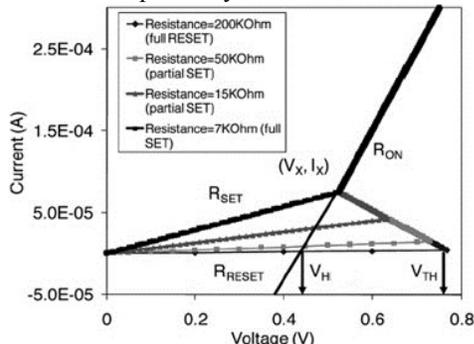


Figure 1. I-V Characteristic of PCM cell when it's in Set, Reset, Partial Set, and Partial Reset State [6].

To simulate the electrical characteristics of a PCM, different models have been proposed in the technical literature. [5] has presented a compact SPICE model with Verilog-A; the resistance of the PCM is based on (1); however, [5] is unable to simulate the I-V curve of a PCM, because it does not consider the holding voltage and the crystallized rate. [1] has presented a detailed HSPICE model; however, the change in resistance of a PCM is not continuous and the holding voltage is not considered, thus failing to generate the I-V curve. In addition to the above three, other models can be found in the technical literature [6, 7, 8, 9]; however, these models encounter the same limitations and disadvantages, such as ignoring the holding voltage, discontinued behavior of the PCM resistance, lacking of verification with simulation data, or utilization of model parameters that are not compatible with an HSPICE simulation environment.

### III. MACROMODELING

This section presents the basic principles of the proposed model; this is a macrolevel model (hereafter referred to as *macromodel*) and its flow chart is shown in Figure 2 of [4]. The macromodel consists of two models: the *basic model* and the *advanced model*. For the basic model (shown in the flowchart in Figure 2), the input and output voltages are provided to the PCM circuit (Figure 3a) to establish its state (ON or OFF) and calculate the resistance. Figure 3a shows the circuit model of the PCM cell; nodes *in* and *out* are the input and output nodes in Figure 2. When there is a voltage difference across *in* and *out*, the *Control ON State* blocks (Figure 2) checks the state of the PCM, i.e. ON or OFF. If it is the ON state, the switch *sw2* is ON, while switch *sw1* is OFF. The resistance of the PCM is reduced to the  $R_{ON}$  value. The voltage source  $V_H$  is added to simulate the holding voltage in the I-V characteristics of the PCM. When the PCM is in the OFF state, the switch *sw1* is ON, while the switch *sw2* is OFF. The resistance of the PCM cell is based on the crystalline fraction of the PCM as calculated using (1).

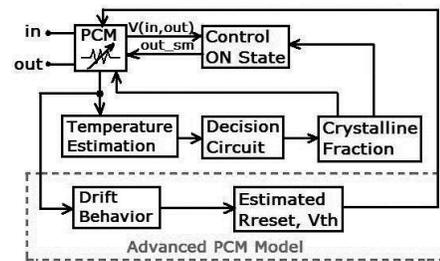


Figure 2. Flowchart of the proposed PCM macromodel.

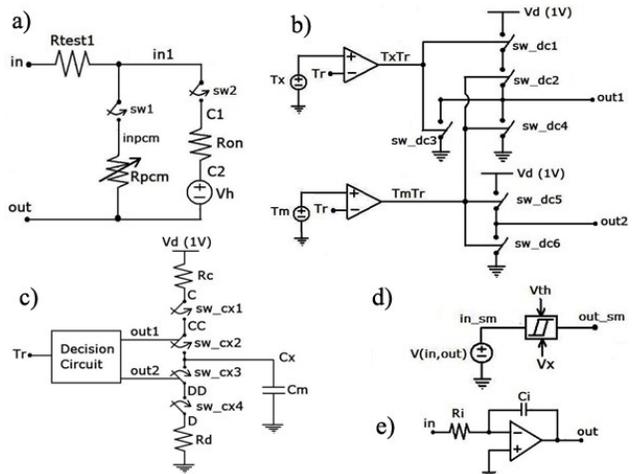


Figure 3. Basic model of Phase Change Memory (PCM) cell a) Main circuit b) Temperature Comparator (Decision Circuit) c) Crystalline fraction calculation circuit d) Control Switch Circuit e) Integrator Circuit

After establishing the state and the resistance of the PCM cell, the temperature is found as in [5] and a decision circuit (Figure 3b) is used to find the behavior of the PCM. Let  $T_r$  correspond to the temperature estimate of the PCM; to check whether the PCM is in the programming state, the temperature must be compared with the glass transition point ( $T_x$ ) and the melting point ( $T_m$ ). If the temperature of the PCM cell is less than  $T_x$ , the resistance remains the same. If the temperature is higher than  $T_x$  but lower than  $T_m$ , then the PCM is programmed to the *crystalline phase*. However if the temperature of the PCM is higher than  $T_m$ , then the PCM is programmed to the *amorphous phase*. Based on the decision circuit (Figure 3b), the voltage at node TxTr represents the voltage difference between  $T_x$  and  $T_r$ , while the voltage at node TmTr represents the voltage difference between  $T_m$  and  $T_r$ . In the decision circuit (Figure 3b), when the voltage at node TxTr is positive, the switch *sw\_dc1* is OFF, while switch *sw\_dc3* is ON. When the voltage at node TmTr is positive, switches *sw\_dc2* and *sw\_dc6* are ON while switches *sw\_dc4* and *sw\_dc5* are OFF. So, the programming behavior of the PCM cell is fully controlled. The crystalline fraction calculation circuit (Figure 3c) is employed for varying the crystalline fraction ( $C_x$ ) of the PCM cell. Switches *sw\_cx2* and *sw\_cx3* depend on the output voltage of the decision circuit that controls the programming behavior of the PCM cell; the switches *sw\_cx1* and *sw\_cx4* are ON when the PCM is in the ON state. The ON/OFF state of the circuit must be considered next; a Schmitt Trigger (Figure 3d) is employed to control

the ON/OFF state of the circuit. The state of the circuit (ON/OFF) is controlled by comparing the voltage difference across the bitline with the threshold and the ON/OFF intersection point voltages.

However, based on the I-V characteristics of the PCM (Figure 1), the programming behavior of the cell is related to the threshold voltage and the crystalline fraction. If the PCM cell is in the amorphous or intermediate phase, voltage across it must be higher than its threshold value ( $V_{th,new}$ ) for programming to take place. If the PCM is in the crystalline phase, the voltage across it must be higher than  $V_x$  for programming to take place.

The relationship between the threshold voltage and the crystalline fraction ( $C_x$ ) can be expressed as follows.

$$V_{th,new} = V_{th} + (V_x - V_{th}) * C_x \quad (2)$$

where  $V_{th,new}$  is the threshold voltage of the PCM cell when its crystalline fraction is varied (i.e. not constant),  $V_{th}$  is the threshold voltage of the PCM cell when the crystalline fraction is equal to zero,  $C_x$  is the crystalline fraction of the PCM cell and is calculated from the voltage at node Cx of Figure 3c.  $V_x$  is the intersection point of the ON and OFF states (as shown in Figure 1); its value is given by

$$V_x = \frac{V_h R_{set}}{R_{set} - R_{ON}} \quad (3)$$

Where  $V_h$  is the holding voltage,  $R_{set}$  is the resistance of the PCM cell when it is in the full crystalline phase, and  $R_{ON}$  is the resistance of the PCM cell when it is in the ON-state.

Next, a discussion of a recently proposed PCM macromodel [1] is pursued. Consider the circuit of the model of [1]; the PCM resistance is switched to  $R_m$  when the PCM is in fully amorphous phase and the temperature is higher than the melting point ( $T_m$ ). So, the rate of change of the resistance of the PCM is not considered in [1] because the time of the write operation from the amorphous to the crystalline phases (or vice versa) is erroneously based on the delay encountered by the macromodel circuit, not its simulated value. The logic control circuit of [1] finds that the PCM resistance is always given by  $R_x$  when the temperature of the PCM is less than  $T_m$  and  $R_m$  when the temperature of the PCM is higher than the melting point and  $C_x$  is less than 100%. However if the temperature of the PCM is higher than the melting point and the crystalline fraction is 100%, then the PCM resistance is based on the previous state of PCM cell. So, when the voltage difference across the PCM is very small (such as during a read operation), the PCM resistance is always given by  $R_x$  as incorrect value. Figure 4 shows the PCM resistance of the macromodel of [1] when the voltage difference across the PCM cell is varied; these results show that the PCM macromodel of [1] is incomplete, because when the crystalline fraction of the PCM cell ( $C_x$ ) is set to 0% (amorphous phase) and the voltage drop across the PCM cell is very low (such as 0.1V), the resistance of PCM cell [1] is incorrectly given by 7k $\Omega$ ; moreover, when the crystalline fraction of the PCM cell is 100% and the voltage difference across PCM cell is large, the macromodel of [1] incorrectly does not switch the PCM to the ON-state.

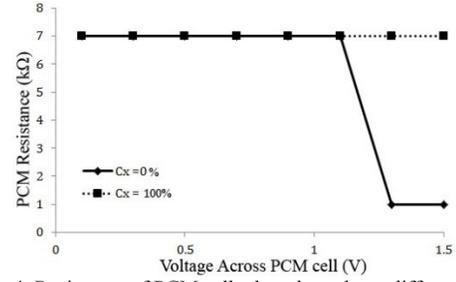


Figure 4. Resistance of PCM cell when the voltage difference across it is varied using [1]

Also, the initial state must be established in [1]; this model [1] must establish the programming operation of the PCM cell prior to the execution of any read operation, thus incurring in a more complex simulation process than the proposed PCM macromodel.

#### IV. PROPOSED DRIFT MODEL

In the previous section, the basic model of a PCM [4] has been described by ignoring the drift in  $R_{reset}$  and  $V_{th}$  as well as the change in write time when the resistance range of the PCM ( $R_{reset} - R_{set}$ ) is changed. In this section, these features are addressed. In the basic model, when the resistance range (range =  $R_{reset} - R_{set}$ ) is changed, the programming time is still assumed to remain the same, i.e. at a constant value. Since the programming time is *nearly linear dependent* on the resistances and its range, the resistance difference between the fully amorphous phase and the fully crystalline phase is ( $R_{reset} - R_{set}$ ). So for example in [7]  $R_{reset}$  and  $R_{set}$  are given by 200k and 7k respectively; the programming time of the Reset state ( $T_{reset}$ ) is 10ns and programming time of the Set state ( $T_{set}$ ) is 200ns. The values of the resistors  $R_c$  and  $R_d$  [4] also determine the *programming time*. So using the data in [7], the values of  $R_c$  and  $R_d$  in the crystalline fraction calculation circuit are given as follows.

$$R_c = \frac{290 * range}{193 * 10^3} \quad (4)$$

$$R_d = \frac{15 * range}{193 * 10^3} \quad (5)$$

[10] has shown that when the PCM is programmed to the amorphous phase, the resistance ( $R_{reset}$ ) and the threshold voltage ( $V_{th}$ ) change as function of the so-called non-programming time ( $T_{off}$ ). This phenomenon is usually referred to as *drift*. The drifts of the reset resistance and the threshold voltage are calculated as follows [10] (under the assumption that the annealing temperature of PCM cell is assumed to be constant).

$$R = R_0 \left( \frac{T_{off}}{T_0} \right)^{v_r} \quad (6)$$

$$V_T = V_{T0} + \Delta V_T \left( \frac{T_{off}}{T_0} \right)^{v_t} \quad (7)$$

where  $R$  and  $V_T$  are the amorphous (Reset) resistance and the threshold voltage drift respectively,  $R_0 = 1.28M\Omega$ ,  $T_0 = 1s$ ,  $V_{T0} = 0.55V$ ,  $\Delta V_T = 0.46$  and the exponents  $v_r = 0.077$ ,  $v_t = 0.074$  [10].

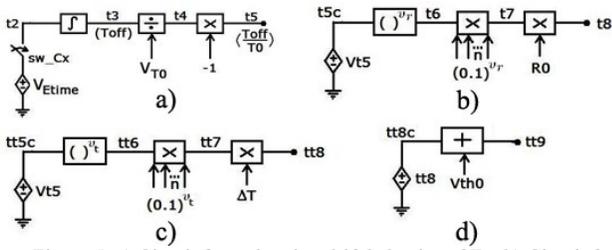


Figure 5. a) Circuit for estimating drift behavior of  $T_{\text{off}}$  b) Circuit for estimating drift behavior of  $R_{\text{reset}}$  c) Circuit for initial estimate of drift behavior of  $V_{\text{th}}$  d) Circuit for final estimate of drift behavior of  $V_{\text{th}}$

Using (6) and (7), the drifts of the Reset resistance and the threshold voltage of a PCM cell are modeled as follows. Figure 5a shows the circuit model for the timing calculation ( $T_{\text{off}}$ ), where  $T_{\text{off}}$  denotes the time when the PCM is in the amorphous phase, and it's not reading or programming. A voltage source ( $V_{\text{Etime}}$ ) is used for checking the behavior of the PCM cell (reading, programming or neither), while the switch  $\text{sw\_Cx}$  is used to check the state of the PCM cell. For checking the behavior of the PCM cell, a voltage source  $V_{\text{Etime}}$  is varied depending on the voltage across the PCM cell ( $V_{\text{in,out}}$ ); so, the behavior of PCM cell is given as follows. (a) If  $V_{\text{in,out}}$  is low (i.e. the PCM cell is not been read or programmed), the voltage  $V_{\text{Etime}}$  is equal to  $V_{\text{DD}}$  (1V, in this case) and the calculation of  $T_{\text{off}}$  in Figure 5a can start. (b) If  $V_{\text{in,out}}$  is high (i.e. the PCM cell is read or programmed),  $V_{\text{Etime}}$  is equal to GND, so the  $T_{\text{off}}$  calculation is stalled.

The switch  $\text{sw\_Cx}$  is used (Figure 5a) for checking the PCM state. The switch  $\text{sw\_Cx}$  is ON if the PCM cell is in the amorphous phase (the voltage at node  $C_x$  is in the amorphous region); else, it is OFF. In Figure 5a, the input voltage (node t2) is provided to the integrator circuit as shown in Figure 3e to find  $T_{\text{off}}$ ; it is then divided by  $V_{T0}$  (as in (6) and (7)), and multiplied by -1 to make it positive. The voltage at node t5 represents the value of  $T_{\text{off}}/T_0$  that is used to establish the drift behaviors of  $R_{\text{reset}}$  and  $V_{\text{th}}$  in (6) and (7). The estimates of these drift behaviors are analyzed next.

#### 1) Reset Resistance ( $R_{\text{reset}}$ )

A voltage controlled voltage source ( $Vt5$ ) is used; it has a value equal to the output voltage at node t5 in the  $T_{\text{off}}$  calculation circuit (Figure 5a). Based on (6), this voltage is used as input for the base. Consider next  $v_r$ , i.e. the exponent. The input voltage of the exponent circuit [11] is limited in its range (0.1V to 10V) as dependent on the simulation time. For a simulation time in the range of 0.1-10 seconds, the voltage at node t6 corresponds to the value  $(\frac{T_{\text{off}}}{T_0})^{v_r}$ . If the simulation time is less than 0.1 second, then the integrator of Figure 3e must be adjusted for the output to be in the acceptable range (0.1V to 10V). So, the circuit for calculating  $0.1^{v_r}$  is replicated  $n$  times and multiplied at node t6 (Figure 5b) to calculate  $(\frac{T_{\text{off}}}{T_0})^{v_r}$ ; note that the value of  $n$  is dependent on the simulation time, i.e. if the simulation step is 1 ns, the value of  $n$  is equal to 8 because the value of  $(\frac{T_{\text{off}}}{T_0})$  is about 0.1V and  $0.1^8 = 0.1^{9v} = (10^{-1})^{9v} = (10^{-9})^v$

$= (1\text{ns})^v$ . After the above calculations,  $R_0$  is multiplied to obtain  $R_{\text{reset}}$  as the drift value at node t8 (Figure 5b).

#### 2) Threshold voltage

The drift behavior of the threshold voltage of the PCM cell is similar to the  $R_{\text{reset}}$  drift behavior; however, some adjustments are required. The circuit in Figure 5c is now used to simulate the drift behavior of the threshold voltage ( $V_{\text{th}}$ ). The  $V_{\text{th}}$  drift behavior is similar to the  $R_{\text{reset}}$  drift behavior; in addition to obvious modifications (such as changes in values from  $v_r$  to  $v_t$ ,  $R_0$  to  $\Delta T$ ), the voltage at node tt8 is duplicated in the circuit of Figure 5d, then it is added to the voltage  $V_{\text{th0}}$ . The drift behavior of the threshold voltage ( $V_{\text{th}}$ ) is given at node tt9.

Previously, the drift behaviors of the PCM model parameters were established; these values ( $R_{\text{reset}}$  and  $V_{\text{th}}$ ) are provided to the basic model of [4]. As the parameters  $R_{\text{reset}}$  and  $V_{\text{th}}$  are changed, then the operation of the basic model is changed as follows. (a) For the drift behavior of the Reset resistance, the value of  $R_{\text{reset}}$  (corresponding to the voltage at node t8) is substituted with  $R_a$  in (1) and  $R_{\text{reset}}$  in (4) and (5). (b) For the drift behavior of the threshold voltage,  $V_{\text{th}}$  must be varied as function of time and the crystalline fraction of the PCM cell (in (2)). By combining these characteristics, the threshold voltage drift that is calculated at node tt9 (from (7)), is used as the threshold voltage when the crystalline fraction is 0. Therefore, it can be combined with the variation of the crystalline fraction (as given in (2)).

## V. SIMULATION

By using the data in [5] for the temperature calculation, [7] for the physical parameters, and [10] for the degradation calculation, the whole macromodel is simulated. Table 1 shows the physical parameters of the PCM cell that are used in the simulation. The parameters at electrical level for HSPICE simulation are selected as follows. (1) To estimate the simulation time for the temperature calculation [4], a very fast input voltage (from 0 to 1V) must be provided to the input of an integrator (Figure 3e). The output of the integrator is then multiplied by  $-10^{-4}$  by using a voltage multiplier circuit [11]. (2) After the simulation time above, the output voltage must undergo a further multiplication by  $10^{-4}$  for the temperature calculation to obtain the final simulation time of the PCM cell. The reason for the double multiplication (one after the integrator and one during the temperature calculation) is that the output of the integrator circuit has a very small value and a single multiplication by  $-10^{-8}$  would make it to drop to nearly zero, thus generating an erroneous temperature calculation. Moreover, the input voltage of the integrator must be a very fast pulse voltage (from 0 to 1V), not a constant value. (3) For calculating  $T_{\text{off}}$  (Figure 5a), the value of  $V_{\text{Etime}}$  is set to 1V if  $V_{\text{in,out}}$  is less than 0.1V (no read or programming); however, it is 0V if  $V_{\text{in,out}}$  is higher than 0.1V. (4) The models of [11] are used for the voltage divider and multiplier circuits; in the integrator (Figure 3e),  $R_i$  is 1  $\Omega$  and  $C_i$  is 10nF. (5) For the Reset drift calculation using the circuit in Figure 5b, the number of times ( $n$ ) that the circuit for calculating  $0.1^{v_r}$  must be replicated, is 8 for 1 nanosecond (as explained previously).

TABLE I. PHYSICAL PARAMETERS FOR PCM SIMULATION

Parameters	Value
Radius of active region ( $r_1$ )	50 nm
Radius of PCM cell ( $r_2$ )	100 nm
Thermal conductivity of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (k)	$4.63 \cdot 10^{-3} \text{ J.cm.K}^{-1}.\text{S}^{-1}$
Thermal capacity of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (C)	$1.25 \text{ J.cm}^{-3}.\text{K}^{-1}$
Volume of PCM cell (V)	$7 \cdot 10^{-14} \text{ cm}^3$
Glass Transition Point ( $T_x$ )	200 C
Melting Point ( $T_m$ )	600 C
Static resistance of reset ( $R_{\text{reset}}$ )	200 k $\Omega$
Static resistance of set ( $R_{\text{set}}$ )	7 k $\Omega$
Dynamic-On Resistance ( $R_{\text{on}}$ )	1 k $\Omega$
Threshold Voltage ( $V_{\text{th}}$ )	0.78 V
Holding Voltage ( $V_{\text{h}}$ )	0.45 V
Programming time of Reset ( $T_{\text{reset}}$ )	10 ns
Programming time of Set ( $T_{\text{set}}$ )	200 ns

To assess the electrical characteristics of a PCM cell, the so-called R-I curve must be generated; this plot allows to test the validity of the proposed macromodel with data obtained from fabricated devices. A pulse sequence must be provided for generating the R-I curve; this sequence consists of Reset, Read and Set pulses with increasing amplitude for the Set pulse until it reaches the same amplitude as the Reset pulse [2]. The simulated R-I curve of the PCM is given in Figure 6a.

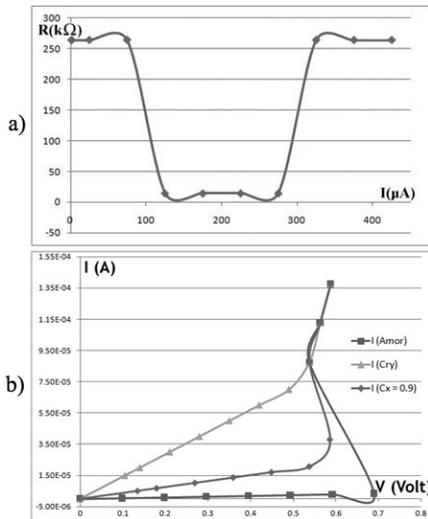


Figure 6. a) I-R curve of PCM cell b) I-V curve of PCM cell

Figure 6b shows the simulation-generated I-V curve of the PCM cell when its initial state is full amorphous ( $C_x = 0$ ), full crystalline ( $C_x = 1$ ), or partial ( $C_x = 0.9$ ). The simulation results show that the snapback behavior of the PCM cell is generated by the proposed macromodel and the threshold voltage is dependent on the crystalline fraction; this plot closely resembles Figure 1 [6]. A comparison between the proposed macromodel and the experimental characterization of [10] (i.e. (6) and (7)) is pursued next. Figure 7 shows both of these plots; the proposed PCM macromodel generates the I-V plot that closely resembles the experiment data of [10] by considering all the electrical features of a PCM. By considering a constant number of circuits for the calculation of  $0.1^v$  (i.e. 8) in the macromodel, the degradation in the values of  $R_{\text{reset}}$  and  $V_{\text{th}}$  due to drift are also found.

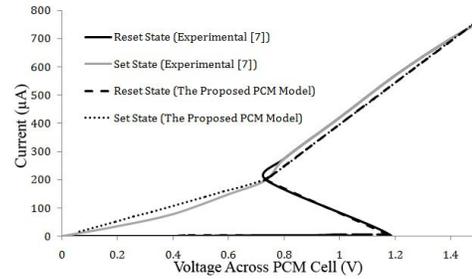


Figure 7. I-V plots of PCM cell from experimental data [10] and proposed PCM macromodel

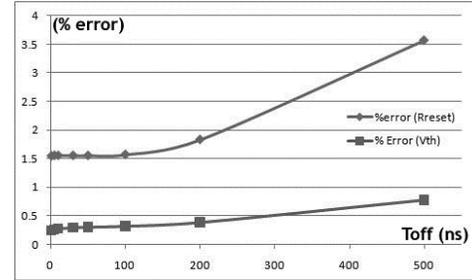


Figure 8. Percentage error in drift of  $R_{\text{reset}}$  and  $V_{\text{th}}$  between macromodel and experimental data of [10]

The plots for the error are shown in Figure 8; when  $T_{\text{off}}$  is less than 100ns, the errors (in percentage) for  $R_{\text{reset}}$  and  $V_{\text{th}}$  are very low and nearly constant. However, when  $T_{\text{off}}$  increases, the error percentage increases over time because the accuracy of the exponentiation circuit in the proposed macromodel is limited to an input voltage from 0.1 to 10V.

Next, the sensitivity of the proposed macromodel to different parameters is assessed with respect to the I-V characteristics. In all cases only a single parameter is changed at a  $\pm 5\%$  level (i.e. all other parameters are left unchanged to their default values).

TABLE II. SUMMARY OF PARAMETERS SENSITIVITY

Variation Parameter	Sensitive Parameter
$R_{\text{reset}}$	$R_{\text{reset}}, T_{\text{reset}}, R_{\text{PCM}}$
$R_{\text{set}}$	$R_{\text{set}}, T_{\text{set}}, R_{\text{PCM}}, V_{\text{th}}, V_x$
$R_{\text{ON}}$	$R_{\text{ON}}, V_{\text{th}}, V_x$
$V_{\text{th}}$	$V_{\text{th}}$
$V_{\text{h}}$	$V_{\text{th}}, V_x, V_{\text{h}}$

Table 2 shows the summary of the sensitivity of each parameter. Table 2 shows that only the variations in the threshold voltage ( $V_{\text{th}}$ ) is not affected by other parameters. However for the other parameters, any variation causes changes especially, in  $R_{\text{set}}$ ,  $R_{\text{ON}}$ , and  $V_{\text{h}}$  (i.e. for  $V_x$  in (3)) and also in  $V_{\text{th}}$  (as in (2)). Based on (1), the variations of  $R_{\text{reset}}$  and  $R_{\text{set}}$  result in a change of  $R_{\text{PCM}}$  when the crystalline fraction of PCM is not zero ( $C_x \neq 0$ ). Also the write time ( $T_{\text{reset}}$  and  $T_{\text{set}}$ ) changes upon variation of  $R_{\text{reset}}$  and  $R_{\text{set}}$ . So while a variation of  $V_{\text{th}}$  has no effect (i.e. it only affects itself),  $R_{\text{set}}$  is the parameter that is sensitive to most parameters.

**Reset Resistance ( $R_{\text{reset}}$ ):** The results of varying the reset resistance ( $R_{\text{reset}}$ ) are given in Tables 3 and 4. As described previously, a change in the value of the reset resistance ( $R_{\text{reset}}$ ) affects the write time (as shown in Table 3) in nearly a linear fashion. Moreover based on (1), the PCM resistance

( $R_{PCM}$ ) is dependent on the crystalline fraction ( $C_x$ ),  $R_{set}$  and  $R_{reset}$ . When reset resistance is changed, the new values of  $R_{PCM}$  (at the same crystalline fraction) are given in Table 4.

TABLE III. WRITE TIME ( $T_{RESET}$ ) WHEN  $R_{RESET}$  IS VARIED

% Variation	Reset Resistance (k $\Omega$ )	PCM Resistance Range (k $\Omega$ )	Write Time, $T_{reset}$ (ns)
0	200	193	10
-5	190	183	9.482
+5	210	203	10.518

TABLE IV.  $R_{PCM}$  AT THE SAME CRYSTALLINE FRACTION

% Variation	$R_{reset}$ (k $\Omega$ )	$R_{PCM}$ (k $\Omega$ )		
		$C_x = 0$	$C_x = 0.5$	$C_x = 1$
0	200	200	103.5	7
-5	190	190	98.5	7
+5	210	210	108.5	7

**Set Resistance ( $R_{set}$ ):** Based on (3), the ON/OFF intersection point of PCM ( $V_x$ ) is dependent on  $R_{set}$ ; the plot of  $V_x$  versus  $R_{set}$  is shown in Figure 9.

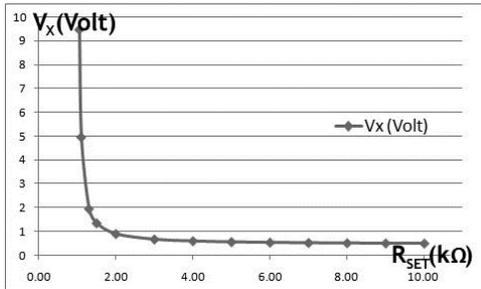


Figure 9. ON/OFF state intersection point ( $V_x$ ) Vs Set resistance ( $R_{set}$ )

When  $R_{set}$  is higher than 2k $\Omega$ ,  $V_x$  reaches a steady value because ( $R_{set} - R_{ON}$ ) is higher than 1k $\Omega$  (as in (3)), and therefore  $V_x$  is less than  $V_h R_{set}$ . This confirms the sensitivity of  $V_x$  at low values of  $R_{set}$  thus showing the criticality of the Set resistance in the operation of a PCM cell.

**Threshold Voltage ( $V_{th}$ ):** The threshold voltage ( $V_{th}$ ) under a variation of  $R_{set}$  depends on  $V_x$  and  $C_x$  (as per (2)). If the PCM cell is in a fully amorphous phase ( $C_x = 0$ ) the threshold voltage is 0.78V. Table 5 shows the threshold voltage when the crystalline fraction ( $C_x$ ) is varied. At a fixed crystalline fraction (and  $C_x \neq 0$ ), Table 5 shows that the threshold voltage has a minor inverse sensitivity to  $R_{set}$ .

TABLE V. THRESHOLD VOLTAGE OF THE PCM WHEN  $R_{SET}$  IS VARIED

% Variation	$R_{set}$ (k $\Omega$ )	$V_{th}$ (Volt)			
		$C_x = 0$	$C_x = 0.1$	$C_x = 0.5$	$C_x = 1$
Normal	7	0.78	0.7545	0.6525	0.5250
-5%	6.65	0.78	0.7550	0.6548	0.5296
5%	7.35	0.78	0.7541	0.6504	0.5209

**ON-State Resistance ( $R_{ON}$ ):** The variation of  $R_{ON}$  mostly affects the ON/OFF Intersection Point ( $V_x$ ). Based on (3),  $V_x$  changes as  $R_{ON}$  is changed. The relationship between  $V_x$  and  $R_{ON}$  is shown in Figure 10. When the value of  $R_{ON}$  is close to  $R_{set}$  (7k $\Omega$ ), the value of  $V_x$  quickly increases (as in (6)). However the value of  $R_{ON}$  cannot be higher than  $R_{set}$ , else

the holding voltage ( $V_h$ ) will be negative and the PCM cell will be incorrectly modeled. The sensitivity of  $V_x$  occurs at higher values of  $R_{ON}$ , thus having more impact on the intersecting point voltage.

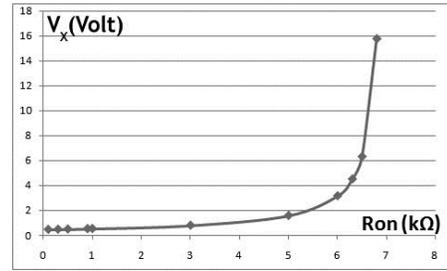


Figure 10. Relationship between ON/OFF intersection point ( $V_x$ ) and ON resistance ( $R_{ON}$ )

## VI. CONCLUSION

In this paper, a HSPICE macromodel of a PCM cell under drift of different parameters has been proposed. This macromodel matches the electrical characteristics with the operational features of PCM; so it's able to comprehensively assess the cell with respect to different features (such as the temperature profile and the crystalline fraction during the programming operation) under drift behavior in the resistance and threshold voltage. This deleterious phenomenon is commonly encountered in PCM operation, leading to incorrect storage. This paper has also shown that the I-V and I-R curves of a PCM cell are found at very small error compared with experimental data. This model for drift behavior is versatile and robust with respect to different operational features (such as the PCM state change and programming process) and parameter sensitivity (found in both drift behaviors of threshold voltage and resistance).

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