A robust wire crossing design for thermostability and fault tolerance in quantum-dot cellular automata

Yongqiang Zhang[a], Guangjun Xie[a*], Jie Han[b]

[a] *School of Electronic Science and Applied Physics, Hefei University of Technology, Hefei, 230009, China*

[b] *Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, T6G 1H9, Canada*

ABSTRACT

Quantum-dot cellular automata (QCA) present an unconventional computing model in the nanometer regime. The applications in QCA require complex wire crossings between intersectional wires. The existing wire crossing schemes show low fault tolerance or thermal stability. In this paper, a robust wire crossing scheme is proposed by using two opposite clock zones and redundant cells. The thermostability and fault tolerance are illustrated by using statistical analysis and fault simulations with regard to cell undeposition. This paper also presents a new signal distribution network (SDN) using the proposed wire crossings. The layouts of an XOR gate and a full adder are investigated to show the scalability of the proposed designs to circuits for logic functions with various number of inputs. For the proposed wire crossing and SDN, the circuitries of metal wires to provide the electric fields for driving the involved cells in each clock zone are also discussed. The functionalities of these circuits are validated by using QCADesigner.

Keywords: Coplanar wire crossing, Robustness, Clocking schemes, Quantum-dot cellular automata

1. Introduction

The continuous downscaling of the feature size of complementary metal oxide semiconductor devices has significantly increased the integration density, while it also introduced several challenges such as leakage power dissipation and short-channel effects [1, 2]. Quantum-dot cellular automata (QCA) provide a promising computing model in the nanoscale regime for solving such problems [3]. A QCA cell typically consists of four quantum dots and two free mobile electrons that can quantum-mechanically tunnel between these dots. The binary information in QCA is expressed by the locations of electrons. As shown in Fig. 1(a), two stable configurations of electrons representing two polarizations can be used to encode binary information due to the Coulomb interaction between these electrons. By an appropriate arrangement of cells, a majority voter in QCA is implemented as shown in Fig. 1(b). With the diagonal configuration of cells, an inverter is then realized as shown in Fig. 1(c) [3]. To achieve the steady operation of a system at ambient working temperature, nanomagnetic logic and molecular QCA may be hopeful in physical implementations [4, 5]. Recently, silicon atom dangling bonds were successfully realized to implement logic gates on an H-Si (100)-2×1 surface [6-8].

To control the direction of signals propagation in cells and ensure a circuit to remain in the instantaneous ground state, the quasi-adiabatic switching mechanism was introduced and it results in four clock zones [9]. Each zone is composed of four phases: switch, hold, release, and relax, as shown in Fig. 2. Taking the clock0 as an example, the inter-dot barrier will gradually increase during the switch phase from t=0 to t=π/2 and then peaks in the hold phase. During the hold phase in clock0, the cells in clock1 are polarized by cells in clock0. After the hold phase, the tunnel barrier continually decreases in the release phase in clock0, while the cells in clock1 keep polarized. When the inter-dot barrier reaches the minimum value, the cells completely lose polarizations and do not have any influence on neighboring cells while getting ready for the next cycle at t=2π. Data will be propagated from the hold phase in clock0 to the next one in clock1, then to clock2 and finally to clock3 as the arrow lines denoted. One should note that the cells in clock0 are in the hold phase while the cells in clock2 remain relaxed, which means that these two clocks are opposite, and two kinds of cells do not affect each other.

Fig. 3 shows the implementation of metal wires for providing electric fields to control the inter-dot barrier, following the technology in previous works [10, 11]. An array of metal wires are placed under a QCA cell layer, seen from the front view in Fig. 3(a). These wires that are aligned vertically can periodically generate electric fields to affect cells, seen from the top view in Fig. 3(b) where cells are marked as white squares. We will describe later that a metal pad below each cell is designed to precisely control its inter-dot barrier, thus to affect its state. Their physical implementation were also studied in molecular and magnetic QCA, respectively [12-15].

With the majority voters, inverters and four-phase clock, one can implement any complex circuit, which inevitably induces wire crossings. Researchers tried to minimize the number of wire crossings for simplifying QCA circuits [16-18]. In [19, 20], three non-wire crossing XOR gates were used to replace each wire crossing. This method will lead to non-wire crossing circuits, while resulting in a QCA system with a larger occupied area. The first coplanar wire crossing was proposed by using rotated cells [21]. It utilizes the second-nearest Coulomb interaction that severely decreases its performance in terms of fault tolerance and thermal characteristic [22]. Similar improvements to this structure were also studied [23]. A coplanar wire crossing consisting of normal cells was designed based on the opposite clock phases [24]. This scheme also employs the inferior second-nearest-neighbor interaction that will degenerate its thermal robustness. By using seven clocks, a coplanar wire crossing was implemented, which results in complex clock signal wires [25]. Although the multilayer wire crossing utilizes the nearest interaction, the physical implementation has yet to be reported to our best knowledge [26, 27].

In [28], a new concept was put forward to separate a system into two parts including a signal distribution network (SDN) and a combinational logic array (CLA). The SDN utilizes a double-service cell to transfer signals. Besides, the input signals are removed until the former inputs are processed.

*Corresponding author.

E-mail address: gjxie8005@hfut.edu.cn (G.J. Xie).

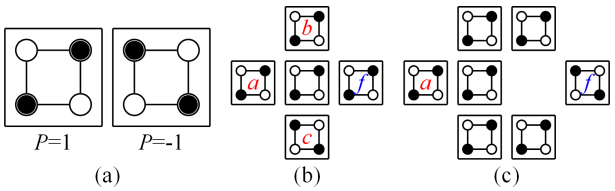

Fig. 1. QCA basics (**a**) QCA cells (**b**) Majority voter (**c**) Inverter.

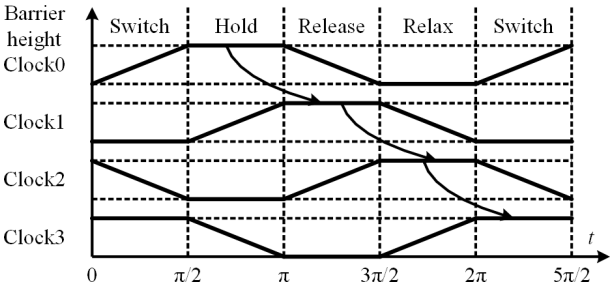

Fig. 2. QCA four-phase clock mechanism.

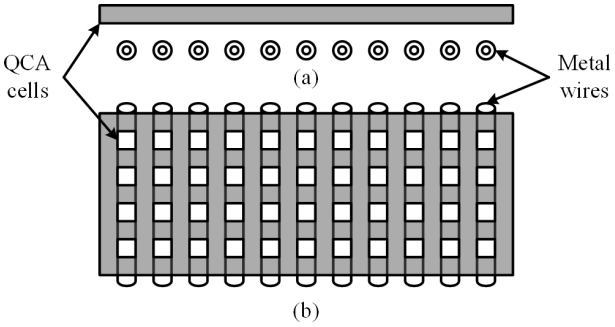

Fig. 3. Metal wires for providing electric field (**a**) Front view (**b**) Top view.

This method severely reduces the operational speed of a system. An optimized scheme was proposed in [29], of which the delay is a constant 1.25 clock cycles for an arbitrary number of inputs. This technique, however, is at the expense of the number of clock signals. Both of these schemes make use of the nearest neighbor Coulomb interaction to enhance the fault tolerance and thermal robustness of a wire crossing in a system. Obviously, one should consider four main aspects in the optimal design of QCA wire crossing including reducing the number of clock signals and clock delay, and enhancing the fault tolerance and thermal stability.

The main contributions of this paper are as follows: a new wire crossing is proposed by employing the four-phase clock mechanism and redundant normal cells. Its characteristics including thermal stability and fault tolerance against cell missing are verified. A new SDN composed of wire crossings is proposed and then applied to an XOR gate and full adder. Moreover, the standard logic functions with two- and three- variables are also implemented with the proposed SDN. In addition, the circuitries of metal wires for providing the electric fields to drive the cells for the proposed wire crossing and SDNs are also discussed. The functionalities and validity of designed circuits are demonstrated using QCADesigner.

This paper proceeds as follows: Section 2 presents the existing wire-crossings and the methods used for evaluating their performances in QCA. Section 3 proposes a new wire crossing. A new signal distribution network and its applications are presented in Section 4. The simulation results are presented in Section 5. Finally, Section 6 concludes this paper.

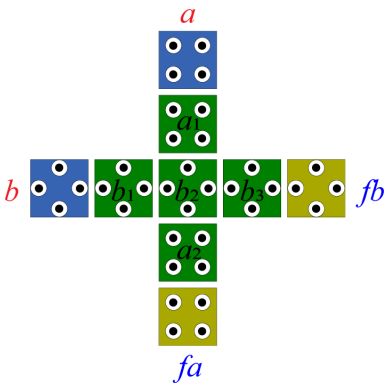

Fig. 4. Coplanar wire crossing using rotated cells in [21].

2. Background Materials

2.1. *Existing wire crossing*

In this subsection, the existing wire crossings are illustrated to find out their merits and disadvantages. Fig. 4 is the first coplanar wire crossing, which uses an array of rotated cells to transmit signals in horizontal wire, and normal cells in vertical wire. The polarizations of cells b_1, b_2 and b_3 do not affect the polarizations of cells a_1 and a_2 because of its symmetric structure, so that this layout can perform the function of a wire crossing [30]. This simple layout make the circuit design convenient, such as the design of full adders [31, 32]. As one can see that, however, the second-nearest Coulomb interaction between cells a_1 and a_2 is susceptible to thermal fluctuations, which will be detrimental to its applications [22].

The second type of wire crossings is based on the unique four-phase clock mechanism in QCA technique as aforementioned. Fig. 5(a) is a simplest one, which uses only clock0 and clock2 to exchange message in a central point [24]. This is achieved since two nonadjacent clock zones have opposite states. For example, if the cells in clock0 are locked in hold phase due to their enough high inter-dot barrier, the cells in clock2 are just in release phase relaying on their lowest barrier, meantime. There does not exist Coulomb interaction between these two types of cells because of their opposite polarization states, so that data will be respectively transmitted without any interference. Its layout is very simple for designing circuits in QCA in terms of cell count and circuit area, while its drawback is highly obvious to use the second-nearest interaction between cells a_1 and a_2 for transmitting signals likely the first wire crossing using rotated cells, resulting in unstable circuits in operating temperature and external noise.

Fig. 5(b) shows a thermostable coplanar wire crossing that uses only nearest Coulomb interaction between cells [28]. An updated one can be find in [29]. Its principles for transmitting signals are as follows. The signals *a* and *b* are synchronously poured into a circuit. The signal *a* is copied into successive circuits at first via a double-service cell, while signal *b* is delayed by one clock cycle as the figure shows. These inputs are then removed until the computation for the first set of inputs is completed. Obviously, this method will decrease the operation speed of a system.

Fig. 5(c) is an ingenious coplanar wire crossing that has a high thermal stability [25]. The cells b_1, b_2 and a_1 are controlled by a set of seven clock signals to realize correct function of a wire crossing. One can find

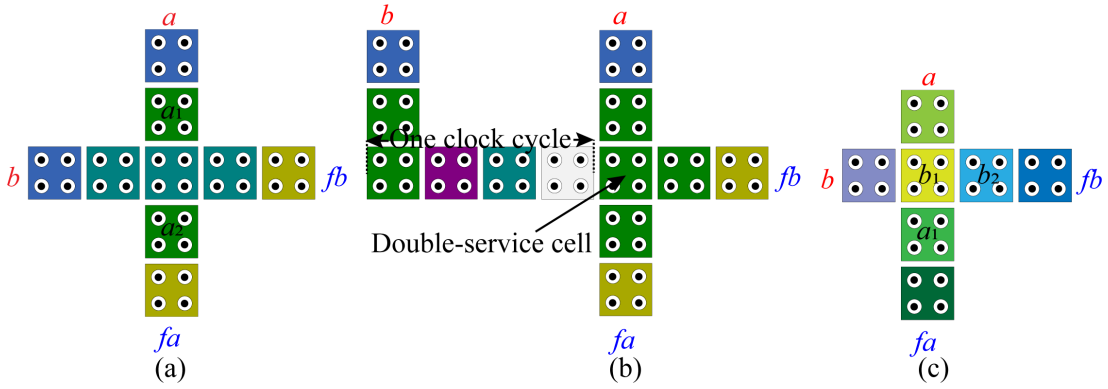

Fig. 5. Coplanar wire crossing using clock signals (**a**) Two signals in [24] (**b**) Four signals in [28] (**c**) Seven signals in [25].

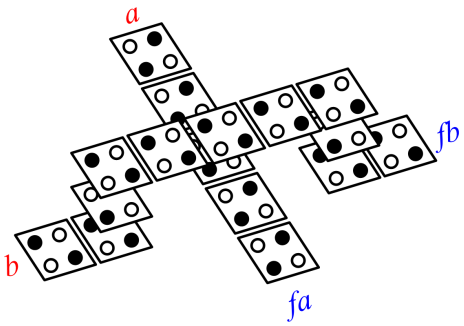

Fig. 6. Multilayer wire crossing in [27].

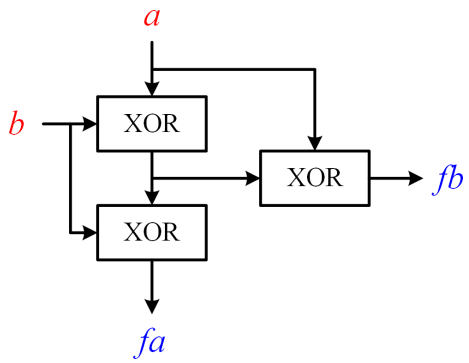

Fig. 7. Eliminating wire crossing using XOR gates in [20].

more details in relevant reference. It is clear that the intricate control signals make this scheme unfavorable.

Except coplanar circuits in QCA, the three dimensional structures were also proposed and verified theoretically [26]. Fig. 6 illustrates a three-layer wire crossing with a bridge structure using normal cells [27]. With a suitable vertical distance between two layers, this layout can realize the function of a wire crossing. It was already demonstrated that a circuit can save almost half area for a circuit with multilayer wire crossings compared with a coplanar one [26]. However, it is not easy from a fabrication standpoint and its physical implementation has yet to be reported to date.

Besides designing superior wire crossings, minimizing the number of crossings or eliminating them may be more feasible. Fig. 7 is a circuit unit consisting of three XOR gates, which can be used to replace each wire crossing in a circuit [20]. It is based on the axiom that $a \oplus b \oplus a = b$ and $a \oplus b \oplus b = a$, where a $\oplus$ denotes the XOR operation. With this unit, a circuit can be constructed by using normal cells and can use nearest Coulomb interaction for transmitting data, so that this unit will increase the thermostability and fault tolerance of a circuit. However, a XOR gate needs three majority gates in QCA, resulting in a circuit with a large area. This method may be not an optimal scheme for designing circuits with wire crossings.

2.2. *Fault tolerance*

Fault tolerance is referred to the ability of a system continually performing its intended function in the presence of faults. Due to the miniaturization of QCA cells and stringent accuracy requirements, perfect manufacturing is extremely difficult. The common faults in QCA include cell displacement / misalignment / rotation, cell / dot missing (or cell / dot undeposition), and extra cell / dot [33, 34]. These faults can be categorized as permanent errors that are mostly introduced by the fabrication imperfection. The basic methods for increasing the fault tolerance of a system for hardware defects is incorporating redundancies into the system [35]. As a basic logic element for QCA, thick wires were constructed by using redundant cells to improve fault tolerance [36]. The majority voter in QCA has been extensively investigated with regard to fault tolerance [37-40]. These designs employed extra cells to preserve their intended functions from one or more cell undeposition. Results indicate that these cells contribute to increasing the stability of the majority voter. The fault tolerance *FT* related to cell missing faults is defined as [41]

$$FT = \frac{N_u}{N_{m,u}} \tag{1}$$

where N_u and $N_{m,u}$ are respectively the number of correct and total patterns when u cells are undeposited in a system with m cells. Thus, *FT* gives the probability of generating the intended functions in the presence of cell missing faults. For example, if two cells are missing in a 6-cell system, the number of total patterns is $C_6^2 = 15$. If twelve cases can produce correct outputs, the fault tolerance *FT* of the system is *FT*=12/15=80%.

2.3. *Statistical models*

In [42], a statistical model was employed to examine the thermal effects on the behaviors of QCA devices. The expected value of an observable A for a system in thermodynamic equilibrium can be computed by

$$\langle A \rangle = \frac{1}{F} \sum_i A_i e^{-\frac{E(i)}{k_B T}} \tag{2}$$

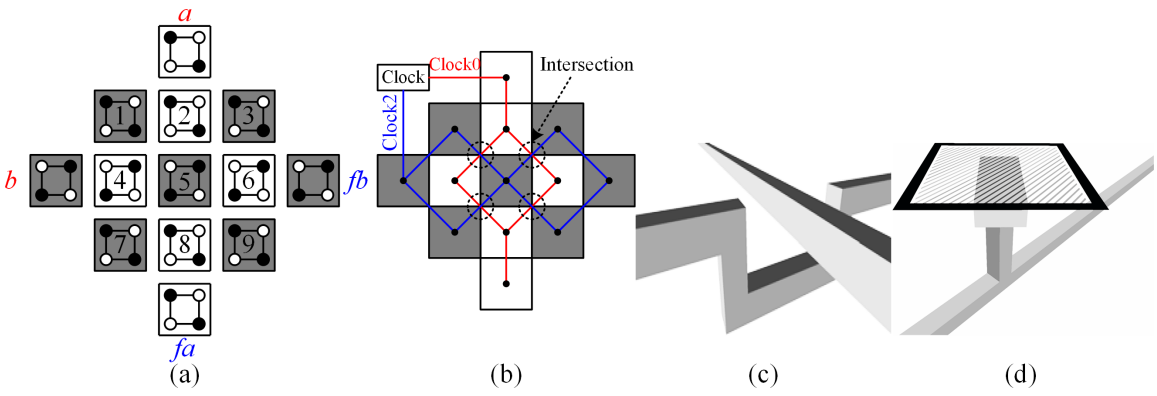

Fig. 8. Proposed wire crossing (**a**) Layout (**b**) Circuitry of metal wires (**c**) Metal wire crossing (d) Metal pad.

where F is the partition function of a system; $E(i)$ is the energy at the ith state; k_B is the Boltzmann constant; T is the temperature of the system in Kelvin. Thus, the expected polarization $<S_N>$ of the output cell N in a QCA system is given by equation (3).

$$\langle S_N \rangle = \frac{1}{F} \sum_{i=1, S_N=\pm 1}^{p} S_N e^{-\frac{E(i)_{S_N}}{k_B T}} = \frac{1}{F} \left(\sum_{i=1}^{p} e^{-\frac{E(i)_{S_N=1}}{k_B T}} - \sum_{i=1}^{p} e^{-\frac{E(i)_{S_N=-1}}{k_B T}} \right) \tag{3}$$

where p is the number of various states of a system. For a system with N cells, the polarization of each cell can be either 1 or -1. The polarizations of the input and output cells are fixed so that p is equal to 2^{N-2}. The canonical partition function F for a system with N cells is expressed

$$F = \sum_{i=1}^{q} e^{-\frac{E(i)}{k_B T}} \tag{4}$$

where q=2^N is the number of various states for N cells including the input and output cells. Because signals are transferred through the Coulomb interaction, the interaction $E_{i,j}^{m,n}$ between cells m and n is given by

$$E_{i,j}^{m,n} = \frac{e^2}{4\pi\varepsilon_0\varepsilon_r \left| r_i^m - r_j^n \right|} \tag{5}$$

where ε_0 and ε_r are respectively the vacuum permittivity and relative dielectric constant that is set to 12.9 as the default for GaAs/AlGaAs heterostructure based semiconductor implementations; $|r_i^m$-$r_i^n|$ is the distance between dot i in cell m and dot j in cell n. Therefore, the total energy between cells m and n for the aforementioned 4-dot cell model is given by

$$E^{m,n} = \sum_{i=1}^{4} \sum_{j=1}^{4} E_{i,j}^{m,n} \tag{6}$$

Finally, the system energy $E(i)$ at the ith state is the sum of the energy of pairwise cells.

3. New Wire Crossing

Using the opposite clocks and redundant cells, a knot type of coplanar wire crossing is proposed, as shown in Fig. 8(a), where the white/grey boxes denote the cells in clock0/clock2, respectively. For the wire crossing, 7 cells (cells b, fb, 1, 3, 5, 7 and 9 as labelled) in clock2 form a horizontal branch, while 6 cells (cells a, fa, 2, 4, 6, and 8 as labelled) in clock0 make up a vertical one. This wire crossing consists of 13 cells and covers an area of 0.01μm^2 for the default semiconductor QCA cells in QCADesigner 2.0.3 [43]. The computing results for verifying its fault tolerance and thermostability will be presented in Section 5.

We then design the circuitry of metal wires for generating the electric fields to drive cells in the proposed wire crossing. As shown in Fig. 8(b), the white/grey boxes denote the cells in clock0/clock2; the red/blue lines represent the metal wires under the cells in clock0/clock2, respectively. As in [10], to address the four intersections between the red and blue lines, two-layer metal wires are required to enable these crossings, as shown in Fig. 8(c). Additionally, a small metal pad indicated by a black dot under each cell, as shown in Fig. 8(d) is used to generate a necessary electric field that is controlled by the clock signal generator. As to The circuitry of metal wires for the proposed wire crossing is easily accessible by utilizing the fabrication methods in [10].

4. New Signal Distribution Network

4.1. XOR gate

Here, we employ a two-input XOR gate to investigate the proposed SDN that consists of the proposed wire crossings. The logic function for an XOR operation is $F = \bar{A}B + A\bar{B}$, whose diagram is shown in Fig. 9(a) using the design method in [28]. Fig. 9(b) shows the corresponding implementation in QCA by using a SDN and a CLA. As for the SDN for a two-variable function, two vertical QCA wires in clock0 form a basic framework. The signal A is propagated to the CLA through two wire crossings, while the signal B is transferred by two fanouts. This SDN requires 0.75 clock cycles; the XOR gate requires 1.25 clock cycles in total and an area of 0.1748μm^2.

The circuitry of metal wires for the SDN in the XOR gate is designed and shown in Fig. 9(c). The white/light grey/grey boxes denote the cells in clock0/clock1/clock2; the red/green/blue lines represent the metal wires under the cells in these clock zones, respectively. The metal wires in two vertical QCA wires in clock0 are connected to each other at the endpoints. The metal wires in clock2 are connected at the rightmost cells. It is worth noting that the metal wires in clock1 need bends and two-layer metal wires to access the vertical wire for avoiding the interference with the metal pads in clock0.

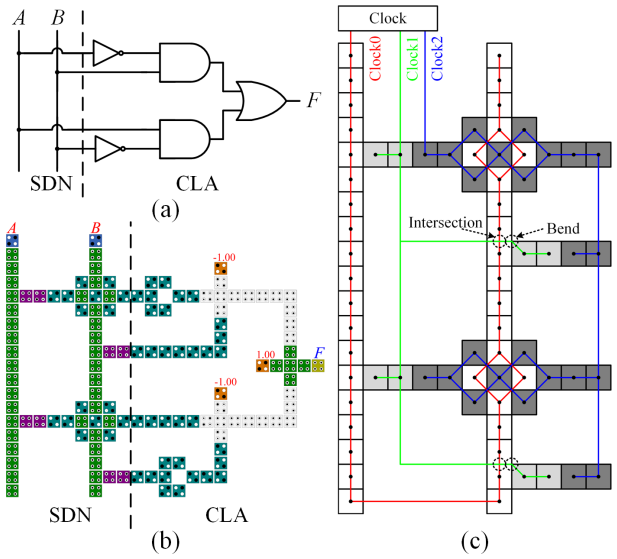

Fig. 9. An XOR gate (a) Diagram in [28] (b) Implementation in QCA using the proposed SDN (c) Circuitry of metal wires for the SDN in an XOR.

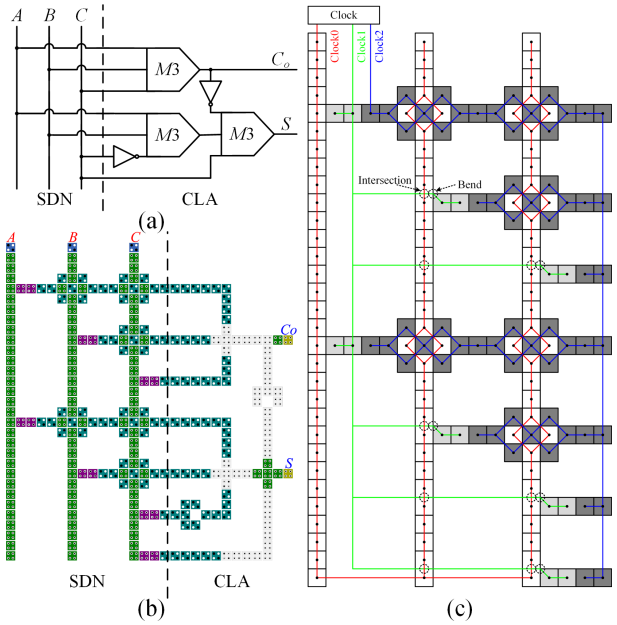

Fig. 10. A full adder (**a**) Diagram in [28] (**b**) Implementation in QCA using the proposed SDN (**c**) Circuitry of metal wires for the SDN in a full adder.

4.2. Full adder

In this subsection, a three-input full adder is designed to show the scalability of the proposed SDN. The carry out for a full adder is expressed as $C_o = AB + AC + BC = MV(A,B,C)$, which can be realized by a majority voter. The sum is denoted as $S = MV(\bar{C_o}, MV(A,B,\bar{C}), C)$ that is achieved by two voters and two inverters. Fig. 10(a) shows the diagram for a full adder that is separated into a SDN and a CLA. Fig. 10(b) illustrates its realization in QCA by using the proposed SDN composed of 6 wire crossings. This structure shows a high degree of regularity. Again, This SDN requires 0.75 clock cycles as the one in the XOR gate; the full adder takes 1.25 clock cycles in total and an area of 0.3472μm^2.

We design the circuitry of metal wires for the SDN in the adder, as shown in Fig. 10(c). The significances of these boxes and lines are the same

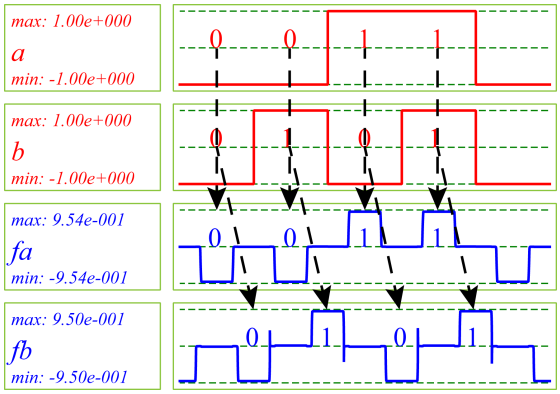

Fig. 11. Simulation results for the proposed wire crossing.

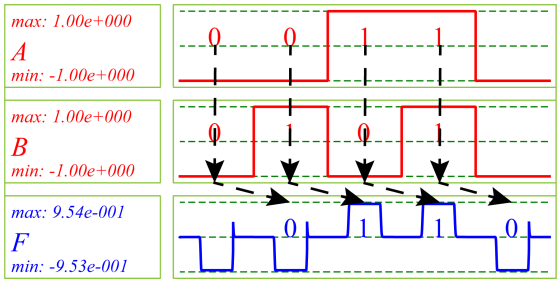

Fig. 12. Simulation results for an XOR gate using the proposed SDN.

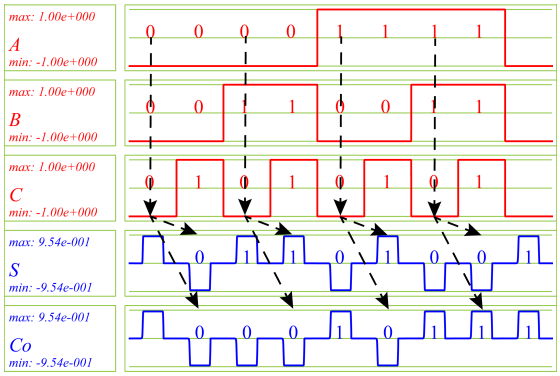

Fig. 13. Simulation results for a full adder using the proposed SDN.

as the SDN in the XOR gate. Similarly, the metal wires in three vertical wires are connected to each other at the bottom. The bends and two-layer metal wires in clock1 are also employed to avert the metal pads under the cells in clock0. The metal wires in clock2 are linked to each other at the rightmost cells. This design methodology for the circuitry of metal wires for a SDN in both the adder and the XOR gate indicates the scalability and practicality of the proposed SDN.

5. Results

In this section, we first show the simulation results for the designed circuits by using QCADesigner [43]. The computing results concerning the fault tolerance and thermal robustness for the proposed wire crossing will then be presented. The last subsection will show the comparisons of the new SDN with previous works.

5.1. Simulation results

Fig. 11 shows the simulation results for the proposed wire crossing. Signals *a* and *b* are delayed by 0.25 and 0.75 clock cycles, respectively.

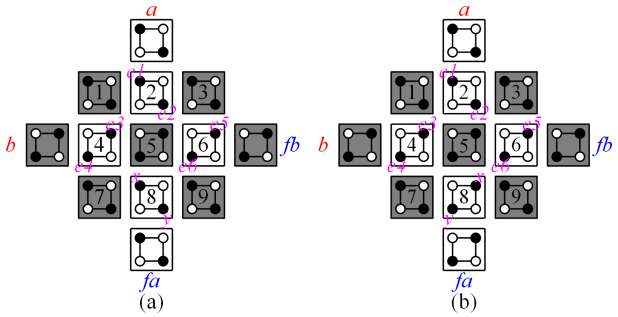

Fig. 14. Different electron arrangements for the proposed wire crossing (a) Case 1 (b) Case 2.

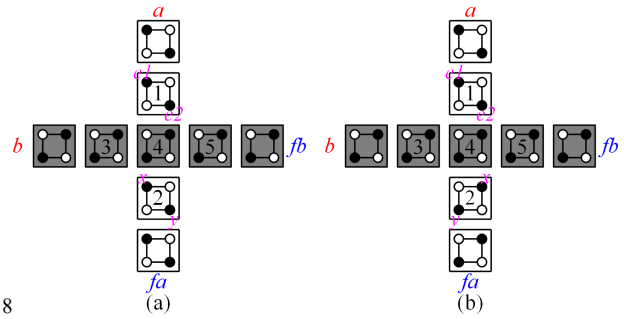

Fig. 15. Different electron arrangements for the wire crossing in [24] (a) Case 1 (b) Case 2.

Table 1

Electrostatic potential energy of cell8 for the proposed wire crossing.

Case 1	
Electron *x*	Electron *y*
$U_{e1}=A/r_{e1}\approx 0.58\times10^{-20}J$	$U_{e1}=A/r_{e1}\approx 0.38\times10^{-20}J$
$U_{e2}=A/r_{e2}\approx 0.81\times10^{-20}J$	$U_{e2}=A/r_{e2}\approx 0.58\times10^{-20}J$
$U_{e3}=A/r_{e3}\approx 1.15\times10^{-20}J$	$U_{e3}=A/r_{e3}\approx 0.54\times10^{-20}J$
$U_{e4}=A/r_{e4}\approx 1.15\times10^{-20}J$	$U_{e4}=A/r_{e4}\approx 0.54\times10^{-20}J$
$U_{e5}=A/r_{e5}\approx 0.54\times10^{-20}J$	$U_{e5}=A/r_{e5}\approx 0.54\times10^{-20}J$
$U_{e6}=A/r_{e6}\approx 1.15\times10^{-20}J$	$U_{e6}=A/r_{e6}\approx 1.15\times10^{-20}J$
$U_1\approx 9.07\times10^{-20}J$	
Case 2	
$U_2\approx 15.54\times10^{-20}J$	

Table 2

Electrostatic potential energy of cell2 for the wire crossing in [24].

Case 1	$U_1\approx 2.34\times10^{-20}J$
Case 2	$U_2\approx 2.50\times10^{-20}J$

This figure directly validates the functionalities of the wire crossing. Fig. 12 and Fig. 13 illustrate the simulation results for the proposed XOR gate and full adder, whose functions are validated. These waveforms perfectly correspond to their logic functions, respectively. Both of the designs are delayed by 1.25 clock cycles.

5.2. *Verification of the proposed wire crossing*

In this subsection, the physical verification is illustrated to validate the proposed wire crossing. It is necessary to calculate the electrostatic potential energy of the output cell, given the polarization of input cell. As we know from above analysis that the cells in clock0 and cells in clock2 do not affect to each other, so that one can consider them separately. Taking the cells in clock0 as an example as in Fig. 14, we label the electrons as *e1*~*e6*, *x* and *y*. It is clear that the output cell *fa* is positively polarized only by cell8, so that we can consider the polarization of cell8 as an indication of output cell. Fig. 14 shows two different electron arrangements, where the cell8 in case 1 has same polarization as input cell; cell8 in case 2 has an opposite polarization. The electrostatic energy of electrons is calculated by

$$U=\frac{k}{r} \tag{7}$$

where k is a constant and represented as $e^2/4\pi\varepsilon_0\varepsilon_r = 23.04\times10^{-29} = A$; r is the distance between two electrons. The total energy according to the energy of electrons x and y can be calculated, as listed in Table 1. The electrostatic energy difference between two cases is about 6.47×10^{-20}. It is clear that case 1 has lower energy than case 2, which means that the output cell in case 1 is more stable, generating correct results. Similarly, the cases for other cells can also be calculated, resulting in similar results.

Table 3

Coulomb interaction potential energy.

Configurations	Potential energy (J)	
	Same polarization	Opposite polarization
Nearest	3.6179×10^{-21}	3.9834×10^{-21}
Second-nearest	1.8101×10^{-21}	1.8210×10^{-21}
Diagonal	2.9502×10^{-21}	2.5911×10^{-21}

Fig. 15 gives two different electron arrangements for the wire crossing in [24]. Its electrostatic energy is also calculated with same method, as listed in Table 3. The results also show that the case 1 is a correct electron arrangement, generating correct output. The energy difference between these two cases is 0.16×10^{-20}.

If the electrostatic energy difference between correct and erroneous arrangements is larger, the probability of erroneous output is smaller, and the structure is more stable. To compare the proposed wire crossing and the one in [24], the absolute value of the electrostatic energy differences is not all-inclusive. Here, we look at the relative differences for two crossings. The relative difference indicates the degree of difficulty of changing the stable electron arrangement to an unstable one. The bigger the relative difference is, the more difficult it is. The relative difference of the energy for two cases in Fig. 14 is $(15.54\times10^{-20}-9.07\times10^{-20})/(9.07\times10^{-20})=71.33\%$, while it is just $(2.50\times10^{-20}-2.34\times10^{-20})/(2.34\times10^{-20})=6.84\%$ for the cases in Fig. 15, so that the proposed wire crossing is more stable than the one in [24].

5.3. *Fault tolerance*

As depicted in Fig. 8, we assume that four input/output cells are faultless and that one or more cells labelled as 1-9 will be undeposited. Table 4 lists the number of correct outputs for *fa* and *fb* against various number of missing cells. In this table, “Patterns” means the number of combinatorial defect patterns when n (0~9) cells are missing. For example, if 3 cells are missing, the number of possible defects is $C_9^3 = 84$, among which 35 and

Table 4

Number of correct outputs against various number of missing cells.

Number of missing cells	0	1	2	3	4	5	6	7	8	9
Patterns	1	9	36	84	126	126	84	36	9	1
Correct *fa*	1	7	21	35	35	21	7	1	0	0
Correct *fb*	1	9	36	80	106	85	40	10	1	0

Table 5

Number of correct outputs against various number of missing cells when an assigned cell is missing.

Number of missing cells	0	1	2	3	4	5	6	7	8
Patterns / Fixed missing cell	1	8	28	56	70	56	28	8	1
Cell 1	1/1	6/8	15/26	20/45	15/45	6/26	1/8	0/1	0/0
Cell 2	0/1	0/8	0/28	0/52	0/54	0/31	0/9	0/1	0/0
Cell 3	1/1	6/8	15/26	20/45	15/45	6/26	1/8	0/1	0/0
Cell 4	1/1	6/8	15/28	20/52	15/54	6/31	1/9	0/1	0/0
Cell 5	1/1	6/8	15/24	20/36	15/29	6/12	1/2	0/0	0/0
Cell 6	1/1	6/8	15/28	20/52	15/54	6/31	1/9	0/1	0/0
Cell 7	1/1	6/8	15/26	20/45	15/45	6/26	1/8	0/1	0/0
Cell 8	0/1	0/8	0/28	0/52	0/54	0/31	0/9	0/1	0/0
Cell 9	1/1	6/8	15/26	20/45	15/45	6/26	1/8	0/1	0/0

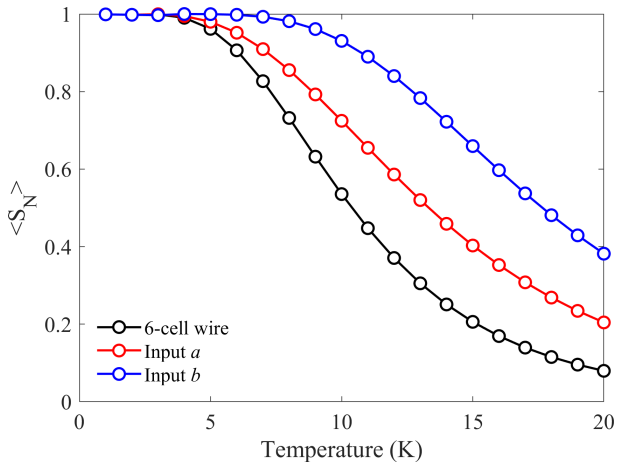

Fig. 16. Thermal characteristics for a 6-cell wire and two signal transmission branches in the proposed wire crossing.

Table 6

Comparisons for various SDNs.

SDNs	Number of clock signals	Delay
[28]	4	(2*n*-1)/2
[29]	6	1.25
Proposed	4	0.75

80 combinations can produce correct outputs for *fa* and *fb*, respectively. According to Table 4, the results lead to the following observations: the fault tolerance of branch *fb* is higher than that of branch *fa*; the fault tolerance of two branches decreases with an increasing number of missing cells; the differences of the fault tolerance between two branches are evident; the proposed wire crossing has a fault-tolerant structure.

To find out which cell is critical to the fault tolerance of the proposed wire crossing, a complementary experiment is performed. As listed in Table 5, we detect the number of correct outputs against various number of missing cells when a fixed cell (Cell1 ~ Cell9) is missing. For example, if cell3 is defined to be undeposited and other2 cells among the remaining 8 cells will be undeposited, there are 28 combinations to produce 15 correct outputs for *fa* and 26 correct results for *fb*, respectively.

According to Table 5, one can easily observe that the loss of either cell2 or cell8 will definitely make an erroneous output for *fa* at any number of missing cells. The cases of other cell missing share the same results for *fa*. As for *fb*, the loss of cell1, cell3, cell7 and cell9 can produce the same results, while the loss of cell2, cell4, cell6 and cell8 will generate a large number of correct outputs. This can also be interpreted as due to the symmetry of the proposed wire crossing. Further, the undeposition of cell5 produces less correct outputs because of its particular position in the layout of the proposed wire crossing.

5.4. Thermal stability

In the following thermal stability evaluation, the distance between two nearest dots is defined as 10 nm and the center-to-center spacing between two nearest cells is 20 nm. Further, the interaction between two cells dramatically decays with the increasing distance between them, thus 2-cell distance for the radius of effect is usually sufficient for a simulation [44]. These assumptions can generate three configurations including the nearest, second-nearest, and diagonal structures. Three types of Coulomb

Table 7

The performance figures for the two- and three-variable standard functions.

No.	Functions	Area (μm²)	Number of cells	Delay	Cost
1	$F = AB = M(A,B,0)$	0.0660	50	1.00	2.00
2	$F = AB + \overline{A}\overline{B} = M\left(M(A,B,0), M(\overline{A},\overline{B},0),1\right)$	0.1380	104	1.25	7.50
3	$F = AB + AC + BC = M(A,B,C)$	0.1120	93	1.00	4.00
4	$F = ABC = M\left(M(A,B,0),C,0\right)$	0.1500	112	1.25	6.25
5	$F = AB + BC = M\left(M(A,1,C),B,0\right)$	0.1500	112	1.25	7.50
6	$F = AB + \overline{B}C = M\left(M(A,B,0), M(0,\overline{B},C),1\right)$	0.1700	129	1.25	8.75
7	$F = ABC + A\overline{B}\overline{C} = M\left(A, M(0,B,C), \overline{M(1,B,C)}\right)$	0.1800	142	1.25	8.75
8	$F = ABC + \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} = M\left(\overline{M(A,B,C)}, M(A,B,\overline{C}), C\right)$	0.2600	197	1.25	11.25
9	$F = AB + \overline{A}\overline{B}C = M\left(M(A,B,0), \overline{M(A,B,1)}, M(A,1,C)\right)$	0.2464	192	1.25	12.50
10	$F = ABC + \overline{A}\overline{B}\overline{C} = M\left(M(A,B,0), \overline{M(1,B,C)}, M(\overline{A},1,C)\right)$	0.2240	174	1.25	11.25
11	$F = AB + BC + \overline{A}\overline{B}\overline{C} = M\left(M(\overline{A},B,1), \overline{M(1,B,C)}, M(A,B,C)\right)$	0.2800	204	1.25	12.50
12	$F = ABC + \overline{A}B\overline{C} + A\overline{B}\overline{C} = M\left(M(A,0,C), \overline{M(A,B,C)}, M(A,B,\overline{C})\right)$	0.3224	237	1.25	13.75

interaction potential energy for these configurations are computed as listed in Table 3. With these values, the system energy $E(i)$ at the ith state can be easily computed; the canonical partition function F and the expected polarization $<S_N>$ of the output cell N can then be calculated.

Fig. 16 shows the thermal characteristics of two branches in the proposed wire crossing. The branches *a* and *b* are composed of 6 and 7 cells, respectively. The thermal robustness for a QCA system will decline with the increase in the number of cells [42], thus, a 6-cell wire is chosen as a reference object for evaluating the thermal stability of the wire crossing. We can see that the expected polarizations of the cell *fa* and *fb* are always larger than that of 6-cell wire. It means that although the signals in the branches *a* and *b* are mainly transferred by the second-nearest and diagonal Coulomb interaction, it is clear that they show excellent thermostability compared with the 6-cell wire. It validates that the proposed wire crossing solves the problem that the conventional wire crossing using the second-nearest interaction is susceptible to thermal effects.

5.5. *Performances of new signal distribution network*

The proposed SDN is compared with the designs in [28, 29] with respect to the number of clock signals and their latency, as listed in Table 6. Although the SDN in [28] employs 4 clock signals, the delay of that scheme linearly increases with the number of inputs *n*. The latency of an optimized design in [29] keeps constant 1.25 clock cycles, whilst it requires 6 clock signals that make the circuitry of metal wires complex. The proposed wire crossing implements an SDN with only 4 clock signals and holds constant 0.75 clock cycles. It can be concluded that the proposed SDN outperforms its counterparts in the considered criteria.

Table 7 lists the performances of simplified layouts using the proposed SDN for the two- and three-variable standard functions in [45]. These circuits utilize fanouts to link input signals and logic components for minimizing the number of wire crossings. The functions 1 and 3 have one stage to compute; each stage holds a 0.25 clock cycle delay. Consequently, both of them get 1.00 cycle delay. Others have two computation stages, thus these circuits require 1.25 clock cycles to finish each computation. We can easily find that a linear relationship between the occupied area and number of cells for these functions with coplanar layouts using the proposed SDN appears. In addition, the cost function in QCA in [46] is used to evaluate these circuits as in the last column. The cost of a system is expressed as $\text{cost}=(M^x+I+C^y)\times L^z$, where M, I, C and L are the number of majority gates, inverters, wire crossings, and clock delay of a circuit; x, y, and z are the exponential weightings for these parameters, respectively. In this paper, we assume that $x=y=z=1$ for uniformly evaluating these components. It is clear that there is a linear relationship between the costs of the designed circuits using the proposed wire crossings for these standard functions and their cell count.

6. Conclusions

Quantum-dot cellular automata (QCA) are a promising design paradigm for solving the deficiencies of conventional circuits. The wire crossing in QCA has attracted many researches due to its important properties. In this paper, a robust wire crossing is proposed by using opposite clock phases and redundant cells. Its thermostability and fault tolerance against cell missing are verified. Simulation results show that this structure has a high thermal robustness. In addition, the results indicate that cell 2 and cell 8 in the proposed wire crossing are critical, whose undepositions are likely to cause the malfunction of the wire crossing. Therefore, it is important to enhance the robustness of these cells in the manufacturing process.

A bit-scalable signal distribution network (SDN) is then designed by using the proposed wire crossing. This SDN only employs 4 clock signals and holds a 0.75 clock cycle delay. A two-input XOR gate and a three-input full adder are investigated to show that the proposed design approach is scalable to circuits with an arbitrary number of inputs. The circuitries of metal wires for generating the electric fields to drive the QCA cells are proposed; their regularity shows the scalability of the proposed SDN.

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