Design and Reliability Analysis of Multiple Valued Logic Gates using Carbon Nanotube FETs

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***Abstract*—With emerging nanometric technologies, multiple valued logic (MVL) circuits have attracted significant attention due to advantages in information density and operating speed. In this paper, a pseudo complementary MVL design is initially proposed for implementations using carbon nanotube field effect transistors (CNTFETs). This design utilizes no resistors in its operation. To account for the properties and fabrication non-idealities of CNTFETs, a transistor-level reliability analysis is proposed to accurately estimate the error rates of MVL gates. This approach considers gate structures and their operation, so it yields a more realistic framework than a logic-level analysis of reliability. To achieve scalability, stochastic computational models are developed to accurately and efficiently analyze MVL gates; the extension of these models to circuits is briefly discussed.**

Keywords - multiple valued logic (MVL); carbon nanotube field effect transistors (CNTFETs); reliability; stochastic computational models (SCMs)

I. INTRODUCTION

The scaling of CMOS technology has not only brought significant improvements in integrated circuits, but also raised reliability concerns for the design and test of digital circuits. As CMOS approaches physical and technological limits, new devices have been proposed to implement nanoscale architectures, such as the multiple-valued logic (MVL) operation with base higher than two. MVL allows for more than two levels of logic; depending on the number of levels, ternary (base 3) and quaternary (base 4) logic have been advocated for different applications [1]. MVL enjoys many advantages over its binary counterpart; for example, each wire can transmit more information than binary, so the number of connections in a chip can be reduced, thus decreasing circuit complexity. However, MVL circuits are subject to issues such as low noise margins.

Recently, carbon nanotube field-effect transistors (CNTFETs) have been extensively studied as a potential alternative to the silicon-based MOSFETs for implementing MVL circuits [2, 3]. Resistor-loaded designs utilize fewer transistors to implement MVL gates, but the chip-implemented resistors and the large static power consumption limit their integration and applications [2]. Complementary designs can be fully integrated and consume little static power but using more transistors [3]. As a trade-off between static power consumption and area cost (i.e., the number of transistors), a pseudo-complementary CNTFET-based MVL design is proposed in this paper.

Similar to nanoscale CMOS circuits, CNTFET-based MVL circuits are affected by manufacturing variations and noise, so their operation is probabilistic and subject to errors. Therefore, the analysis of reliability of MVL circuits is of significant concern. A number of approaches have been proposed for the reliability evaluation of binary circuits, including both gate-level [4-8] and transistor-level [9-11] approaches. However, to the best knowledge of the authors no approach has been proposed for the reliability analysis of MVL gates. In particular, the structure and topologies of MVL gates need to be taken into consideration in an accurate evaluation approach. Hence, a transistor-level analysis is highly desirable because it can provide a better assessment of the gate structure as well as the error susceptibility of a particular implementation.

For this process to be viable, it is important to efficiently evaluate the reliability though a simple, yet efficient method to provide insight on reliability as well as its enhancements. Therefore, one of the goals of this paper is to efficiently estimate reliability for further developing enhancement techniques. In particular, this paper makes the following contributions:

(1) A pseudo complementary CNTFET-based MVL design is proposed as an alternative to the previously proposed resistor-loaded and complementary CNTFET MVL (Section III).

(2) A transistor-level reliability analysis to accurately estimate the probabilistic behaviour of the newly proposed MVL design is pursued (Section IV).

(3) Stochastic computational models (SCMs) for MVL are developed for evaluating the reliability of gates; the applicability of these models to circuits is briefly treated through an illustrative example (Section V).

The rest of this paper starts with a review on CNTFETs and a probabilistic analysis of their error characteristics in Section II. Section III presents the pseudo complementary CNTFET MVL design and its HSPICE simulation. Section IV and V discuss the transistor-level analysis and SCMs for reliability, followed by conclusions in Section VI.

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II. REVIEW

In this section, a brief overview of the CNTFET (inclusive of fault models) and the asymmetrically-correlated carbon nanotube (ACCNT) technique is provided, with a probabilistic analysis of open and short defects.

A. The CNTFET

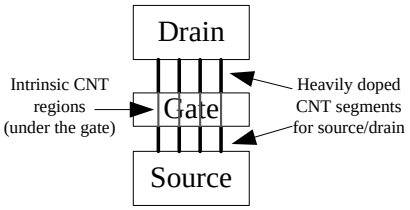


Fig. 1. CNTFET structure with four CNTs in the channel.

The features of high mobility of charge carriers and the reduction in subthreshold slope in gate geometry make the CNTFET a promising candidate as a post-CMOS device [12, 13]. Fig. 1 illustrates the device structure of a CNTFET with four ideal single-wall semiconductor CNTs in the channel [3]. Current CNT fabrication processes are not ideal; in addition to the traditional CMOS fabrication defects (such as faulty open and bridge contacts), the CNTFET manufacturing process suffers from new variation challenges, such as in CNT diameters and bandgap. Therefore, many sources of uncertainty and defects affect the reliable operation of CNTFET devices.

A metallic CNT is one of the most dominant defects; a CNT can be either metallic (m-CNT) or semiconducting (s-CNT) depending on its chirality. Currently, there is no known technique available to grow 100% s-CNTs. The conductivity of m-CNTs cannot be controlled by the gate due to the zero or near-zero bandgap and therefore the removal of m-CNTs or m-CNT tolerance is required.

B. The ACCNT technique

Since techniques such as the selective chemical etching [14] are not perfect and cannot guarantee a robust circuit fabrication, a VLSI-compatible methodology referred to as asymmetrically-correlated carbon nanotubes (ACCNTs) has been proposed for reliable circuit design [15].

As a metallic-CNT tolerant technique, ACCNT can tolerate short defects (as caused by metallic CNTs) by utilizing uncorrelated stacks of CNTFETs in series. Furthermore, the ACCNT technique uses correlated branches of parallel CNTFETs to increase the device drive strength without degrading the failure rate [15]. ACCNT requires a conventional CNTFET process, and does not conflict with other metallic removal or breakdown solutions. Although this technique incurs a large area overhead, it has been shown to be efficient in tolerating metallic-CNTs at wafer level in the manufacturing process flow. Therefore, the ACCNT technique can effectively enhance yield.

C. Open and short defect probabilities for ACCNT

An accurate mathematical model that considers the density variation in ACCNTs has been proposed in [16]. Although variations may affect the chirality values of the CNTs, the discussion in this paper is focused on short and open defects.

Let the CNT placement be totally random (i.e., at a probability of 0.5 at any given site), the average density of the CNTs be D CNTs/μm, the window size (or CNTFET width) be W μm; then the average number of CNTs in each CNTFET is given by

$$\bar{N}_{CNT} = WD. \quad (1)$$

For a placement probability of 0.5, $2\bar{N}_{CNT}$ CNTs need to be placed in the channel for an expected value given by (1). The probability of an open defect is then given by:

$$P_{O(CNFET)} = 0.5^{2\bar{N}_{CNT}}. \quad (2)$$

A CNTFET is defective (**s**hort) when at least one metallic CNT is present; so by considering the CNT density variation,

$$\bar{P}_{S(CNFET)} = \sum_{k=1}^{2\bar{N}_{CNT}} \frac{(2\bar{N}_{CNT})!}{k!(2\bar{N}_{CNT}-k)!} 0.5^{2\bar{N}_{CNT}}[1 - (1-P_M)^k], \quad (3)$$

where P_M denotes the probability of a CNT to be metalic.

For uncorrelated CNTFETs in series of N_{STACK} stacks, the probability that an ACCNT-based transistor has short defects, is given by

$$P_{S(ACCNT)} = \bar{P}_S^{N_{STACK}}. \quad (4)$$

The probability that an ACCNT-based transistor has open defects, is

$$P_{O(ACCNT)} = 1 - (1-P_O)^{N_{STACK}}. \quad (5)$$

In the general case, a metallic CNT has a probability of around $\frac{1}{3}$ [15, 16], i.e., $P_M = \frac{1}{3}$. Assume $\bar{N}_{CNT} = 4$ and $N_{STACK} = 14$, the following defect probabilities are found:

$P_{S(ACCNT)}$=0.046 and $P_{O(ACCNT)}$=0.053.

For simplicity and without loss of generality, an independent defect rate of $P_{S(ACCNT)} = P_{O(ACCNT)}$ =0.05 is considered in the following calculations.

III. PSEUDO COMPLEMENTARY CNTFET BASED MVLS

Ternary logic gates can be designed using CNTFETs [2, 3]. In [2], a resistance-loaded design is realized for ternary logic as a basis to further use CNTFETs. This approach however suffers from the disadvantage of large area overhead (due to a large resistance) and power dissipation. However, its operational principles are valuable, which establishes some important features for CNTFET-based design. A pseudo complementary implementation of MVL based on CNTFETs is proposed next. The proposed design replaces the resistors used in [2] with p-type CNTFETs (with the gate connected to ground), while threshold voltage operation is accomplished by

adjusting the chirality and the number of CNTs in each CNTFET. This approach (referred to as *pseudo complementary*) exploits the similarities in threshold voltage control in the p- and n-types while ensuring a correct MVL design for both ternary and quaternary logic gates.

A. *Pseudo complementary ternary logic*

Table 1. Truth table for three ternary inverters

Input	STI	NTI	PTI
0	2	2	2
1	1	0	2
2	0	0	0

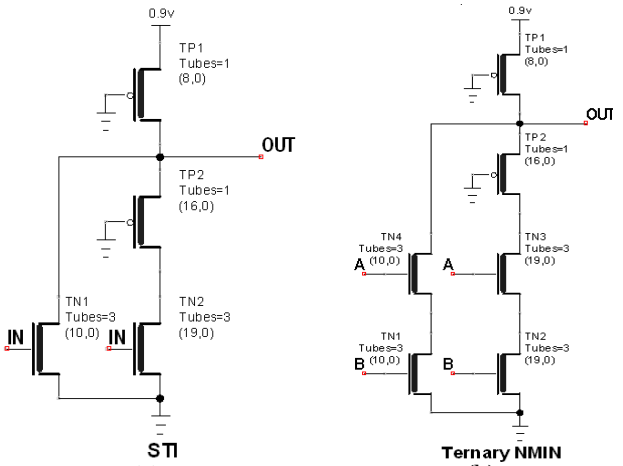


Fig. 2 (a) A pseudo complementary STI; (b) A pseudo complementary ternary NMIN operator.

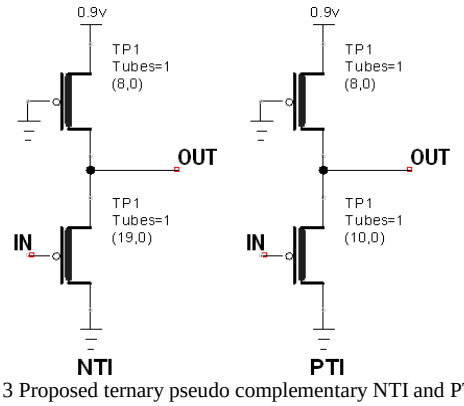


Fig. 3 Proposed ternary pseudo complementary NTI and PTI.

Consider first ternary operation. There are three types of ternary inverters (Table 1): standard ternary inverter (STI), negative ternary inverter (NTI), and positive ternary inverter (PTI). Fig. 2(a) shows the proposed pseudo complementary STI using CNTFETs. It consists of two n-type CNTFETs and two p-type CNTFETs. One of the CNTFETs (T_{P1}) has a chirality of (8, 0); it is used as the pull-up network, while the other three CNTFETs are used as the pull-down network. The chiralities of T_{N1} and T_{N2} are (10, 0) and (19, 0), and the corresponding threshold voltages are 0.559 V and 0.293 V respectively. Consider an input voltage V_{in}. For small values of V_{in}, both T_{N1} and T_{N2} are off. Hence, the output node (OUT) is held at V_{DD}. As V_{in} increases beyond V_{th2} (0.293 V), T_{N2} is turned on. The output voltage is determined by the resistance ratio of T_{P1}, T_{P2} and T_{N2}; therefore it is held approximately at $V_{DD}/2$ until V_{in} reaches V_{th1} (0.559 V). Once V_{in} exceeds V_{th1}, T_{N1} is turned on and the output is pulled down to nearly zero. The voltage at the output node is plotted in Fig. 4 (obtained by HSPICE simulation). Similarly, Fig. 3 shows the proposed pseudo complementary NTI and PTI implementations. The HSPICE simulation results in Figs. 4 and 5 show the correct operations of the proposed designs.

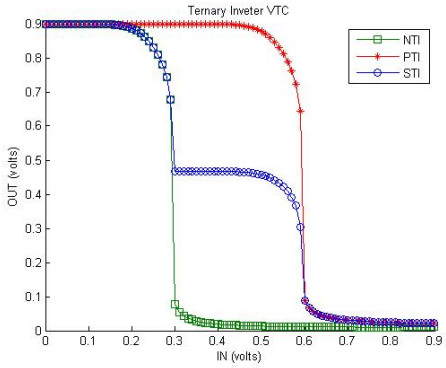


Fig. 4 Voltage transfer diagram for the ternary inverters (STI, PTI and NTI).

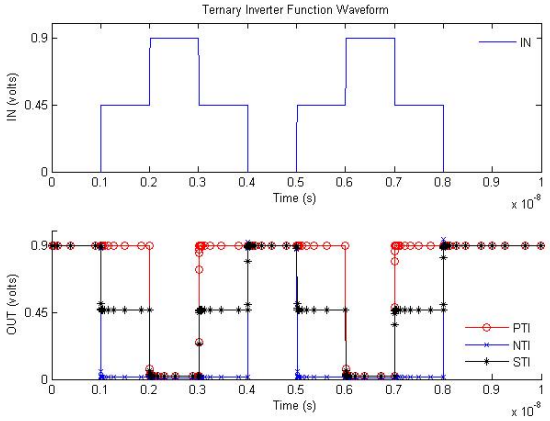


Fig. 5 Transient simulation results of the ternary inverters.

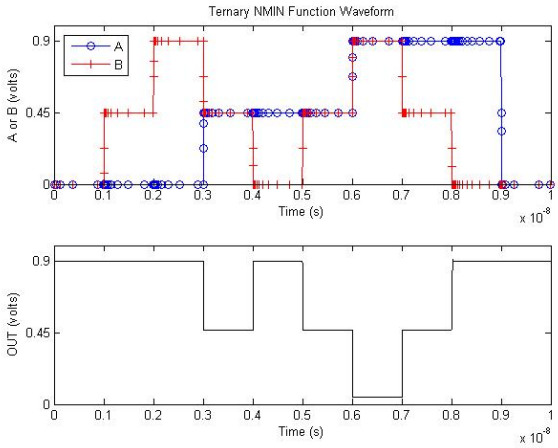


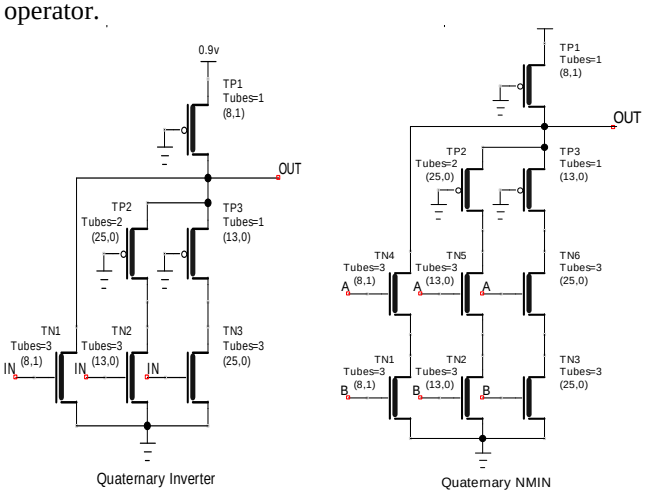
Fig. 6 Transient simulation results of ternary NMIN operator.

A pseudo complementary ternary NMIN is designed next (Fig. 2(b)). This gate consists of six CNTFETs, with four different chiralities. In this gate, similar to the ternary STI in

Fig. 2(a), the CNTFETs with chiralities (10, 0) and (19, 0) have threshold voltages of 0.559 V and 0.293 V, respectively. HSPICE simulation (shown in Fig. 6) confirms the correctness of the proposed design.

B. Pseudo complementary quaternary logic

Similarly, pseudo complementary quaternary logic gates are designed in this section. Fig. 7(a) shows a pseudo complementary CNTFET quaternary inverter, while Fig. 7(b) shows a pseudo complementary CNTFET quaternary NMIN operator.



(a) (b)

Fig. 7 (a) A pseudo complementary quaternary inverter; (b) A pseudo complementary quaternary NMIN operator.

The inverter consists of three n-type CNTFETs and three p-type CNTFETs, each with a different chirality; the NMIN operator consists of six n-type CNTFETs and three p-type CNTFETs. Each of the p-type CNTFETs has a distinct chirality, while the six n-type CNTFETs have three chiralities. Fig. 8 shows the voltage transfer diagram of the quaternary inverter. Compared to the simulation results of the ternary inverter (Fig. 4), Fig. 8 shows the reduced noise margin for the quaternary logic. Fig. 9 shows the transient simulation results (simulated by HSPICE).

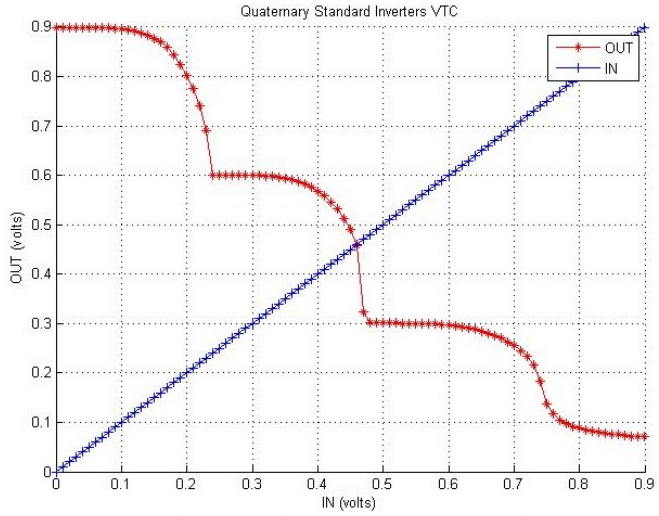


Fig. 8 Voltage transfer diagram for the quaternary inverter of Fig. 7(a).

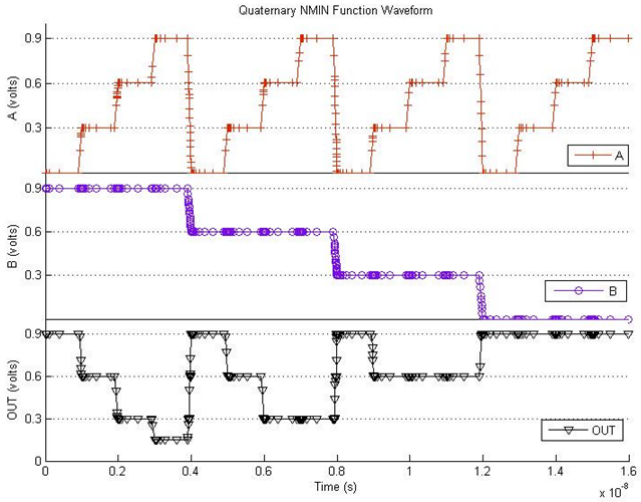


Fig. 9 Transient simulation results of quaternary inverter and NMIN operator.

IV. RELIABILITY ANALYSIS OF MVL GATES

Most previous methods for reliability evaluation are based on the simple assumption that every gate fails with a given probability. This assumption is common due to its simplicity in a mathematical model and efficiency in a gate-level evaluation. However, this assumption is not fully applicable when gate complexity is taken into account; for example, in a binary CMOS circuit, an inverter consists of one PMOS transistor and one NMOS transistor, while an AND gate usually consist of three PMOS transistors and three NMOS transistors. Due to the non-idealities in fabrication and operational conditions (such as induced noise), it is evident that an AND gate has a larger probability to fail compared to an inverter.

This section proposes a transistor level analysis to estimate the probabilistic behavior of MVL gates; with no loss of generality, the pseudo complementary CNTFET logic gates proposed in the previous section are utilized to illustrate the proposed method. However, the method is sufficiently flexible that it can easily be extended and generalized to other MVLs.

A. Ternary logic

As discussed previously, open and short defects can be modeled on a probabilistic basis. Consider the function of the ternary inverter in Fig. 2(a). When the input voltage is lower than 0.293 V (logic 0), both T_{N1} and T_{N2} are expected to be turned off. However, on a probabilistic basis by taking into account the error probability of each CNTFET, the correct response of the inverter (by considering all CNTFETs in this gate) is given by a probability of only $(1 - \mathrm{Po})(1 - \mathrm{Ps})^2$. In this paper, the open and short defects are considered to occur independently, although they may be correlated due to the manufacturing process. To consider other defect scenarios, for example, there is a probability of $\mathrm{Po}(1 - \mathrm{Ps})^2$ for T_{P1} to be open, T_{N1} to be operating correctly or open, and T_{N2} to be operating correctly or open. The output can also be floating and therefore, its current value is determined by the previous value. The detailed analysis of all scenarios and the corresponding probabilities are given in Table 2.

Table 2. All possible scenarios for an STI when Input<0.3V (Logic 0) ("floating" indicates both pull-up and pull-down networks are off. N: normal; S: short defect; O: open defect; X: don't care; '/' means 'or'.)

Scenario	Probability	OUT logic
TP1:N/S;TP2:X; TN1:N/O;TN2:N/O.	$(1-Po)(1-Ps)^2$	2
TP1:O;TP2:X; TN1:N/O;TN2:N/O.	$Po(1-Ps)^2$	Floating
TP1:X;TP2:X; TN1: S; TN2: X.	Ps	0
TP1:O;TP2:O; TN1: N/O; TN2: S.	$Po^2(1-Ps)Ps$	Floating
TP1:S/N;TP2:O; TN1: N/O; TN2: S.	$(1-Po)Po(1-Ps)Ps$	2
TP1:N/S;TP2:N/S; TN1: N/O; TN2: S.	$(1-Po)^2Po(1-Ps)$	1
TP1:O;TP2:N/S; TN1: N/O; TN2: S.	$Po(1-Po)(1-Ps)Ps$	0

Based on Table 2, the output probability distributions for an input at logic 0 can then be calculated (as shown in Table 3).

Table 3. Output probabilities of an STI when Input<0.3V (Logic 0)

Output	Probability
0	$\text{Prob}_{0\|0} = Ps + Po(1-Po)(1-Ps)Ps$
1	$\text{Prob}_{1\|0} = (1-Po)^2Po(1-Ps)$
2	$\text{Prob}_{2\|0} = (1-Po)(1-Ps)^2 + (1-Po)Po(1-Ps)Ps$
Floating	$\text{Prob}_{\text{floating}\|0} = Po(1-Ps)^2 + Po^2(1-Ps)Ps$

Table 4. Output probabilities of an STI when 0.3V<Input<0.6V (Logic 1)

Output	Probability
0	$\text{Prob}_{0\|1} = \text{Ps}+\text{Po}(1-\text{Ps})(1-\text{Po})^2$
1	$\text{Prob}_{1\|1} = (1-\text{Po})^2(1-\text{Ps})^2$
2	$\text{Prob}_{2\|1} = (1-\text{Po})(1-(1-\text{Po})^2)(1-\text{Ps})$
Floating	$\text{Prob}_{\text{floating}\|1} = \text{Po}(1-\text{Ps})(1-(1-\text{Po})^2)$

Table 5. Output probabilities of an STI when Input>0.6V (Logic 2)

Output	Probability
0	$\text{Prob}_{0\|2} = 1-\text{Po}+\text{Po}^2(1-\text{Po})^2$
1	$\text{Prob}_{1\|2} = \text{Po}(1-\text{Po})^3$
2	$\text{Prob}_{2\|2} = (1-\text{Po})\text{Po}(1-(1-\text{Po})^2)$
Floating	$\text{Prob}_{\text{floating}\|2} = \text{Po}^2(1-(1-\text{Po})^2)$

Similarly, the output probabilities of a ternary inverter when the input is at logic 1 and 2 can be found in Tables 4 and 5 respectively.

By combining for an input the values of the output probabilities (given in Table 3, Table 4 and Table 5), a single comprehensive table can be generated. This comprehensive table describes the probabilistic mapping from the primary inputs to the primary output of a gate.

So for a ternary inverter, the input can have three different logic values, while the output can have four different values, including the additional floating scenario. When floating, the gate operates as a DRAM (Dynamic Random Access Memory) and the current output is determined by the previous value. The vector that estimates the probability of the previous value to be the logic values of '0', '1' and '2' is therefore given by

$$\boldsymbol{P_{pre}} = [\text{p}_{\text{pre=0}} \quad \text{p}_{\text{pre=1}} \quad \text{p}_{\text{pre=2}}]. \tag{6}$$

So for an input '*i*', the probability for the output being '*j*' is calculated as

$$P_{j|i} = Prob_{j|i} + Prob_{floating|i} * p_{pre=j}. \tag{7}$$

Assume $\text{p}_{\text{pre=0}} = \text{p}_{\text{pre=1}} = \text{p}_{\text{pre=2}} = \frac{1}{3}$; using the analysis in the previous section, Ps=Po=0.05. So, the values of the conditional probabilities are now given in Table 6:

Table 6. Output probabilities of the proposed STI

Input	Output=0	Output=1	Output=2
0	$P_{0\|0} = 0.0673$	$P_{1\|0} = 0.0579$	$P_{2\|0} = 0.8748$
1	$P_{0\|1} = 0.0945$	$P_{1\|1} = 0.8160$	$P_{2\|1} = 0.0895$
2	$P_{0\|2} = 0.9524$	$P_{1\|2} = 0.0429$	$P_{2\|2} = 0.0047$

Table 6 can then be expressed by a single equation given by:

$$\begin{aligned} Output_{inverter} = {} & \left(2 * P_{2|0} + 1 * P_{1|0} + 0 * P_{0|0}\right) * P_{input=0} \\ & + \left(2 * P_{2|1} + 1 * P_{1|1} + 0 * P_{0|1}\right) * P_{input=1} \\ & + \left(2 * P_{2|2} + 1 * P_{1|2} + 0 * P_{0|2}\right) * P_{input=2} \\ = {} & \textstyle\sum_{\text{i=0}}^{2}(P_{input=i} * \sum_{\text{j=0}}^{2} j * P_{j|i}) \end{aligned} \tag{8}$$

By a similar process, the transistor level equation of any ternary gate can be found. Table 7 shows the results for the NMIN operator of Fig. 2(b), while Table 8 shows the results for the NTI and the PTI of Fig. 3.

Table 7. Output probabilities of the NMIN operator

Inputs	Output=0	Output=1	Output=2
00	$\text{P}_{0\|00} = 0.0192$	$\text{P}_{1\|00} = 0.0189$	$\text{P}_{2\|00} = 0.9619$
01	$\text{P}_{0\|01} = 0.0206$	$\text{P}_{1\|01} = 0.0586$	$\text{P}_{2\|01} = 0.9208$
02	$\text{P}_{0\|02} = 0.0648$	$\text{P}_{1\|02} = 0.0603$	$\text{P}_{2\|02} = 0.8749$
10	$\text{P}_{0\|10} = 0.0206$	$\text{P}_{1\|10} = 0.0586$	$\text{P}_{2\|10} = 0.9208$
11	$\text{P}_{0\|11} = 0.0477$	$\text{P}_{1\|11} = 0.8148$	$\text{P}_{2\|11} = 0.1375$
12	$\text{P}_{0\|12} = 0.0906$	$\text{P}_{1\|12} = 0.7780$	$\text{P}_{2\|12} = 0.1314$
20	$\text{P}_{0\|20} = 0.0648$	$\text{P}_{1\|20} = 0.0603$	$\text{P}_{2\|20} = 0.8749$
21	$\text{p}_{0\|21} = 0.0906$	$\text{P}_{1\|21} = 0.7780$	$\text{P}_{2\|21} = 0.1314$
22	$\text{p}_{0\|22} = 0.9069$	$\text{P}_{1\|22} = 0.0797$	$\text{P}_{2\|22} = 0.0134$

Table 8. Output probabilities of the NTI and PTI operator

Type	Input	Output=0	Output=1	Output=2
NTI	0	$P_{0\|0} = 0.0738$	$P_{1\|0} = 0$	$P_{2\|0} = 0.9262$
	1	$P_{0\|1} = 0.9512$	$P_{1\|1} = 0$	$P_{2\|1} = 0.0488$
	2	$P_{0\|2} = 0.9512$	$P_{1\|2} = 0$	$P_{2\|2} = 0.0488$
PTI	0	$P_{0\|0} = 0.0738$	$P_{1\|0} = 0$	$P_{2\|0} = 0.9262$
	1	$P_{0\|1} = 0.0738$	$P_{1\|1} = 0$	$P_{2\|1} = 0.9262$
	2	$P_{0\|2} = 0.9512$	$P_{1\|2} = 0$	$P_{2\|2} = 0.0488$

B. Quaternary logic

The previously designed quaternary inverter is considered as a further example to show that the proposed method is applicable at a higher base of 4.

Table 9. All possible scenarios of quaternary inverter when Input<0.3V (Logic 0). ("Floating" indicates that both pull-up and pull-down networks are turned off. N: normal; S: short defect; O: open defect; X: don't care; '/' means 'or'.)

Scenario	Probability	OUT logic
TP1:X;TP2:X;TP3:X; TN1:S;TN2:X;TN3:X;	Ps	0
TP1:N/S;TP2:N/S;TP3:N/S; TN1: N/O; TN2:S;TN3:S.	$(1-\mathrm{Po})^3(1-\mathrm{Ps})\mathrm{Ps}^2$	1
TP1:N/S;TP2:N/S;TP3:N/S; TN1:N/O;TN2:S;TN3:N/O.	$(1-\mathrm{Po})^3(1-\mathrm{Ps})\mathrm{Ps}(1-\mathrm{Ps})$	1
TP1:N/S;TP2:N/S;TP3:O; TN1: N/O; TN2:S;TN3:X.	$(1-\mathrm{Po})^2\mathrm{Po}(1-\mathrm{Ps})\mathrm{Ps}$	1
TP1:N/S;TP2:N/S;TP3:N/S; TN1:N/O;TN2:N/O;TN3:S.	$(1-\mathrm{Po})^3(1-\mathrm{Ps})^2\mathrm{Ps}$	2
TP1:N/S;TP2:O;TP3:N/S; TN1: N/O; TN2:S;TN3:S.	$(1-\mathrm{Po})^2\mathrm{Po}(1-\mathrm{Ps})\mathrm{Ps}^2$	2
TP1: N/S; (TP2 OR TN2): O; (TP3 OR TN3): O;	$(1-\mathrm{Po})(1-\mathrm{Ps})(1-(1-\mathrm{Po})\mathrm{Ps})^2$	3
TP1: O; (TP2-TN2 PATH OR TP3-TN3 PATH): S;	$\mathrm{Po}(1-\mathrm{Ps})[1-(1-(1-\mathrm{Po})\mathrm{Ps})^2]$	0
TP1: O; (TP2 OR TN2): O; (TP3 OR TN3): O;	$Po(1-Ps)(1-(1-Po)Ps)^2$	Floating

Using the expressions in Table 9, the output probability distributions for an input at logic 0 can be calculated as shown in Table 10.

Table 10. Output probabilities of quaternary inverter when Input<0.3V (Logic 0)

Output	Probability
0	$\mathrm{Prob}_{0\|0} = \mathrm{Ps} + \mathrm{Po}(1-\mathrm{Ps})[1-(1-(1-\mathrm{Po})\mathrm{Ps})^2]$
1	$\mathrm{Prob}_{1\|0} = (1-\mathrm{Po})^2(1-\mathrm{Ps})\mathrm{Ps}$
2	$\mathrm{Prob}_{2\|0} = (1-\mathrm{Po})^2(1-\mathrm{Ps})[1-(1-\mathrm{Po})\mathrm{Ps}]\mathrm{Ps}$
3	$\mathrm{Prob}_{3\|0} = (1-\mathrm{Po})(1-\mathrm{Ps})(1-(1-\mathrm{Po})\mathrm{Ps})^2$
Floating	$\mathrm{Prob}_{\mathrm{floating}\|0} = \mathrm{Po}(1-\mathrm{Ps})(1-(1-\mathrm{Po})\mathrm{Ps})^2$

As previously discussed, the output probabilities for input = 1, 2 and 3 are calculated and shown in Table 11.

Table 11. Output probabilities of a quaternary inverter

Input	Output=0	Output=1	Output=2	Output=3
0	$P_{0\|0} = 0.0652$	$P_{1\|0} = 0.0536$	$P_{2\|0} = 0.0516$	$P_{3\|0} = 0.8296$
1	$P_{0\|1} = 0.0942$	$P_{1\|1} = 0.0440$	$P_{2\|1} = 0.7769$	$P_{3\|1} = 0.0849$
2	$P_{0\|2} = 0.0972$	$P_{1\|2} = 0.8146$	$P_{2\|2} = 0.0795$	$P_{3\|2} = 0.0087$
3	$P_{0\|3} = 0.9525$	$P_{1\|3} = 0.0429$	$P_{2\|3} = 0.0042$	$P_{3\|3} = 0.0004$

C. Generalized transistor level analysis

As indicated by (8), for any MVL gate with *d+1* possible logic values (0, 1, 2, …, d), the final output of this gate can be described by the following equation:

$$\text{Output} = \sum_j P(input = j) * (\sum_{i=0}^{d} i * P(i|j)), \quad (9)$$

where *j* is the index to an input from the set of all input vectors. (9) has significant implications on the reliability evaluation of a MVL gate. So rather than simply assuming that the gate is affected by a given probability, (9) describes the probabilistic behavior based on a physical structure, therefore providing a more detailed characterization and evaluation (as detailed in the next section).

V. Stochastic Computational Models for MVLs

In this section, different stochastic computation models (SCMs) are analyzed for reliability evaluation of ternary/quaternary inverters, an arbitrary MVL gate and a MVL combinational circuit.

A. Ternary and quaternary inverters

As discussed in [7, 8], stochastic computation transforms Boolean logic operations into a probabilistic computation in the real domain. In this process the so-called stochastic multiplexer plays an important role. A *stochastic multiplexer* is equivalent to a weighted adder and its function can be described by:

$$Output = \sum_{j\in A} P_j * I_j, \quad (10)$$

where *A* represents the set of all combinations of the control bits, P_j is the probability of the control vector being *j*, and I_j represents the input value corresponding to the scenario for the control vector *j*.

(10) can then be used as basis for a stochastic computational model (SCM) as applicable to MVL gates. The SCM for the proposed STI is shown in Fig. 10(a). The sequences of all three inputs can be determined using Table 6. In this case, a sequence length of 10000 is employed. The first sequence corresponding to input = '0', as discussed previously, consists of 673 0's, 579 1's and 8747 2's. The second input sequence consists of 945 0's, 8160 1's and 895 2's. The third input sequence consists of 9523 0's, 429 1's and 47 2's.

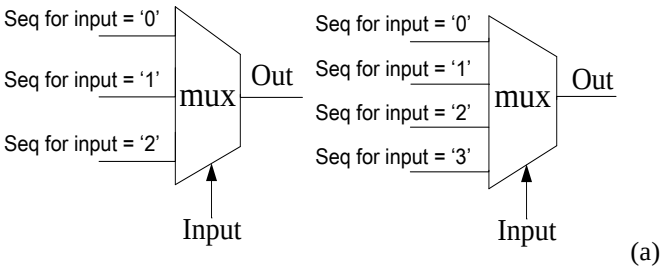


Fig. 10 Stochastic computational model for (a) a ternary inverter (b) a quaternary inverter

Therefore, each sequence can be described by the following expression:

$$\text{Output}(j) = \sum_{i=0}^{2} i * P(i|j) \quad (11)$$

With the stochastic multiplexer function and (11), the equation of the final output of this gate is given by:

$$\text{Output} = \sum_{j=0}^{2} P(input = j) * \text{Output}(j) \quad (12)$$

By combining (11) and (12), it is clear that Fig. 10(a) is an implementation of (8) (or the more general expression given by (9)). Similarly to the previous discussion for Table 11, a general stochastic computation model can also be obtained for a quaternary inverter. Fig. 10(b) shows the SCM for a quaternary inverter.

The ternary and quaternary NMIN operators can also be evaluated by the proposed approach. The SCM is a general framework that is applicable to the reliability evaluation of any MVL gate. Due to space limitation, however, this is not discussed in detail in this paper.

B. SCMs for combinational MVLs

Based on the proposed SCM, a stochastic computational network can be constructed using the SCMs of the gates for circuit reliability evaluation. As discussed in [7, 8], the computational network is a nonlinear structure constituted by SCMs. Feeding stochastic input sequences into the network and propagating them from the primary inputs to the outputs calculate the output probabilities. A distinguishing feature of the SCM approach is that it handles reconvergent fanouts at a very small effort; when signals are processed in the form of bit streams (such as consisting of 0's, '1' and '2's in ternary logic case), logic operations do not need to consider the correlation caused by reconvergent fanouts. Moreover, signal dependencies are inherently maintained in the distribution patterns of the random bit streams. A detailed analysis and discussion of these features can be found in [7, 8].

So, the evaluation procedure using the proposed SCM approach for a ternary circuit can be described as follows:

1. Compute the error rate for the CNTFET and execute the transistor level analysis for every type of ternary logic gates;
2. Construct the stochastic computational model by replacing every logic gate with a ternary multiplexer;
3. Generate the initial random bit streams by encoding the output distributions for every input vector. These random bit streams are used as inputs of the multiplexers;
4. Propagate the bit streams from the primary inputs to the outputs and obtain a random bit stream for each output;
5. Decode the signal probability and calculate the reliability of each output from the obtained random bit stream.

An example of a MVL circuit is analyzed in more detail next. As discussed in [3], a ternary decoder is required for designing arithmetic circuits such as ternary adders and multipliers. The ternary decoder is a one-input and three-output combinational circuit that generates unary functions for the input *X*; the function of the ternary decoder is described by:

$$X_k = \begin{cases} 2, & \text{if } X = k \\ 0, & \text{if } X \neq k \end{cases} \quad (13)$$

where *k* has a logic value of 0, 1, or 2.

Using the proposed pseudo complementary ternary gates (STI, NTI, PTI and NMIN) as discussed in Section III, a decoder is designed; this circuit is functionally equivalent as the design proposed in [3].

Based on Section IV, the SCM for the decoder in Fig. 11 is constructed by replacing each gate with a multiplexer, as shown in Fig. 12. Simulation was performed on a PC with an Intel(R) Core(TM) i5-2430M CPU @ 2.40GHz and a 4.00 GB RAM. Table 12 shows the simulation results.

As shown in Table 12, even if the number of gates in the decoder is small, the joint reliability is rather low; this is due to the low reliability of each gate. This suggests that to enhance reliability, the fabrication process of CNTFET gates should be improved and fault-tolerant techniques must be applied. Also, the time for SCM simulation is very small.

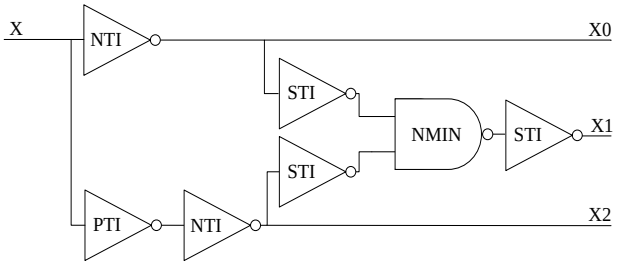


Fig. 11 Schematic diagram of the ternary decoder.

Table 12. Simulation results of the decoder using SCMs (sequence length = 10000 bits)

Input	Joint reliability	Simulation Time (s)
0	0.6737	0.068443
1	0.5346	0.071037
2	0.6905	0.070564
random	0.6407	0.063327

VI. CONCLUSION

This paper has presented the design and reliability evaluation of multiple valued logic (MVL) gates. A pseudo complementary implementation of MVL based on CNTFETs has been proposed; it replaces the resistors used in [2] with p-type CNTFETs (with their gates connected to ground) and utilizes threshold voltage operation by adjusting the chirality and the number of CNTs in each CNTFET. Therefore, this approach (referred to as *pseudo complementary*) exploits the similarities in threshold voltage control in the p- and n-types

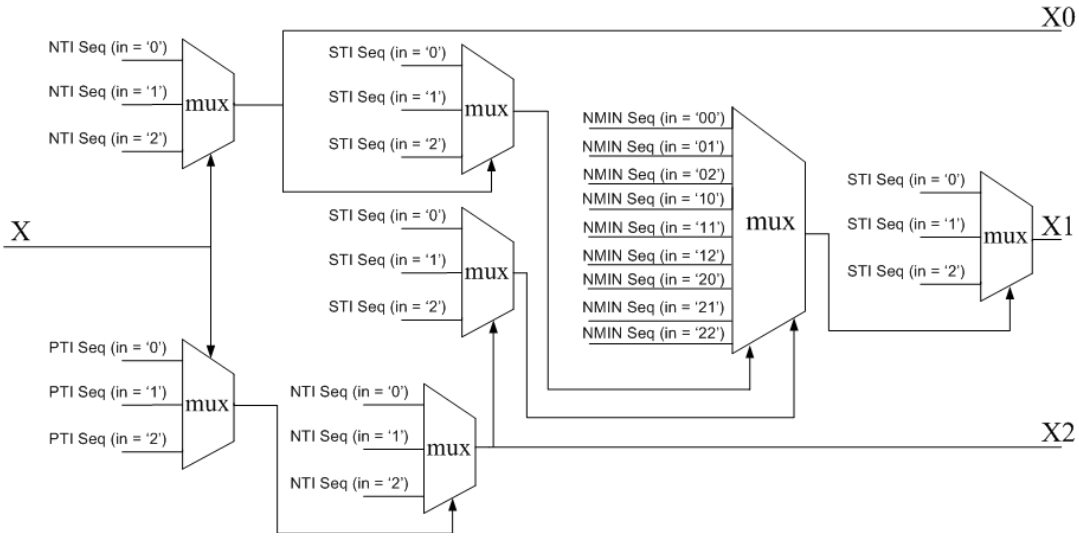


Fig. 12 Reliability evaluation using stochastic computational models for the ternary decoder.

while ensuring a correct MVL design for both ternary and quaternary logic gates. Simulation results using HSPICE have confirmed the validity of the proposed pseudo complementary approach.

A transistor-level analysis has further been proposed to accurately estimate the error rate of the MVL gates; this analytical approach is based on the structure of the gate so it is significantly different from previous approaches that assume the same error rate for all logic gates. A general stochastic computational model for reliability evaluation of MVL gates has also been proposed. The initial application of this approach to MVL circuits has been briefly presented by simulating a ternary decoder.

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