Design and Evaluation of Multiple Valued Logic Gates using Pseudo N-type Carbon Nanotube FETs

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Abstract—Multiple valued logic (MVL) circuits are particularly attractive for nanoscale implementation as advantages in information density and operating speed can be harvested using emerging technologies. In this paper, a new family of MVL gates is proposed for implementation using carbon nanotube field effect transistors (CNTFETs). The proposed designs use pseudo N-type CNTFETs and no resistor is utilized for their operation. This approach exploits threshold voltage control of the P-type and N-type transistors, while ensuring correct MVL operation for both ternary and quaternary logic gates. This paper provides a detailed assessment of several figures of merit, such as static power consumption, switching power consumption, propagation delay and the power-delay product (PDP). Compared with resistor-loaded designs, the proposed pseudo-NCNTFET MVL gates show advantages in circuit area, power consumption and energy efficiency, while still incurring a comparable propagation delay. Compared to a complementary logic family, the pseudo-NCNTFET MVL logic family requires a smaller circuit area with a similar propagation delay on average, albeit with a larger PDP and static power consumption. A design methodology and a discussion of issues related to leakage and yield are also provided for the proposed MVL logic family.

***Index Terms*— Multiple valued logic (MVL), carbon nanotube field effect transistor (CNTFET), logic design, emerging technologies.**

I. INTRODUCTION

The scaling of CMOS technology has not only brought significant improvements in integrated circuits, but it has also raised concerns over power consumption in advanced digital designs. As CMOS approaches physical and technological limits, new devices have been proposed to implement nanoscale circuits, such as those based on multiple-valued logic (MVL) operations. MVL allows for more than two levels of logic; implementations of ternary and quaternary logic have been advocated for various applications [1]. MVL enjoys many advantages over its binary counterpart; for example, each wire can transmit more information, so the number of interconnections in a chip can be reduced, resulting in a lower circuit complexity. However, MVL circuits are subject to issues such as a lower noise margin in CMOS-based implementations.

Recently, several novel devices have been proposed for MVL design; for instance, quantum-dot gate FETs (QDGFET) [2], that are based on quantum-dot cellular automata (QCA), have been suggested for ternary combinational logic design. In [3], single electron tunneling (SET) devices have also been proposed for designing multiple-valued memory cells. Reversible logic has also been shown to be a potential candidate for MVL [4]. In particular, carbon nanotube field-effect transistors (CNTFETs) have attracted significant attention as an alternative to silicon-based MOSFETs for implementing MVL gates and circuits [5, 6, 7].

A CNTFET has many potential advantages (such as high mobility of charge carriers and subthreshold operation due to its gate geometry) over silicon-based CMOS [8, 9]. CNTFET circuits could provide significant power-delay-product (PDP) benefits over CMOS at the 16 nm technology node [10]; however, several challenges must be overcome before these performance benefits can be fully realized in fabricated devices. For economic feasibility, large-scale, high-density, aligned arrays of single-walled nanotubes (SWNTs) have been manufactured by guided chemical vapor deposition (CVD) growth on commercially available single-crystal quartz substrates [11] as a first step to fabricate CNTFETs that are compatible with current CMOS processes. Fabrication in [12] is based on transferring aligned CNTs from quartz substrates to Si/SiO2 substrates followed by electrode patterning. Novel fault-tolerant techniques have also been developed to alleviate non-idealities in CNTFET fabrication, such as the presence of metallic CNTs; a stochastic modeling and analysis [13] and a metallic-CNT tolerant SRAM architecture [14] have been proposed as possible solutions by utilizing uncorrelated CNTs in series to lower the probability of a shortening defect.

In the technical literature, several approaches have appeared for designing MVL gates and circuits based on CNTFETs. Resistor-loaded designs utilize fewer transistors to implement MVL gates; however, the chip implementation of a resistor and the large static power consumption limit their integration [5]. Complementary designs can be fully integrated and consume significantly lower static power, but they utilize additional transistors [6]. A dynamic ternary logic design using CNTFETs has been proposed in [7]. A new MVL family is proposed in this paper; this approach trades off static power consumption and circuit area (as given by the number of transistors). The proposed gate designs use N-type CNTFETs as switches and

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P-type CNTFETs as loads; therefore, they are referred to as a pseudo N-type CNTFET (NCNTFET) MVL family.

This paper extends the contribution of [15], in which pseudo-NCNTFET based MVL designs were presented as an alternative to [5] and [6]; the reliability of those designs was evaluated using stochastic computational models [16-18]. This paper makes additional contributions by presenting a detailed assessment of several figures of merit, such as static power and switching power consumption, propagation delay, the power-delay product (PDP) and circuit area. The proposed designs are then compared with both resistor-loaded and complementary CNTFET MVL designs [5, 6].

The rest of this paper starts with a review of related CNTFET MVL designs in Section II. Section III presents the proposed gates using pseudo-NCNTFET MVL designs and the HSPICE simulation results. Section IV presents the comparison results of the proposed gates with previous designs. Section V discusses the impacts of using multiple tubes. Section VI discusses leakage and Section VII provides a design methodology for the proposed logic family. Section VIII discusses yield and manufacturing issues, followed by the conclusion in Section IX.

II. Resistor-loaded and Complementary CNTFET MVL Designs

The high mobility of charge carriers and reduced subthreshold slopes in gate geometry make the CNTFET a promising candidate as a post-CMOS device [8, 9]. Fig. 1 illustrates the device structure of a CNTFET with four ideal single-walled semiconductor CNTs in the channel [6]. Current CNT fabrication processes are not ideal; in addition to traditional CMOS fabrication defects (such as open and bridge contacts), a CNTFET manufacturing process also suffers from variation-based effects in CNT diameter and bandgap.

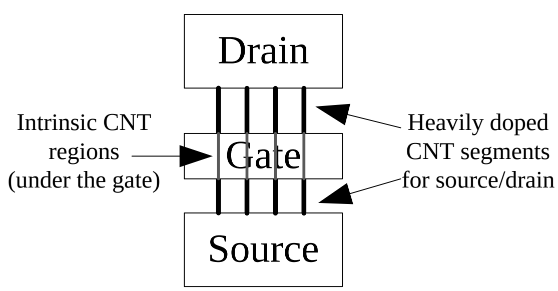


Fig. 1. CNTFET structure with four CNTs in the channel.

Ternary logic gates have been designed using CNTFETs [5, 6, 7]. These gates are based on the novel feature that carbon nanotubes of different diameters in CNTFETs have different threshold voltages. For resistor-loaded MVL [5] and complementary MVL families [6], Figs. 2 and 3 show the schematics of standard ternary inverters (STIs), positive ternary inverters (PTIs), negative ternary inverters (NTIs) and standard quaternary inverters (SQIs). Although these designs either incur a large overhead due to the large resistance and power dissipation or resort to additional transistors, their design principles are valuable, because they establish some important features for CNTFET-based MVL operation.

III. Pseudo-NCNTFET MVL Gates

A pseudo-NCNTFET implementation is proposed next. The proposed design replaces the resistors used in [5] with P-type CNTFETs (with the gate connected to ground), while threshold voltage control is accomplished by adjusting the chirality and the number of CNTs in each CNTFET. This approach exploits the similarities in threshold voltage control of the P- and N-type CNTFETs, while ensuring a correct MVL operation for both ternary and quaternary logic gates.

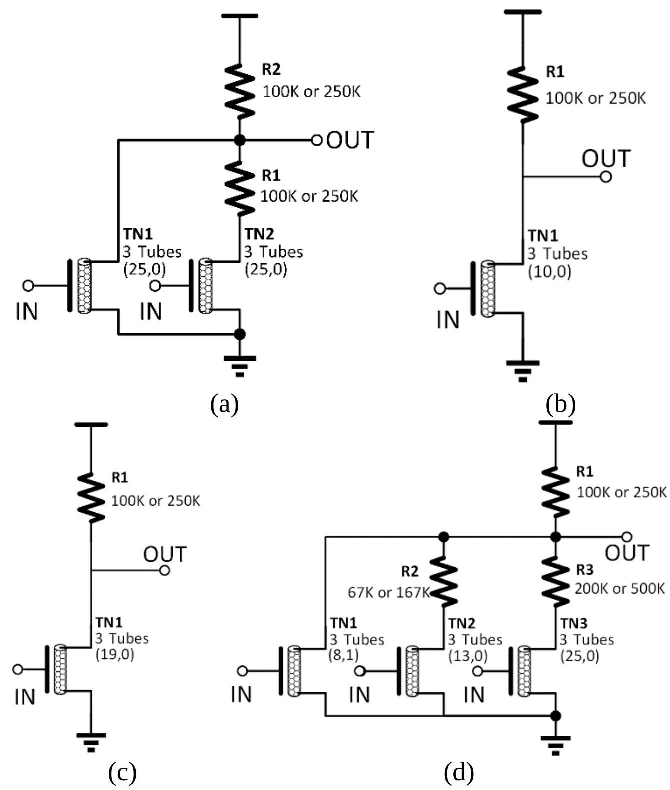
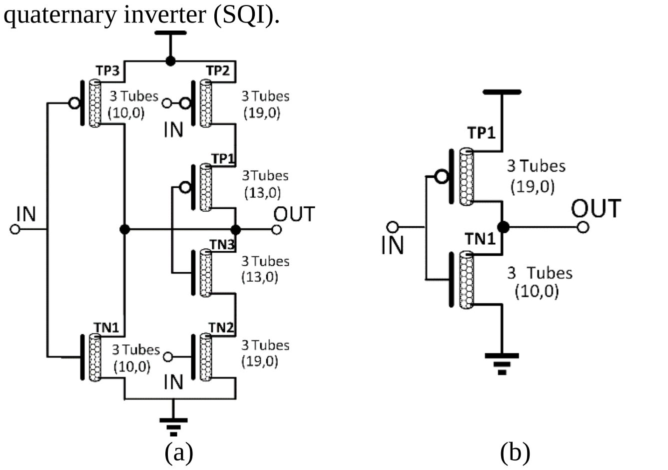
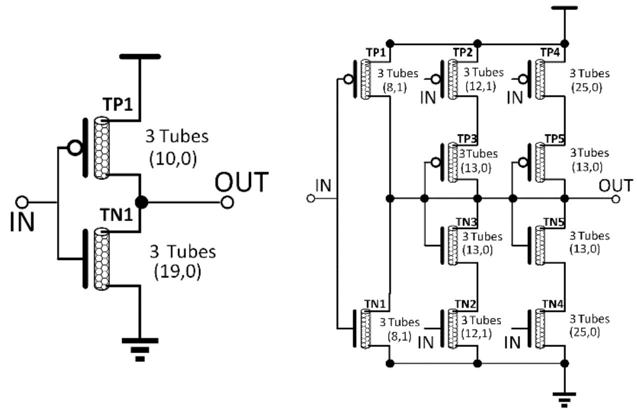


Fig. 2. Resistor-loaded CNTFET MVL gates [5]: (a) standard ternary inverter (STI); (b) positive ternary inverter (PTI); (c) negative ternary inverter (NTI); and (d) standard quaternary inverter (SQI).





(c) (d)

Fig. 3. Complementary CNTFET MVL gates [6]: (a) standard ternary inverter (STI); (b) positive ternary inverter (PTI); (c) negative ternary inverter (NTI); and (d) standard quaternary inverter (SQI).

A. Pseudo-NCNTFET ternary gates

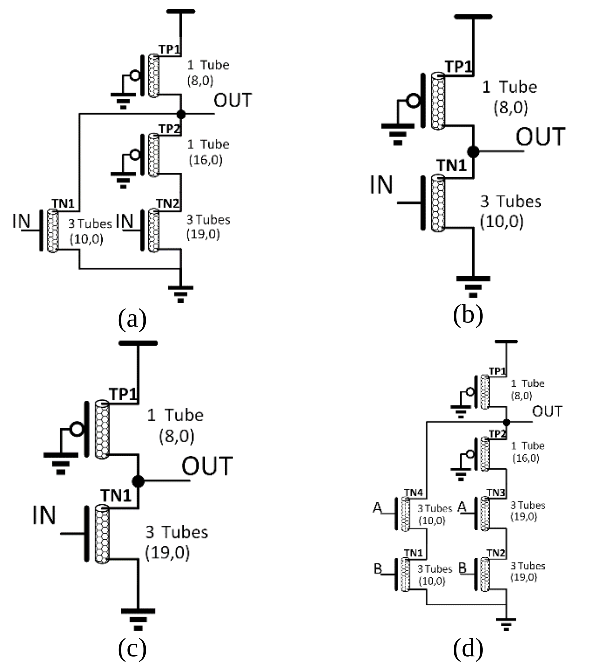


Fig. 4. Pseudo-NCNTFET MVL gates: (a) standard ternary inverter (STI) and (b) positive ternary inverter (PTI) (c) negative ternary inverter (NTI) and (d) ternary NMIN operator.

Table 1. Truth table for the three ternary inverters

Input	STI	NTI	PTI
0	2	2	2
1	1	0	2
2	0	0	0

Consider first the ternary operation. There are three types of ternary inverters (Table 1): standard ternary inverter (STI), negative ternary inverter (NTI) and positive ternary inverter (PTI). Fig. 4(a) shows the proposed pseudo-NCNTFET STI using CNTFETs, while Fig. 4 (b) and (c) show the PTI and NTI implementations respectively. The STI consists of two N-type CNTFETs and two P-type CNTFETs. One of the CNTFETs (TP1) has a chirality of (8, 0); it is used as a pull-up network, while the other three CNTFETs are used as a pull-down network. The chiralities of TN1 and TN2 are (10, 0) and (19, 0), and the corresponding threshold voltages are 0.559 V and 0.293 V respectively. Consider an input voltage V_{in}. For small values of V_{in}, both TN1 and TN2 are OFF; hence, the output node (OUT) is held at Vdd. When V_{in} increases beyond V_{th2} (0.293 V), TN2 is turned ON. The output voltage is determined by the resistance ratio of TP1, TP2 and TN2; therefore, it is held approximately at Vdd/2 until V_{in} reaches V_{th1} (0.559 V). Once V_{in} exceeds V_{th1}, TN1 is turned ON and the output is pulled down to nearly zero.

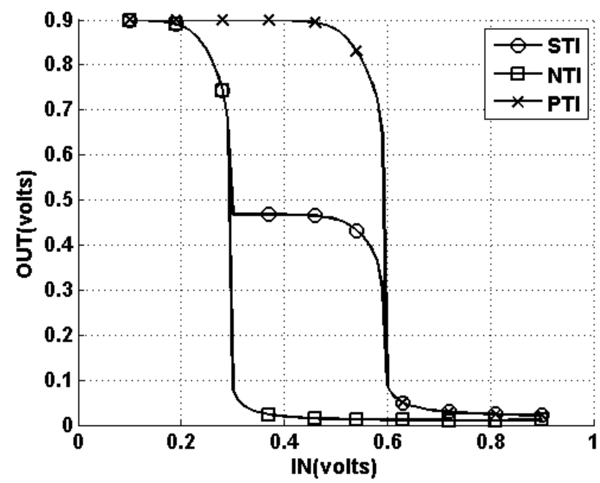


Fig. 5. Voltage transfer diagram for the pseudo-NCNTFET ternary inverters (STI, PTI and NTI).

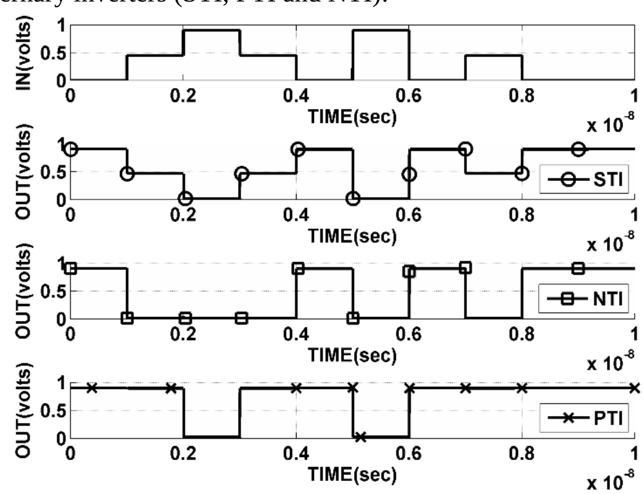


Fig. 6. Transient simulation of the pseudo-NCNTFET ternary inverters.

Table 2 Ternary NMIN Truth Table

A	B	OUT
0	0	2
0	1	2
0	2	2
1	0	2
1	1	1
1	2	1

2	0	2
2	1	1
2	2	0

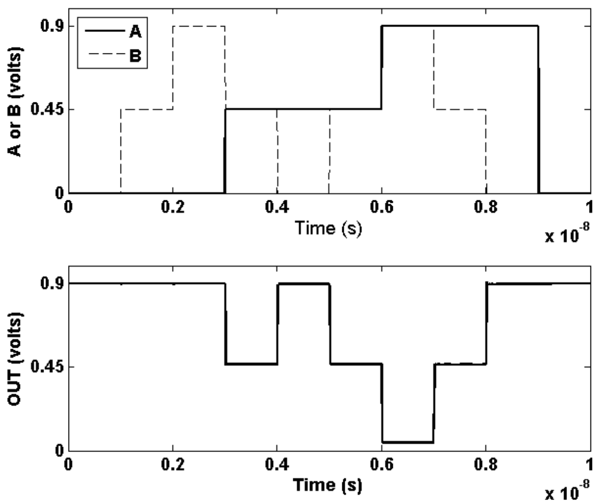


Fig. 7. Transient simulation of the pseudo-NCNTFET ternary NMIN operator.

The voltages at the output node are plotted in Figs. 5 and 6 (obtained by HSPICE simulation) for the transfer diagram and transient simulation results of the pseudo-NCNTFET ternary inverters (STI, PTI and NTI). These results show the correct operation of the proposed ternary inverters.

A pseudo-NCNTFET ternary NMIN is designed next (Fig. 4(d)). The truth table of the ternary NMIN is shown as Table 2. This gate consists of six CNTFETs with four different chiralities; similar to the ternary STI in Fig. 4(a), the CNTFETs with chiralities (10, 0) and (19, 0) have threshold voltages of 0.559 V and 0.293 V, respectively. HSPICE simulation (shown in Fig. 7) confirms the correctness of the proposed design.

B. Pseudo-NCNTFET quaternary gates

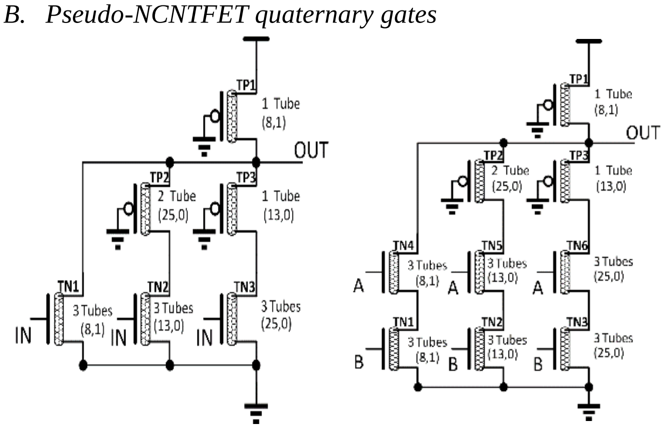


Fig. 8. Pseudo-NCNTFET quaternary logic gates: (a) an inverter and (b) an NMIN operator.

Pseudo-NCNTFET quaternary logic gates are designed in this section. Fig. 8 shows a pseudo-NCNTFET standard quaternary inverter (SQI) and an NMIN operator. The truth tables for the SQI and NMIN are shown as Tables 3 and 4.

Table 3 Standard Quaternary Inverter (SQI) Truth Table

IN	OUT
0	3
1	2
2	1
3	0

Table 4 Quaternary NMIN Truth Table

A	B	OUT	A	B	OUT
0	0	3	2	0	3
0	1	3	2	1	2
0	2	3	2	2	1
0	3	3	2	3	1
1	0	3	3	0	3
1	1	2	3	1	2
1	2	2	3	2	1
1	3	2	3	3	0

The inverter consists of three N-type CNTFETs and three P-type CNTFETs, each with a different chirality; the NMIN operator consists of six N-type CNTFETs and three P-type CNTFETs. Each of the P-type CNTFETs has a distinct chirality, while the six N-type CNTFETs have three different chiralities. Fig. 9 shows the voltage transfer diagram of the SQI. Compared to the simulation results of the ternary inverter (Fig. 5), Fig. 9 shows a reduced noise margin for the quaternary logic. Fig. 10 shows the transient simulation results of the quaternary NMIN gates by HSPICE.

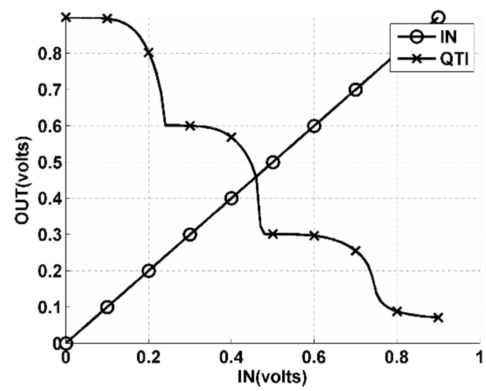


Fig. 9. Voltage transfer diagram for the pseudo-NCNETFET quaternary inverter of Fig. 8(a).

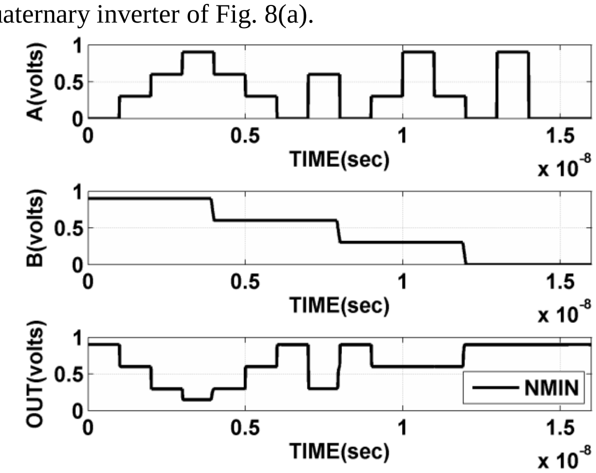


Fig.10. Transient simulation of the pseudo-NCNTFET quaternary NMIN operator.

IV. COMPARATIVE EVALUATION

In this section, comparison under various figures of merit such as power, delay, power-delay product (PDP) and circuit area is performed between resistor-loaded MVL, complementary MVL and Pseudo-NCNTFET STIs by HSPICE simulation. For resistor-loaded designs, a 100KΩ resistor is used as in [5] and a 250KΩ resistor is further considered for an improved performance.

A. STI

Fig. 11 shows the voltage transfer diagram of the resistor-loaded, complementary and pseudo-NCNTFET STIs (Figs. 2(a), 3(a) and 4(a)). When the input is gradually increased from 0 to Vdd, the proposed pseudo-NCNTFET STI has a steeper response than the resistor-loaded design, although it is not as sharp as the complementary one. Albeit this effectively increases the input/output capability of the circuit, thereby improving the functionality of the proposed design compared to the resistor-loaded one, neither resistor-loaded nor pseudo-NCNTFET STIs provide a rail-to-rail output voltage swing. However, a complementary STI can drive the output from ground to supply voltage. Thus, MVL designs based on either pseudo-NCNTFET or resistor-loaded cannot provide a larger noise margin than complementary designs.

1) Static power

There are static currents in both the resistor-loaded and the pseudo-NCNTFET designs due to the use of resistors and the always-on P-type CNTFETs for all inputs. However, there is only a limited static current in a complementary design for only a single value (Input = 1); these static currents result in static power consumption. Both the output voltage and equivalent output resistances change with the input voltage, so the static power consumption is input-voltage dependent. The simulated equivalent output resistances are shown in Table 5 and a detailed analysis of various scenarios is given below.

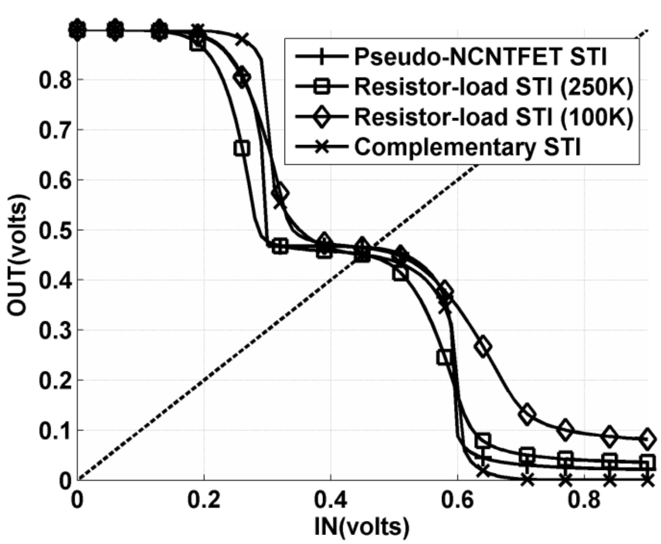


Fig. 11. Voltage transfer diagram for different STIs.

Table 5 Equivalent resistance of pseudo-NCNTFET and complementary STIs for different inputs

IN	OUT	Pseudo-NCNTFET		Complementary	
		TP1	TP2	Pull-up Network	Pull-down Network
0	2	87.3kΩ	20.3kΩ	11KΩ	1.8GΩ
1	1	216kΩ	230kΩ	648KΩ	688KΩ
2	0	437kΩ	38GΩ	7.78GΩ	78GΩ

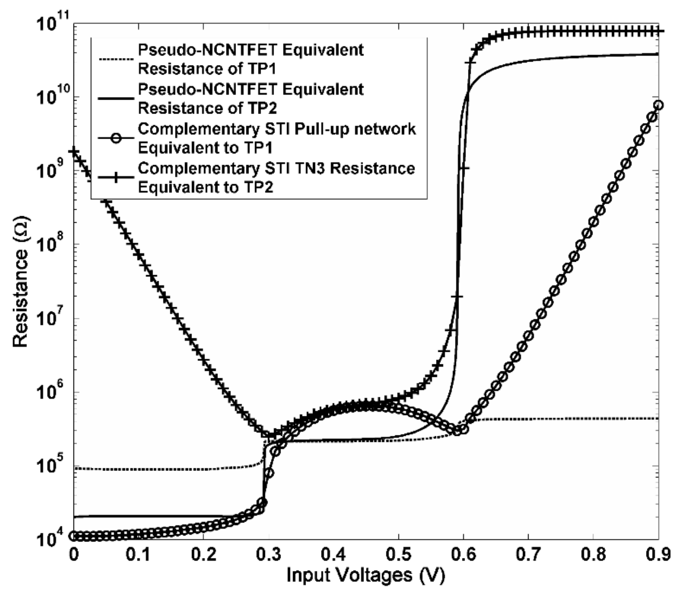


Fig. 12. Equivalent resistance of the P-type CNTFET in the pseudo-NCNTFET STI and complementary STI designs at different input voltages

- When the input is logic 0, TN1 and TN2 in all three designs (as shown in Fig. 2(a), Fig. 3(a) and Fig. 4(a)) are OFF (a detailed discussion has been presented in Section III). Since the output is expected to be logic 2 and the P-type CNTFET has a strong capability to transfer a high voltage, TP1 and TP2 in the pseudo-NCNTFET STI (Fig. 4(a)) are both working in the deep triode region (or deep linear region). The equivalent resistances of TP1 and TP2 are small and negligible, as shown in Fig. 12. TP3 and TP2 in a complementary STI (in Fig. 3(a)) are both turned ON and operate in the deep triode region. Therefore the static power consumptions for all three designs are very small under this scenario, as confirmed by the HSPICE simulation results in Fig. 13.
- When the input is logic 1, for the pseudo-NCNTFET STI, TN2 is ON and TN1 is OFF. TP1 and TP2 both work in the saturation region, and the equivalent resistances are used as voltage divider to determine the output voltage (the resistance of TN2 is very small and thus negligible). Thus, the equivalent resistances of TP1 and TP2 should be similar. In the proposed design, simulation has shown that this equivalent resistance is approximately 220 KΩ (Fig. 12). Hence, the static power consumption for the proposed design is significantly smaller than for the 100 KΩ resistor-loaded design but slightly larger than for the 250 KΩ resistor-loaded design (Fig. 13).

As mentioned previously, static power consumption must be accounted for this input using the complementary STI. This occurs because the logic 1 output is also obtained from a voltage divider that is implemented by always-ON CNTFETs. However, due to the larger equivalent resistances (as shown in Table 5, equivalent resistances of 648KΩ for the pull-up network and 688KΩ for the pull-down network), the static power consumption of a complementary STI is smaller than its pseudo-NCNTFET counterpart (as clearly illustrated in Fig.13).

- When the input is logic 2, both TN1 and TN2 are ON. The output is expected to be logic 0, so TP1 is ON, while TP2 works in the triode region. Although TP1 is still in the saturation region in this scenario, the drain voltage has decreased from Vdd/2 to 0. The higher voltage drop across TP1 has resulted in a larger current through TP1 due to second-order effects; however, the equivalent resistance of TP1 increases to approximately 400 KΩ (Fig.12). Since the P-type FET has a poor capability to transfer a low voltage, the equivalent resistance of TP2 is much larger than for the previous scenario (also shown in Fig. 12). These larger resistances lead to a lower static power consumption of the pseudo-NCNTFET design compared to the resistor-loaded design (Fig. 13). Since there is no DC path in a complementary STI for this input, its static power consumption is close to 0 (Fig. 13). This result can be further verified in Table 5, i.e. an equivalent output resistance of 437 kΩ || 38 GΩ = 437 kΩ for the pseudo-NCNTFET STI and an equivalent output resistance of 7.78 GΩ || 78 GΩ = 7.78 GΩ for the complementary STI.

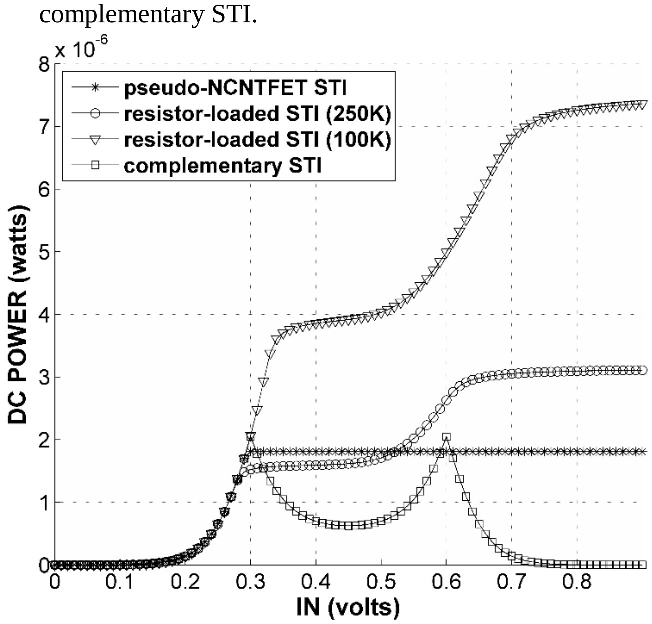


Fig. 13. Static power consumptions of different STIs.

2) Switching power

The switching power, P, of these designs consists of two parts: the power consumption due to charging of the output capacitance (P_c) and the power consumption due to the "short path" formed during switching (P_s). Hence,

$$P = P_c + P_s. \tag{1}$$

P_c and P_s are obtained respectively as follows.

Initially, the power consumption resulting from charging the output capacitance is found. This is estimated using the following equation:

$$P_c = E_c \cdot f \cdot A, \tag{2}$$

where E_c is the energy consumed per transition by charging the capacitance, f is the clock frequency and A is the active switching factor on a single path.

Usually, we can have,

$$E_c = C_{out} \cdot (\Delta V)^2, \tag{3}$$

where C_{out} is the effective output capacitance, consisting of the internal parasitic and external load capacitances, ΔV is the output voltage difference before and after the transition. Hereafter, it is assumed that the STI is unloaded for both the pseudo-NCNTFET and resistor-loaded designs.

The parasitic capacitances for both the pseudo-NCNTFET and resistor-loaded logic at different output levels are shown in Table 6. The complementary design has the largest load capacitance among the three considered schemes, while the resistor-loaded design has the smallest capacitance. The difference is however very small due to the parasitic drain capacitance. Due to non-idealities in the resistor-loaded and pseudo-NCNTFET designs, the voltage change ΔV is smaller than 0.45 V for the 0-1 and 1-2 transitions and smaller than 0.9 V for the 0-2 transition (Table 6). ΔV is larger for the 0-1 and 0-2 transitions of the pseudo-NCNTFET design than the resistor-loaded design due to the lower output voltage value of logic 0. However, the transition voltage of the complementary design is close to the ideal case due to the negligible impact of non-idealities.

Table 6 Equivalent capacitance and transition voltage

Transition Voltage, ΔV (mV)			
	Pseudo-NCNTFET	Resistor-loaded	Complementary
0-1 transition	442.4	355.1	450
0-2 transition	878.4	818.1	900
1-2 transition	436.0	437.0	450
Equivalent Capacitance, C_{out} (aF)			
OUT	Pseudo-NCNTFET	Resistor-loaded	Complementary
2	68.1	67.8	74.4
1	44.7	43.9	68.4
0	6.29	6.28	42.3

If the same input distribution is assumed, the switching factor A is the same for both designs; therefore, the power consumption of the proposed pseudo-NCNTFET design P_c is slightly larger than the resistor-loaded design, while the complementary design has the largest P_c among the three types.

Next, the power consumption due to the short circuit path from Vdd to ground in a transition is evaluated. The short circuit path can be viewed as resistive from Vdd to ground; the total resistance from Vdd to ground varies for each type of transition. The power consumption due to this short circuit path is given by:

$$P_s = E_s \cdot f \cdot A, \tag{4}$$

where E_s is the energy consumed per transition due to the short circuit, f is the clock frequency and A is the active switching factor on a single path. Furthermore, E_s is given by:

$$E_s = \int_{t_1}^{t_2} \frac{V_{dd}^2}{R(t)} dt, \quad (5)$$

where, $t_1 \sim t_2$ is the transition time, usually defined as the time interval between 10% and 90% of the voltage difference in a transition, R(t) is the equivalent resistance of the short path during the transition. Hence, E_s is also affected by the input signal slope due to its effect on the switching time interval ($t_1 \sim t_2$).

As shown in Fig. 12, the average equivalent resistances of the pseudo-NCNTFET design are larger than those of the resistor-loaded design, while the complementary design has the largest average equivalent resistance; so for the same values of f and A, P_s of the proposed design is smaller than P_s of the resistor-loaded design under the same conditions for a transition, and the complementary design has the smallest P_s.

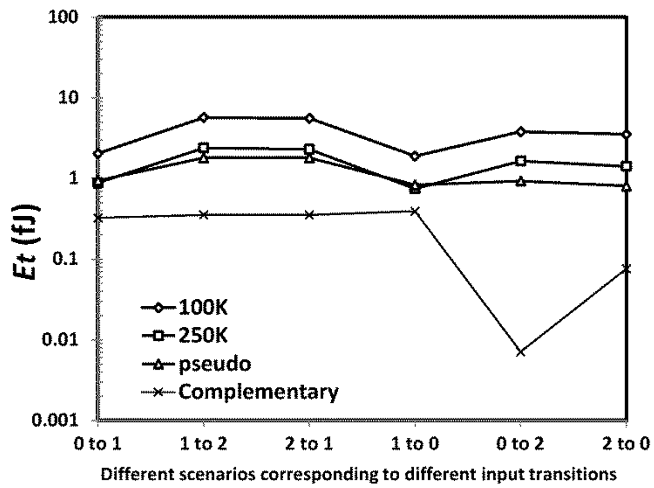


Fig. 14. Total transition energy for different transitions in the STIs.

The switching power P is evaluated as

$$P = E_t \cdot f \cdot A, \quad (6)$$

where, $E_t = E_c + E_s$. Simulation has shown that the short circuit power consumption is the main power consumption during switching, i.e. E_t is dominated by E_s. The total transition energy E_t at each different transition has been simulated using HSPICE. As shown in Fig 14, E_t is smaller for the pseudo-NCNTFET compared to the resistor-loaded design. It also confirms the analysis that the complementary design incurs the smallest switching power.

3) Propagation Delay

In the traditional RC model, the propagation delay is dependent on the output node capacitance and resistance. As shown in Fig. 12 and Table 6, the equivalent capacitances of the output node for the three types of design are similar, thus the delay is dominated by the average equivalent resistance. As shown in Fig. 12, the 100KΩ resistor-loaded design has the lowest equivalent resistance, while the 250KΩ resistor-loaded design has the largest equivalent resistance. Therefore, the 100KΩ resistor-loaded design has the smallest overall propagation delay, while the 250KΩ resistor-loaded design has the largest overall propagation delay (as confirmed by HSPICE simulation in Fig. 15). The delays of the pseudo-NCNTFET and complementary designs are between the 100KΩ and 250KΩ resistor-loaded design cases.

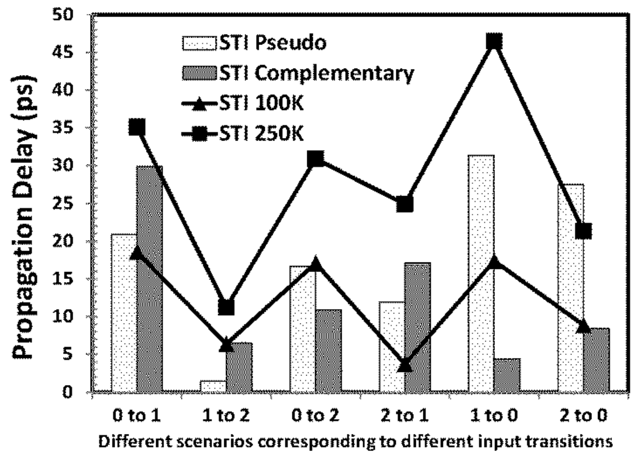


Fig. 15 Propagation delay of STIs

4) Power Delay Product (PDP)

The PDP of a logic gate is defined as,

$$PDP = E_t \cdot f \cdot A \cdot t_p \quad (7)$$

where E_t is the transition energy, f is the clock frequency and A is the active switching factor on a single path, t_p is the propagation delay of the gate. For ease of analysis, $f \cdot A$ is assumed to be the same for all designs; so by normalizing $f \cdot A$ to 1, the PDP is given as,

$$PDP_{norm} = E_t \cdot 1 \cdot t_p = E_t \cdot t_p \ (\mathrm{J \cdot s}) \quad (8)$$

Using the above analysis and the simulation results for the switching power consumption E_t and the propagation delay, the PDP_{norm} of the proposed pseudo-NCNTFET STI is compared with both the resistor-loaded and complementary designs (Table 7); the complementary STI has the smallest PDP_{norm} for all transitions, while the resistor-loaded designs have the largest PDP_{norm} (Table 7). Hence, both the complementary and pseudo-NCNTFET STIs are more energy efficient compared to the resistor-loaded design.

Table 7. PDP_{norm} for different transitions and designs (fJ·ps)

Design	0-->1	1-->2	0-->2	2-->1	1-->0	2-->0
Resistor-loaded (100k)	38.11	36.22	65.02	20.85	32.95	31.37
Resistor-loaded (250k)	31.00	26.82	50.97	57.38	34.79	30.24
Pseudo-NCNTFET	19.65	2.66	15.60	21.53	26.13	22.23
Complementary	9.72	2.32	0.08	6.07	1.74	0.65

5) Circuit Area

The advantage of the pseudo-NCNTFET logic is the lower circuit area compared to either complementary logic or resistor-loaded designs. For resistor-loaded designs, the requirement of large resistors needs either an off-chip or a complex circuit implementation. A complementary design requires nearly two times as many transistors as a pseudo-N design. The number of transistors is summarized in Table 8.

Table 8 Number of transistors used in different logic gates

Design	Ternary			Quaternary	
	NTI/PTI	STI	NMIN	SQI	NMIN
Complementary	2	6	10	10	16
Pseudo-NCNTFET	2	4	6	6	9

Therefore, a pseudo-NCNTFET STI has smaller power consumption, circuit area and PDP compared to a resistor-loaded design. The pseudo-NCNTFET STI offers advantages over a complementary STI with respect to circuit area, but incurring a larger static power consumption and a larger PDP.

B. PTI and NTI

In the resistor-loaded NTI and PTI designs [5] (and shown in Fig. 2(b, c)), the P-type CNTFETs are replaced with either 100KΩ or 250KΩ resistors. The voltage transfer characteristics (VTCs) of both types of NTI and PTI are shown in Fig. 16.

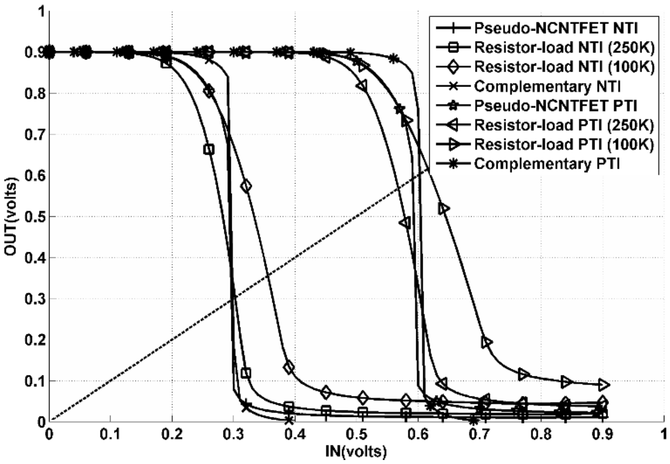


Fig. 16 Voltage transfer characteristics (VTCs) of pseudo-NCNTFET and resistor-loaded designs of NTI and PTI.

1) Static Power

Similar to the STIs, the equivalent resistance of TP1 in both the NTI and PTI circuits is simulated (Fig 17). The static power consumption at different input voltages is shown in Fig. 18; the same analysis as for the STI applies to the low static power dissipation in pseudo-NCNTFET and complementary designs.

2) Switching Power

As per (1), the switching power P consists of two components: P_c, due to the charging and discharging processes of the output capacitance, and P_s, due to the short path in switching. By (2), P_c is calculated in a similar way as for the STI. Table 8 shows the switched capacitance and transition voltage values for both NTI and PTI; P_c of the pseudo-NCNTFET design is higher than that of the resistor-loaded design, while P_c of the complementary design has the largest value.

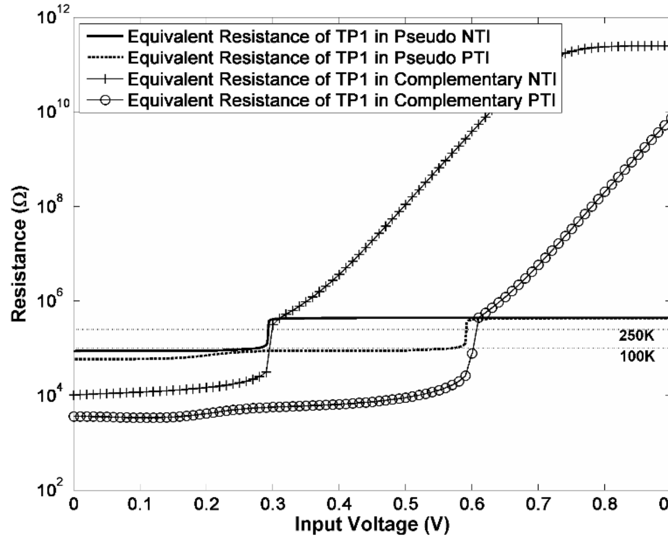


Fig. 17. Equivalent resistance of TP1 in the pseudo-NCNTFET NTI and PTI circuits.

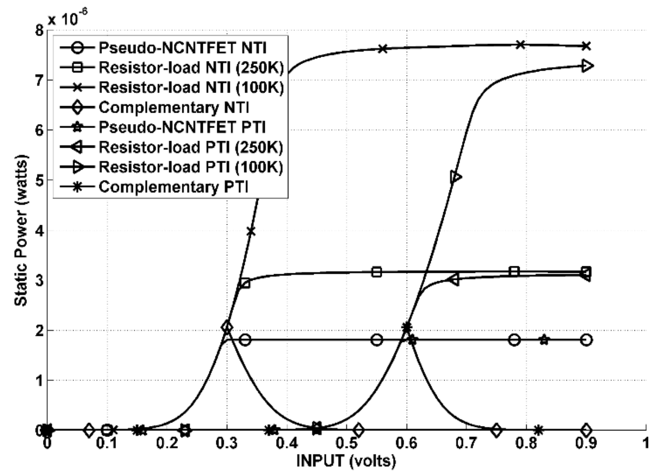
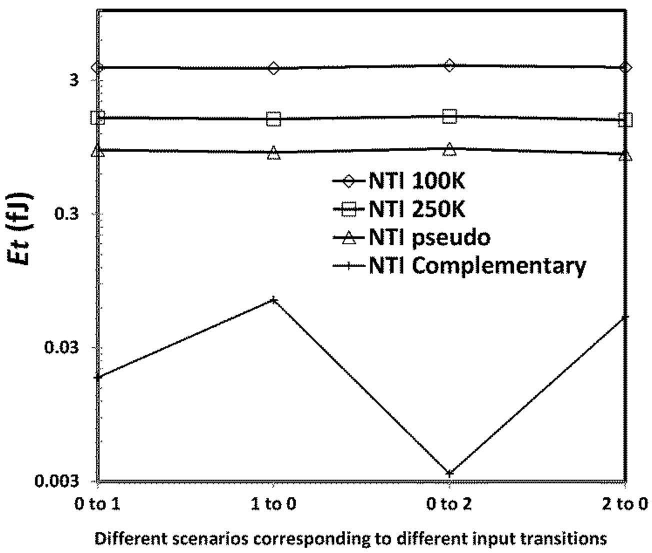


Fig. 18. Static power of pseudo-NCNTFET, complementary and resistor-loaded NTIs and PTIs.

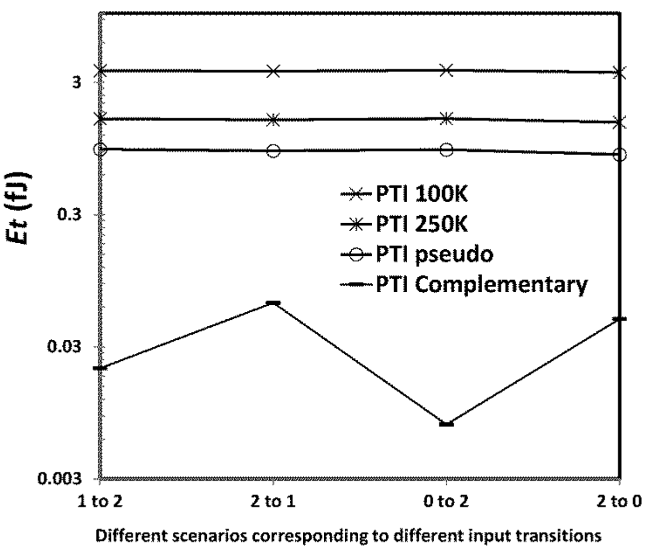
Table 9. Switching capacitance and transition voltage for PTI and NTI.

Transition Voltage (mV)			
	Pseudo-NCNTFET	Resistor-Loaded	Complementary
0-2 transition	888.9	853.3	900
Equivalent Switched Capacitance, $\boldsymbol{C_{out}}$, (aF)			
OUT	Pseudo-NCNTFET	Resistor-loaded	Complementary
2	32.6	33.2	35.6
0	3.16	3.17	21.8

Similar to the STI, the switching power dissipations of both NTI and PTI are also dominated by the short circuit power consumption P_s. The HSPICE simulation results are shown in Fig. 19. The 100K resistor-loaded implementations of both PTI and NTI have the highest switching power consumption, whereas complementary designs consume the lowest switching power.

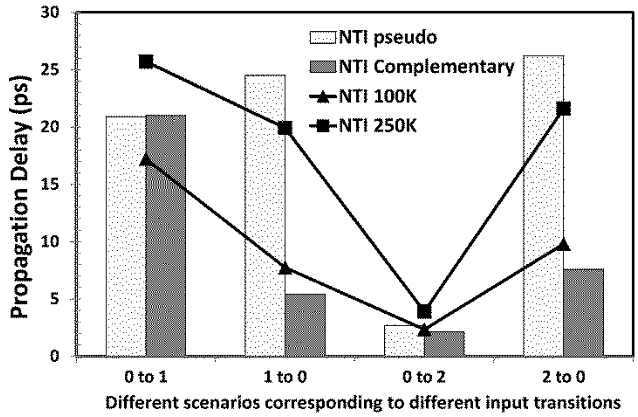


(a)

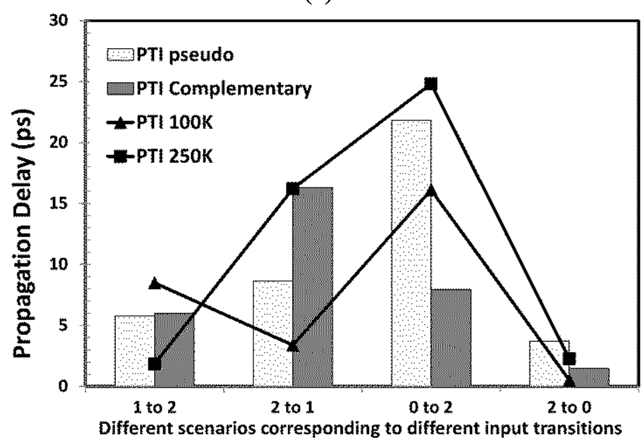


(b)

Fig. 19. Total transition energy at different transitions for (a) NTI and (b) PTI.



(a)



(b)

Fig. 20. Propagation delays of (a) NTI and (b) PTI.

3) Propagation Delay

The equivalent resistance and capacitance at the output node are simulated based on the RC model; in Table 8 there is no significant difference between the equivalent capacitances of the output nodes of the three designs, except for the case when output=0, the capacitance for the complementary design is much higher than the other two. Therefore, the propagation delay of a design is dominated by the average equivalent resistance. The RC delay can thus be calculated using Fig. 17 and Table 9. The propagation delays of both NTI and PTI are shown in Fig. 20. Similar to the STI simulation results, the delays of the pseudo-NCNTFET and complementary designs are similar on average and are between the delays of resistor-loaded designs using resistors of 100KΩ and 250KΩ.

4) Power Delay Product (PDP)

The PDP_{norm} of NTI and PTI based on the three designs are given in Table 10; similar to the previous results for STI, the complementary designs have the smallest PDP_{norm} for all transitions. The pseudo-NCNTFET designs rank the second best. This indicates that the complementary and pseudo-NCNTFET NTI and PTI are more energy efficient than the resistor-loaded designs.

Table 10. PDP_{norm} for different transitions and designs (fJ·ps)

Design	Implementation	0-->1	1-->0	0-->2	2-->0
NTI	Resistor-loaded (100k)	64.45	28.61	9.10	36.82
	Resistor-loaded (250k)	40.57	30.66	6.31	32.85
	Pseudo N-CNTFET	18.95	21.35	2.50	22.18
	Complementary	0.39	0.37	0.01	0.39
PTI	Resistor-loaded (100k)	31.24	12.30	59.80	1.78
	Resistor-loaded (250k)	2.91	25.35	39.62	3.38
	Pseudo N-CNTFET	5.39	7.86	20.25	3.16
	Complementary	0.12	1.05	0.06	0.07

C. Ternary NMIN

1) Static Power

The static power consumption is found by setting the input B at a desired value and then sweep the input A from 0 to Vdd; the simulation results of the static power consumption for both the resistor-loaded and pseudo-NCNTFET NMIN designs are shown in Fig. 21. The highest static power consumption occurs when $V_A = V_B = 0.9$V; however, the pseudo-NCNTFET NMIN consumes less static power than the other two resistor-loaded NMIN implementations (as previously detailed for the STI).

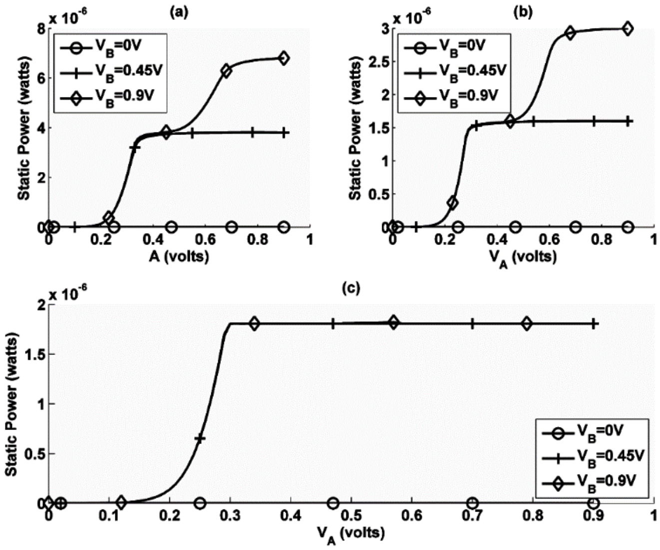


Fig. 21. Static power consumption for ternary NMIN gates. (a) Resistor-load NMIN (100K); (b) Resistor-load NMIN (250K); (c) Pseudo-NCNTFET NMIN

2) Switching Power

The worst case switching power consumption occurs when input B is at logic 2. When input B is at logic 2 (V_B=0.9V and both TN1 and TN2 are ON), V_A is swept through logic 0, 1 and 2; so, the NMIN functions as an STI with a single input A. In this case the switching power of the NMIN is similar to the STI.

3) Propagation Delay and Power-Delay Product (PDP)

For delay analysis, the worst case occurs when the output transitions from 0 to 2. The overall equivalent resistance and capacitance are used to determine the delay of the gates. As for the pseudo-NCNTFET design, the equivalent switching resistance is higher, thus the average switching delay of a pseudo-NCNTFET design is larger than the resistor-loaded design. However, the calculation of the PDP_{norm} shows that the pseudo-NCNTFET design is more efficient compared to the resistor-loaded design.

D. Quaternary Gates

Similar to the ternary logic family, the standard inverter (SQI) is analyzed for the quaternary logic family. The voltage transfer characteristics (VTCs), static power consumption, switching power consumption and propagation delay of the proposed SQI are shown in Figs. 22 - 25. The pseudo-NCNTFET SQI has a better performance in terms of power consumption and energy efficiency compared to a resistor-loaded design.

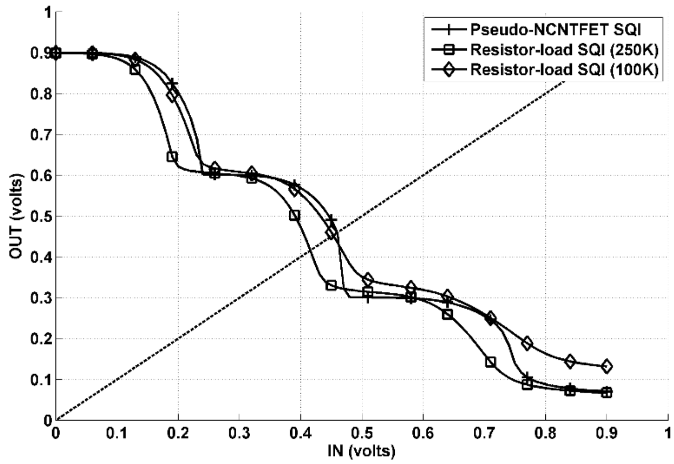


Fig. 22. Voltage transfer characteristics (VTCs) of SQIs.

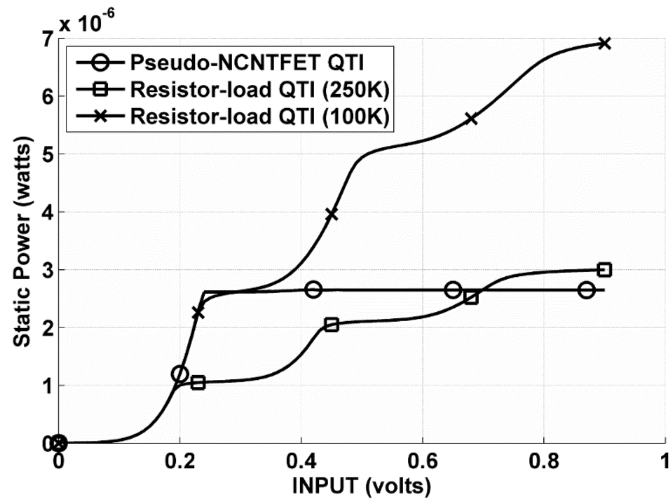


Fig. 23. Static power of SQIs.

Figs. 22 and 23 show that the quaternary design exhibit a better performance in terms of noise margin and power consumption than the resistor-loaded counterparts. Same as the ternary logic family, the P-type transistors in the pull down network play an important role to increase the SNM and reduce the static power.

As shown in Figs. 24 and 25, the pseudo-NCNTFET quaternary logic shows a very competitive delay as the 100K resistive load design and dynamic power as the 250K resistive load design. The PDP_{norm} of SQI for different transition is shown in Table 11. The proposed SQI has the smallest average PDP_{norm} value among them. Moreover, the circuit area is reduced by using the active nonlinear P-type CNT transistor, thus providing a denser implementation of the same functionality.

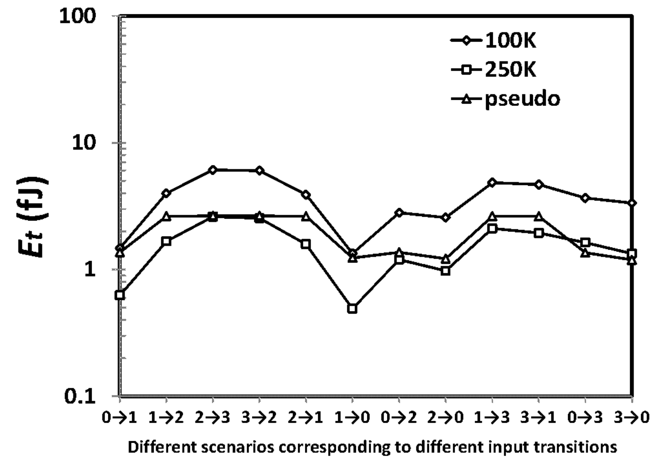


Fig. 24. Switching power of SQIs.

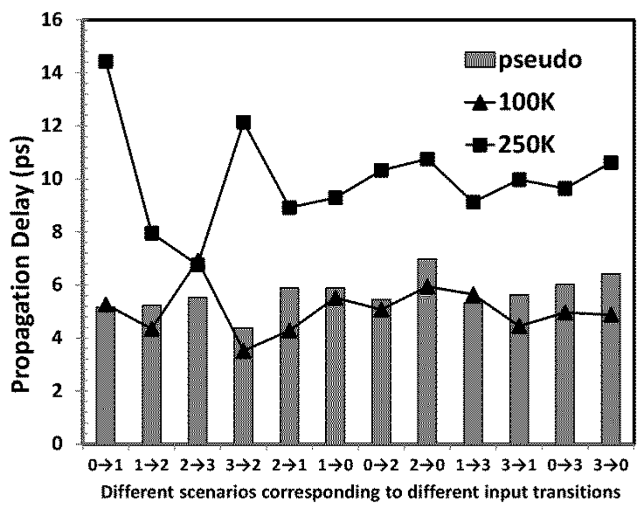


Fig. 25. Propagation delay of SQIs.

Table 11 PDP_{norm} for different transitions and designs (fJ·ps)

IN	0→1	1→2	2→3	3→2	2→1	1→0
OUT	3→2	2→1	1→0	0→1	1→2	2→3
Pseudo	6.72	13.9	14.7	11.6	15.4	8.03
250K	7.19	12.8	17.4	32.0	14.9	5.40
100K	7.26	17.0	41.8	21.4	17.1	8.08
IN	0→2	2→0	1→3	3→1	0→3	3→0
OUT	3→1	1→3	2→0	0→2	3→0	0→3
Pseudo	7.40	9.78	14.1	14.7	8.21	9.10
250K	10.7	12.8	18.1	21.1	13.7	17.4
100K	13.4	16.7	26.6	21.6	17.0	17.9

V. Impact of Multiple Tubes

For ease, only a single carbon nanotube is utilized in the P-type CNTFETs for all proposed designs as presented in previous sections. Likely, an implementation utilizes multiple tubes to address reliability and manufacturing concerns. The simulation results for a single-tube gate are still applicable to designs utilizing a proportionally scaled number of tubes. The impact of multiple tubes per CNTFET on various figures of merit (FOM) is analyzed next.

A. VTC

Similar to the width of a MOSFET, the number of tubes within a CNTFET determines its transconductance. Therefore, to retain the same driving capabilities for both the pull-up and pull-down networks, the ratio of N_{NCNT} and N_{PCNT} must be kept at a constant value, where N_{NCNT} and N_{PCNT} denote the numbers of tubes of an N-CNTFET and the always-on P-CNTFET. So for example, if the number of tubes of the P-CNTFET is increased from 1 to 10 in the STI of Fig. 4(a), then the number of tubes of the N-CNTFET must be increased from 3 to 30. As the driving capabilities of the pull-up and pull-down networks are unaffected, VTC is the same as for the single-tube case of a P-CNTFET; this condition has been validated by simulation.

B. Static Power Consumption

The static current proportionally increases when the number of tubes is increased. This result is intuitive: the equivalent resistance decreases, causing more current from the power supply, hence, this results in a higher static power consumption when the number of tubes increases. This is validated by the simulation results in Fig. 26.

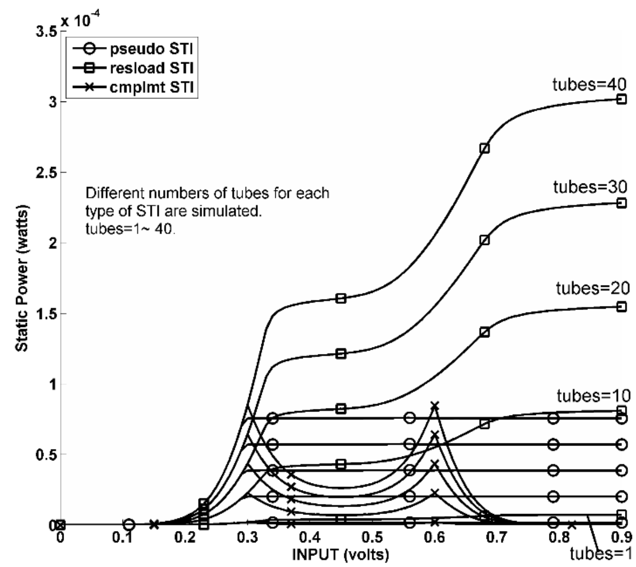


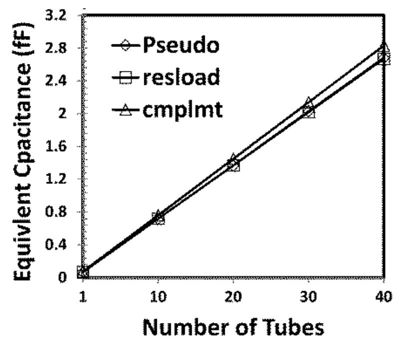
Fig. 26 Static power consumption as varying the number of tubes per transistor.

C. Delay

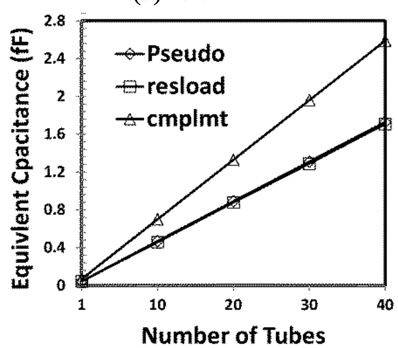
The delay is analyzed using a simplified *RC*-delay model. As previously discussed, the equivalent resistance is inversely proportional to the number of tubes. The simulation results of Fig. 27 show that the equivalent capacitance is proportional to the number of tubes. Therefore, the delay is unchanged as long as the ratio between N_{NCNT} and N_{PCNT} is constant.

D. Switching Power Consumption

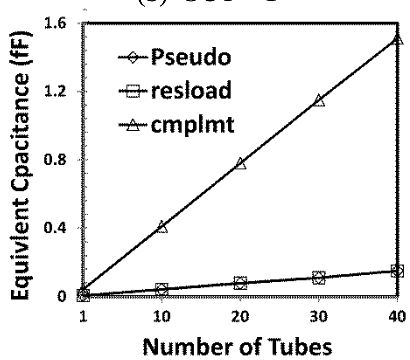
As previously discussed, the total switching energy consumption E_t is calculated using (3) and (5).



(a) OUT = 2



(b) OUT = 1



(c) OUT = 0

Fig. 27 Equivalent capacitance C_{out} as varying the number of tubes per transistor.

As the delay is unchanged (and previously analyzed in (3) and (5)), the integration interval ($t_1 \sim t_2$) stays the same as the number of tubes changes. Therefore, with a proportionally inverse (direct) increase of $R(t)$ (C_{out}), both E_s and E_c increase, thus resulting in a proportional increase of the total switching power consumption with respect to the number of tubes per transistor.

E. Power Delay Product

As analyzed in (8), the normalized PDP is determined by the product of the switching energy consumption E_t and the propagation delay t_p. As t_p is unchanged and E_t increases proportionally with the number of tubes, then PDP_{norm} proportionally increases too.

VI. Leakage Current

The proposed pseudo-NCNTFET logic family is based on ratioed logic, thus the outputs are determined by the ratio of the equivalent resistances of the pull-up network (PUN) and the pull-down network (PDN).

For an MVL gate, PDN usually consists of multiple pull down branches (PDBs) connected in parallel between the output node and ground. If the NCNTFETs in PDB are all turned on, then its always-on PCNTFET determines the equivalent resistance of the PDB. Otherwise, this PDB is turned off and its resistance is usually large due to the small leakage current. All PDB resistances (in parallel) then determine the total resistance of PDN.

Different from MOSFETs (in which the sub-threshold leakage is due to a weak inversion in the MOSFET channel), the subthreshold leakage for the CNTFETs is mostly caused by the so-called Band-to-Band Tunneling (BTBT) current [19, 20]. Usually a high threshold CNTFET (i.e. the device with low-chirality tubes) reduces leakage compared to the one with a low threshold. The drain to source voltage drop affects both the slope and the magnitude of the BTBT current. The BTBT current is significant only when a high drain to source voltage drop occurs. The subthreshold slope worsens with a larger electrostatic capacitance between the channel and substrate; therefore, for a multiple-tube design, the leakage for the CNTFETs increases when the number of tubes is increased.

Table 12 shows the simulation results of the static current of each PDB in the proposed STI and SQI for different input scenarios. The leakage currents are significantly affected by the drain-to-source voltage drop. However, the leakage currents are usually negligible, compared to the current in a turned-on PDB.

Table 12 Currents of different PDBs in STI and SQI

Pseudo-NCNTFET STI (Fig. 4 (a))				
Input	0	1	2	
Branch L	4.26pA	47.1nA	2.01μA	
Branch R	122pA	1.96μA	0.478pA	
Pseudo-NCNTFET SQI (Fig. 8 (a))				
Input	0	1	2	3
Branch L	4.25pA	8.68pA	212nA	2.94μA
Branch M	4.96pA	33.2nA	2.73μA	1.71nA
Branch R	1.56nA	2.87μA	1.6nA	0.22pA

*Note: The shaded entries show the leakage currents of the turned-off PDBs; the other entries show the currents of the turned-on PDBs. L: Left; M: Middle; R: Right.

VII. Design Methodology

A general (heuristic) methodology is outlined for designing a multiple-valued logic gate using the proposed pseudo-NCNTFET logic family; consider ternary logic.

1) Start with an always-on P-CNTFET as PDN; initially, set the number of tubes within the P-CNTFET to 1.
2) If logic 1 is ignored in the truth table, logic 0 and logic 2 can be treated as binary values; thus the standard pull-down network generation process (as for CMOS technology) can be used to generate a pseudo-NCNTFET logic gate (i.e. using logic minimization tools such as a K-map). This is a single

branch of the PDN, referred to as PDB1.
3) A second PDB2 is then generated to account for all logic 1's in the truth table. This branch is in parallel with PDB1 and is referred to as PDB2. PDB2 usually requires the use of additional always-on PCNTFETs and NCNTFETs with various chiralities.
4) Finally, the number of tubes must be scaled for different design specifications by keeping the ratio of N_{NCNT} and N_{PCNT} unchanged. As an example, if a higher yield is desired and a higher power consumption is affordable, then a larger number of tubes can be used. However, this trade-off among reliability, power and PDP must be also assessed.

Although ternary logic has been used in the above presentation, the proposed design methodology is also applicable to other multiple-valued logic by iteratively considering the PDBs.

VIII. Yield and Manufacturing Issues

A metallic CNT is one of the most dominant defects; a CNT can be either metallic (m-CNT) or semiconducting (s-CNT) depending on its chirality. Currently, there is no known technique available to grow 100% s-CNTs. The conductivity of m-CNTs cannot be controlled by the gate due to the zero or near-zero bandgap and therefore the removal of m-CNTs or m-CNT tolerance is required. Since techniques such as the selective chemical etching [21] are not perfect and cannot guarantee a robust circuit implementation, a VLSI-compatible methodology utilizing an array of redundant CNTFETs has been proposed for reliable circuit design [22]. Although this technique incurs a large area overhead, it has been shown that it is efficient in tolerating metallic-CNTs at wafer scale level in the manufacturing process flow. Therefore, it effectively enhances the yield.

Another related issue is the use of multi-chirality CNTs in the same chip. Using CNTs of multiple chiralities does not only allows for the implementation of novel logic families (as those in [5, 6, 7]), but it also brings in additional benefits. For instance, metallic CNTs with a unique chirality will result in shorted CNTFETs (as discussed previously). However, it has been shown that metallic CNTs are promising for use as energy-efficient and high-speed interconnects [23]. While the fabrication of multi-chirality CNTs is still under investigation, novel circuit and interconnect architectures could be developed by exploiting the full benefits of implementing multi-chirality CNTs into a single chip.

IX. Conclusion

This paper has presented the design and performance analysis of a new family of multiple valued logic (MVL) gates. The proposed designs, referred to as pseudo-NCNTFET MVL, replace the resistors of [5] with always-on P-type CNTFETs. The proper adjustment of the chirality and the number of CNTs in each CNTFET is then required. Therefore, the proposed approach exploits threshold voltage control of the P- and N-type transistors, while ensuring correct MVL operation for both ternary and quaternary logic gates.

The features of the pseudo-NCNTFET MVL designs are summarized as follows with respect to three sections of the structure of a gate:

- *Lower section:* the N-type transistors of the pull down network determine the logic function of a gate. The chirality of each N-type CNTFET is adjusted according to the required threshold voltage level.
- *Middle section:* the P-type transistors in the pull down network constitute the novel design scheme. The nonlinearity of the transistors ensures that a large range of values are possible and therefore the static behavior is improved. Moreover, they are utilized in the voltage divider when generating the multi-level output voltage. Thus, sizing of these transistors as determined by the chirality and number of tubes per CNTFET is very important.
- *Upper section:* the P-type transistor of the pull-up network generates the current to drive the logic gate. In addition to reducing circuit area, this P-type transistor is also part of the output voltage divider. Thus, sizing of this pull-up transistor must consider both its driving ability and the output.

Simulation results using HSPICE have been presented to assess the functionality and performance of the proposed designs. It has been shown that the pseudo-NCNTFET MVL logic family provides advantages over the resistor-loaded logic family in terms of circuit area, power consumption and energy efficiency, while still incurring a similar propagation delay. Compared to the complementary logic family, the pseudo-NCNTFET MVL logic family shows up to more than 40% reduction in circuit area with a similar propagation delay on average, albeit with a larger static power consumption and a larger power-delay product (PDP). Future work will address the reliability of the proposed MVL designs, the effects of chirality variation and the impact of metallic CNTs in the logic circuits. It is expected that these designs to be evaluated using the tool of [24] to allow different manufacturing defects to be injected at device and circuit levels.

Acknowledgment

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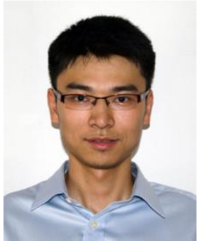

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