Robust HSPICE Modeling of a Single Electron Turnstile

Wei Wei, Jie Han and Fabrizio Lombardi

Abstract

This paper presents a novel HSPICE circuit model for designing and simulating a Single-Electron (SE) turnstile, as applicable at the nanometric feature sizes. The proposed SE model consists of two nearly similar parts whose operation is independent of each other; this disjoint feature permits the accurate and reliable modeling of the sequential transfer of electrons through the turnstile in the storage node (modeled on a voltage level basis). It therefore avoids the transient (current-based) nature of a previous model, thus ensuring robustness in simulated operation. The model has been simulated and results show that it can robustly operate at 32 and 45 nm with excellent stability in its operation. Extensive simulation results are presented to substantiate the advantages of using the proposed model with respect to changes in the circuit model parameters as related to capacitances, feature size and voltages.

Keyword

Single-electron (SE) Turnstile, HSPICE, Single electron tunneling transistor

1. Introduction

The last decade has seen the development of nanometric circuits as MOSFET-based design has moved to feature sizes well below 100 nm; CMOS technology has attained high performance and density according to Moore's Law while meeting an aggressive technology roadmap. However, concerns over short channel effects, ultrathin gate leakage, doping fluctuations, and large power dissipation have been widely reported for integrated circuits at 45 and 32 nm. So-called emerging technologies have been advocated to surmount the physical and economic barriers of current technology [1-7]. However emerging technologies have encountered only limited success; among them, single-electron devices have been attracting considerable attention for application to arithmetic and memory circuits as well as sensors. Modeling and fabrication techniques for single-electron (SE) devices have been reported [8-13]; SE transfer requires the utilization of specific devices, such as pumps and turnstiles [19]. SE pumps and turnstiles have been proposed and experimentally demonstrated by using multiple metal islands separated by metal-oxide tunnel junctions. An accurate transfer with an error rate of 10^{-8} has been achieved by using a seven-tunnel junction

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pump, so the operation frequency is still limited to the order of MHz due to the resistance of the tunnel junctions. [18] has reported an operating frequency of 166MHz. Although the operating frequency is still limited, modulated tunnel barriers have been proposed to improve performance as well as fabrication.

A HSPICE model has been presented in [21] using a charging pulse to represent the electron transfer event. However, the MOSFET-based model of [21] fails to properly simulate the operation of SE devices at nanometric scales. Therefore, a modification and improvement to this simulation model are required. The objective of this paper is to propose a new and robust model for a SE turnstile; the proposed model is HSPICE compatible and takes advantage of a nearly symmetric circuit in which each of its two parts operates almost independently. The voltage driven outcome of the model circuit avoids the transient nature of the current-driven output of a previous model [21], thus ensuring proper operation. The HSPICE model is evaluated and simulated at 32 and 45 nm because several scaling challenges have been encountered at these feature sizes [20]. Extensive simulation results are provided as assessment of the proposed model with respect to its operational and robust functionality in the presence of parameter changes. The proposed model has also been applied to simulate and assess a hybrid memory cell employing a SE transfer process [23]. This Static Random Access Memory (SRAM) cell incorporates a SE turnstile and a Single-Electron Transistor (SET)/MOS circuit in its operations [23]. The turnstile enables SE transfer in and out of the storage node and simulation has demonstrated the correct operation of this memory cell using the turnstile HSPICE model presented in this manuscript. Moreover, [23] has extensively evaluated the internal parameters of the turnstile model, showing that correct operation can still be retained under their variations.

This paper is organized as follows. Section II outlines the basic principles of a SE turnstile inclusive of the review of a previous model [21]; Section III deals with the proposed HSPICE compatible model. Section IV presents the simulation results and its comparison with experimentally found parameters (as reported in [19]). Section V outlines a comparative discussion and analysis of the results of the proposed model versus [21]. Section VI discusses the limitations of the proposed circuit model.

2. SE Turnstile

Single electron operation was demonstrated experimentally by Millikan at the beginning of the last century, however not until the late 1980's this was implemented into electronic circuits [26]. Single electron devices have been successfully implemented at nanometric scales with the development of novel fabrication techniques [27]. The so-called "orthodox" theory has played a guiding role as basis for this mode of operation due to the discreteness of single electrons [26]. The so-called Coulomb-blockade (CB) is an effect that is usually observed in a Single-Electron Transistor (SET); it is named after Charles-Augustin de Coulomb's electrical force as the effect of increased resistance occurring at a small bias voltage for at least one low-capacitance tunnel junction internally to an electronic device [25]. The SET must have a small conductive island for exploiting CB and manipulating electrons by means of a one-by-one transfer process [26]. As the current through a tunnel junction consists of a series of events, then only one electron tunnels sequentially through the barrier due to the discreteness of its electrical charge [25]. While the spontaneous tunneling at junctions is inhibited due to the high charging energy (resulting from the small total capacitance around the island), the number of electrons in the island becomes discrete under the control of the gate voltage. Therefore, the drain current changes periodically with respect to the gate voltage, showing valleys and peaks respectively at integer and half-integer numbers of electrons in the island [23].

Different from SET, the turnstile is also a type of SE devices and firstly demonstrated in [28]. The turnstile (Fig. 1) consists of multiple tunnel junctions and a central island and can pull in/out electrons using voltage signals [26]. If the gate voltage is cycled, the electrons are capable of transferring through the SE turnstile, i.e. from source to drain within one period by utilizing the CB. Therefore, CB is investigated for its potential advantages, such as low power consumption, large electrical margins and high scalability. These features make devices employing CB good candidates for memory design [19], because CB is capable of controlling the behavior in the transfer of individual electrons within a small device dimension and in the presence of statistical fluctuations [25].

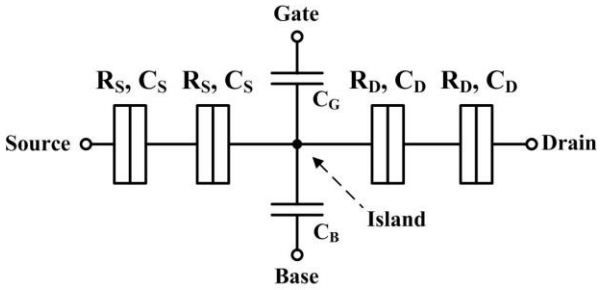

Fig. 1. Single-Electron turnstile [25]

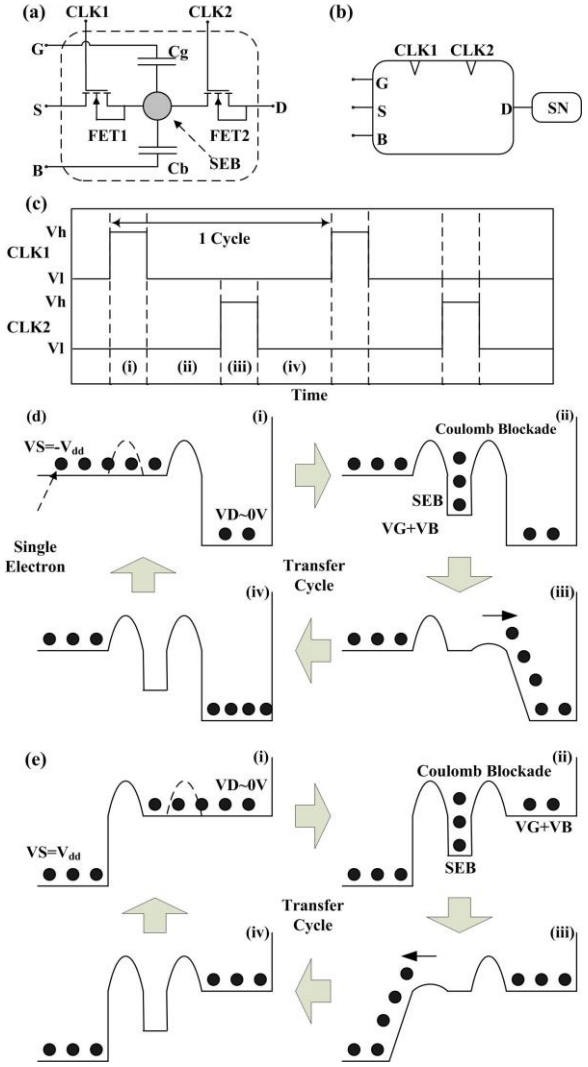

Fig. 2. (a) Equivalent circuit of the MOSFET-based SE turnstile. (b) Circuit symbol of the SE turnstile. It consists of a source terminal, a drain terminal, an input gate voltage terminal, a bias voltage terminal and two clock terminals. The drain is connected to a storage node(SN). (c) Repulsive clock voltage pulses for the turnstile operation. A transfer cycles is composed of four steps. (d) Schematic diagram to accurately inject electron into the storage node (SN). The four steps correspond to the steps in (c). (e) Schematic diagram to accurately eject electrons from the SN [21].

The MOSFET-based SE turnstile is a promising device that can accurately transfer Single Electrons (SEs) at high speed even at room temperature [14, 15, 16, 18, 19]. Its equivalent circuit is shown in Fig. 2(a). The SE turnstile consists of the following elements: a source S, a drain D, a gate voltage terminal G, a voltage terminal B, and two clock voltage terminals (CLK1 and CLK2) [21]. In the model proposed in this paper, the source is connected to a supply voltage (V_{dd} or $-V_{dd}$). The drain is connected to an electron storage node (SN). Electrons can be injected into the SN or ejected from the SN by the SE turnstile. The turnstile consists of two MOSFETs (FET1 and FET2). Single electrons are transferred from the source to the drain one by one (i.e. sequentially) by turning FET1 and FET2 ON and OFF alternately [16]. The circuit symbol shown in Fig. 2(b) is commonly used to represent the SE turnstile.

Compared with [19], an additional voltage terminal B is introduced to the circuit. Generally, terminals G and B are the upper or side gates and they control the number of electrons transferred per cycle. G and B are connected to the input voltage V_G and the bias voltage V_B, respectively. The pulse sequences for CLK1 and CLK2 to controlling the turnstile operation are shown in Fig. 2(c). Fig. 1(d) presents the process by which SEs are transferred from the source to the SN as per steps (i)-(iv) (shown in Fig. 2(c)) when the source (S) of the SE turnstile is connected to $-V_{dd}$.

The operation of the SE turnstile can be described by a *transfer cycle* made of four steps as follows. When both FET1 and FET2 are turned OFF, a single-electron-box (SEB) is electrically formed. The potential of the SEB is controlled by electrically coupling the voltages of V_G and V_B [19]. When FET1 is turned ON, the electrons enter the SEB from the source [step (i)]. After FET1 is turned OFF again, the electrons are retained in the SEB [step (ii)]. The number of electrons transferred (N) is dependent on the potential difference between the SEB and the source. At a working temperature T = 0 [21], N is given by

If $V_G+V_B \leq -V_{dd}$

$$N=0 \quad (1)$$

If $-V_{dd}<V_G+V_B$

$$N=[Cg(V_G+V_B+V_{dd})/e+1/2] \quad (2)$$

where Cg is the capacitance between the gates and the SEB, e is the electron charge [21].

The electron injection process is given as follows. When FET2 is turned ON, the SEB is connected to the SN [step (iii)]. The capacitance of SN is denoted by C_{SN} and is much larger than the capacitance of the SEB; theoretically when electrons enter the SN, the variation in voltage does not influence the behavioral model; thus, it can be neglected and for simplicity it is assumed that the voltage of the SN is always 0V. When simulating using the HSPICE model of [21] and the model proposed in this paper, voltage variations appear when representing the stored electrons. This occurs because the SN is modeled as an ideal capacitor. Hence When $V_G + V_B < 0$, the potential of the SN is lower than the SEB, resulting in all SEs flow into the SN [19]. In this case,

the number of electrons (N) transferred depends exclusively on V_G. Nevertheless, when $V_G + V_B > 0$, not all electrons flow out of the SEB; in this case, N is only determined by the potential difference between the source and the SN. Eventually after FET2 is turned OFF [step (iv)], and the transfer cycle is completed. To sum up, when the SE turnstile injects electrons into the SN, N is given by

If $V_G+V_B \leq -V_{dd}$

$$N=0 \quad (3)$$

If $-V_{dd}<V_G+V_B<0$

$$N=[Cg(V_G+V_B+V_{dd})/e+1/2] \quad (4)$$

If $V_G+V_B \geq 0$

$$N=[CgV_{dd}/e+1/2] \quad (5)$$

Correspondingly, single electrons can also be ejected from the SN, as shown in Fig. 2(e). In this case, the source of the SE turnstile is connected to V_{SS} and V_G is positive. The number of transfer electrons (N) in the SEB is dependent on the potential difference between the SEB and SN. In steps (iii) and (iv), electrons flow out of the SEB to the source. When $V_G + V_B < V_{dd}$, the voltage of the SN is lower than the SEB, and all electrons flow out of the SEB. So, N also depends on V_G. However, when $V_G + V_B > V_{dd}$, the voltage of the SN is higher than the SEB, and not all electrons flow out of the SEB, i.e. N only depends on V_{dd}. Therefore, when the SE turnstile ejects electrons from the SN, N is given by

If $V_G+V_B \leq 0$

$$N=0 \quad (6)$$

If $0<V_G+V_B<V_{dd}$

$$N=[Cg(V_G+V_B+V_{dd})/e+1/2] \quad (7)$$

If $V_G+V_B \geq V_{dd}$

$$N=[CgV_{dd}/e+1/2] \quad (8)$$

Using (5)-(8), N can be directly controlled by the gate voltage; this feature permits the SE turnstile to be used in many applications, such as multi-valued memory cells and threshold logic circuits [15] [16].

For circuit design, it is likely that the SE turnstile will be used together with CMOS devices (with compatible fabrication [19]); hence, an electrical model of its operation is highly desirable.

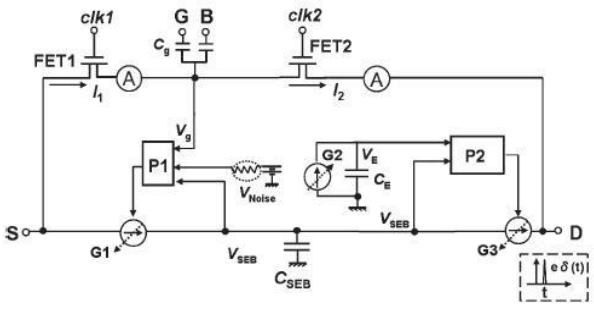

Fig. 3. HSPICE Model of a SE Turnstile [21]

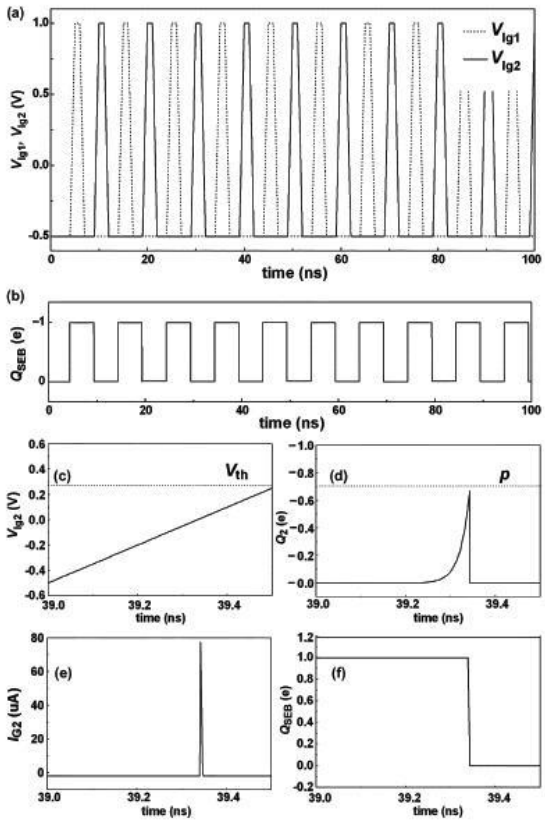

Fig. 4. Simulation of a SE turnstile using the HSPICE model of [22]. (a) Gate voltage pulses for turnstile operation. (b) Amount of charge in an ideal SEB capacitor. (c)-(f) have the same time scale. (c) FET2 is gradually turned ON. (d) Amount of charge in C2 (included in the equivalent circuit of the model) as function of time. (e) Transient current pulse appears at G2 to represent a SE transfer. (f) Charge in SEB changes back after the transfer event,

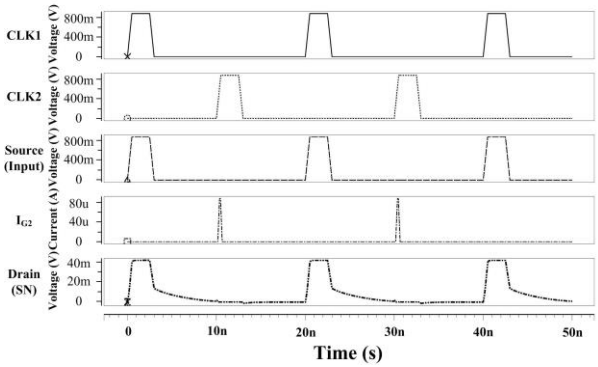

Fig. 5. Simulation of SE Turnstile using the model of [21] at 32nm

Table 1. Device Parameters for HSPICE Simulation

Feature Size		45 nm	32 nm
Temperature		26 K	26 K
Power Supply	V_{dd}	2.1 V	0.9 V
	$-V_{dd}$	-2.1 V	-0.9 V
SE turnstile	W_{FET1}, W_{FET2}	45 nm	32 nm
	L_{FET1}, L_{FET2}	45 nm	32 nm
	Vg1, Vg2	2.1 V	0.9 V
	V_h	2.1 V	0.9 V
	V_l	0 V	0 V
	C_{SEB}	0.5 aF	0.5 aF
	C_{SN}	10 aF	10 aF
	C_0	1 aF	1 aF

Although the dynamic behavior of the SE transfer process is stochastic in nature, a HSPICE model for the MOSFET-based SE turnstile has been proposed in [21] (Fig. 3). The SEB is modeled as an ideal capacitor with capacitance C_{SEB}. G1 is a voltage-controlled current mirror of I_1 and is controlled by the output of module P1. The number of electrons stored in the SEB is controlled by Vg and they are stored in C_{SEB}. With the rising edge of CLK2, the current mirror G2 (controlled by FET2), begins to charge C_E. When the charge on C_E is larger than e, then N*e/ C_E>V_{SEB} and the comparator P2 resets the charge in C_E to "0". Meanwhile, the output of comparator P2 transiently enables the voltage-controlled current source G3, such that G3 produces a sharp current pulse as output. A SE transfer event will occur. Using the current pulse for the SE transfer, G3 is transiently opened for N times until all electron flow to the drain. Fig. 4 shows the simulation result of this HSPICE model for the SE turnstile [22] and in particular shows the transient nature of [22] with respect to its current-driven mode of operation. By considering the above device operations, the dynamic behavior of the SE turnstile has been modeled and evaluated using a HSPICE simulation environment.

However, the behavioral MOSFET-based HSPICE model of [21] does not correctly model the SE transfer process at nanometric scales; the model of [21] has been simulated using the parameter listed in Table 1 with the equivalent circuit of [22] to simulate its operations at 32 nm feature size. As shown in Fig. 5; the current pulse at G2 appears when the FET2 is turned ON by the voltage pulse of CLK2. However, there is no electron accumulation at the Drain (D); hence the SE transfer operation fails when a 32 nm feature size is utilized for the MOSFETs because the voltage at the Drain is also influenced by the voltage pulse of CLK1, although its voltage variation is limited to 50 mV. Compared with the simulated results of [21, 22], the parameter values used in Table 1 have been slightly changed to account for the predictive technology model corresponding to the lower feature size of the MOSFETs [20]. The use of a predictive technology model (PTM) [24] at nanoscales allows to take into account both scalability and technology phenomena (such as process variations) that may lead to new insights in both the simulation process and the SE transfer process. Moreover, when the operating frequency is increased, this transient feature may result in an erroneous modeling of the turnstile because the SE transfer process may be affected; hence, a reliable and robust model at circuit level is required if nanometric feature sizes are utilized.

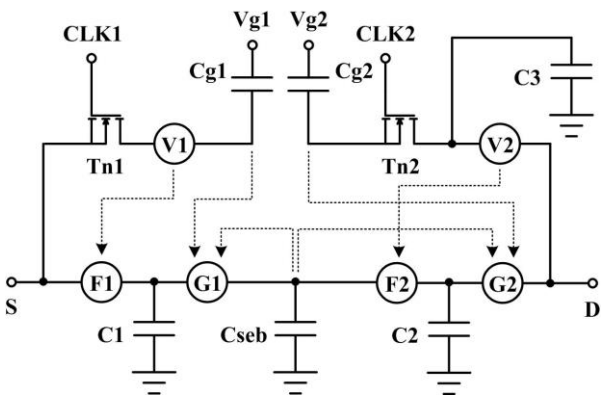

Fig. 6. Proposed HSPICE Model of a SE Turnstile

3. Proposed HSPICE Model

Fig. 6 shows the proposed HSPICE model of a SE turnstile. The goal of this circuit model is to reduce the transient effects from the input signals (source) to the output node (drain) as occurring in [21]. Its *robust nature* refers to the ability to properly model the operational behavior of the turnstile at circuit level; moreover as evidenced in later section, stability is also achieved at nanometric feature size. The SEB and the SN are modeled as ideal capacitors with capacitance C_{SEB} and C_{SN},

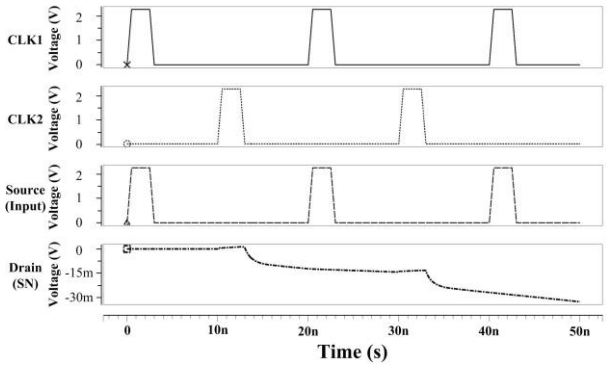

Fig. 7. Simulation Timing Diagram of SE Turnstile at 45nm

respectively. An electron transfer event is accomplished as follows: when the two transistors Tn1 and Tn2 are turned ON, two separate reference voltage nodes (Vg1 and Vg2) are utilized. There is no direct connection between the transistors, when both the input signal and CLK1 are high, the output will not experience a voltage change; therefore, the two transistors can separately control the two parts of this model.

Consider initially the left part of the proposed model; when CLK1 and the input signal are both "1", the path of the current mirror F1 is open by controlling (turning ON) the transistor Tn1. Meanwhile, an electron is transferred from the source node (S) into the SEB. Then, C_{SEB} is charged and its voltage V_{SEB} is fed back. A voltage-controlled current source G1 is then used to compare the voltage difference between V_{SEB} and Vg1. When $V_{SEB}>N*e/C_{SEB}$, the voltage-controlled current source G1 is turned OFF. Therefore, the electron that has been transferred into the SEB, is stored, i.e. it is not returned to the input source node. This is a very stable and precise process. The value of the voltage of the SEB will not decrease back to its initial value, so the equivalent charge stored in the SEB is exactly N*e. This structure can eliminate the effects of CLK1 when it changes back to "0", causing a negative current pulse in the controlling path [21]. This ensures that the robust nature of this operation in the proposed circuit-level model. Hence, as the number of single-electrons stored in the SEB (N) is controlled by Vg1, then using CLK1, N electrons are reliably stored in C_{SEB}. As for the right part of Fig. 6, a circuit similar to the left part is used in the model. The right part operates as follows. With the rise edge of CLK2, the current mirror F2 generates a current pulse from the drain to the SEB; this indicates that an electron is transferred from the SEB to the drain. Similarly, a voltage-controlled current source G2 is used for the voltage of the drain node, i.e. the voltage of the storage node (SN). All single-electrons are transferred into the SN using a series of pulses of CLK2.

The proposed model has still behavioral features; the microscopic process in steps (i) and (ii) are rather difficult to model in HSPICE. Physical modeling of the SE turnstile requires a detailed investigation of the electrical generation of the Coulomb blockade as well as the electron dynamics. This paper mostly deals with confirming the macroscopic circuit behavior; moreover from a circuit prospective, steps (i) and (ii) are not of the uttermost significance as only the transfer of the electrons in the SN is relevant at application level. Electrons are transferred into the SN when FET2 is turned ON (as corresponding to step (iii) of Fig. 2(c)), and this process is fully simulated by HSPICE, thus making the behavior of the SE to be accurately modeled by the proposed circuit.

The proposed HSPICE model for the SE turnstile has been simulated and demonstrated to successfully address most of the concerns found in the previous model [21] (Fig. 5); as shown in later sections, the evaluation of the proposed model at 45 and 32 nm, shows its robust functionality, also in the presence of variation in parameters. The significant difference in operational modes between these two models allows capturing the dynamic behavior of the SE turnstile at nanometric scales. In addition, the proposed HSPICE model has been successfully applied to a hybrid memory cell whose design has been assessed under variation of tunnel resistance and capacitance, thus further showing its robustness [23].

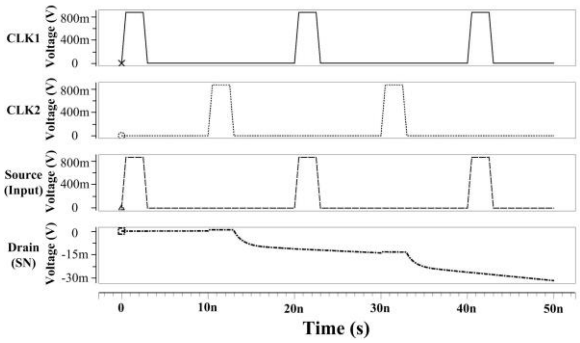

Fig. 8. Simulation Timing Diagram of SE Turnstile at 32nm

4. Simulation Results

The proposed SE turnstile model has been simulated at the feature sizes of 45 and 32 nm; Table 1 shows the values of the device parameters as applicable to the simulation of the proposed model. V_h denotes the bias voltage for CLK1 and CLK2 in Fig. 6 to control the MOSFET switching operations.

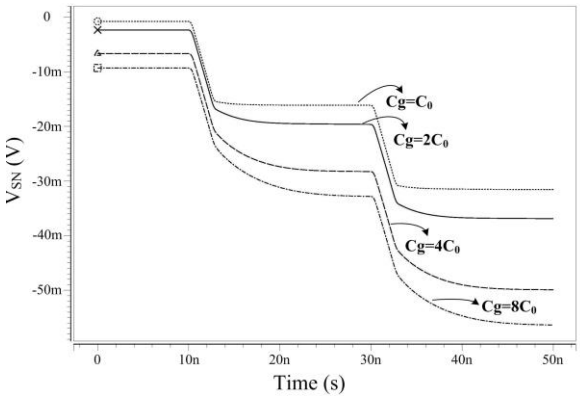

Fig. 9. Number of electrons transferred by the SE turnstile with different Cg at 32 nm with bias voltage V_h of 0.9V

The temperature is set to 26 degrees Kelvin using experimental data from the fabrication process of the SE turnstile in [19]; hence, in this paper this value is used with the parameters of Table 2. Moreover for simulation purposes, additional capacitors (C1, C2 and C3) are introduced to connect few nodes to ground; the value of 1 aF is selected for all these capacitors based on the features of the fabricated device of [19] and mitigating their influence on the simulated operation in the proposed model. Hereafter in the evaluation, the operational frequency of the turnstile has been set to 50 MHz; this value has been selected by considering the transfer rate for the correct operation of the SE turnstile [18].

Fig. 7 and 8 show the simulation results for the SE turnstile at 45 and 32 nm. Each of these figures shows the two clocks (CLK1 and CLK2) as well as the input (at the source) and the drain (SN). In both cases, the electrons transfer into the SN occurs sequentially, as shown by the decrease of the voltage level of the SN. Differently from the results in Fig. 5 for the model of [21], Fig. 8 shows that the proposed approach correctly models the electron transfer operation and the voltage change as result of the presence of electrons in the SN.

The number of electrons transferred by the SE turnstile (N) depends on the value of Cg, i.e. the capacitance between the gates and the SEB. In this paper it is assumed that $Cg/C_0=x$, where C_0=1 aF as a unit capacitance and x is a simulated defined integer parameter for the device. From Fig. 9, the voltage level can be controlled by different values of the capacitance Cg. Besides, the N transferred electrons correspond to a negative voltage level. This mechanism is given by (2) and N is linear with x.

The simulation results in Fig. 9 are average values (over four trials) for the voltage levels (linear to N) as function of time when x=1, 2, 4, 8 and V_B=0. The voltage-time function has several plateaus with a width given by the transfer cycle. The first plateau is the highest as corresponding to N=0. For example when x=2, the number of electrons transferred by the SE turnstile is two and the plateau has a negative voltage level and in each transfer cycle, two electrons are transferred into the SN through the SEB.

For a comprehensive and complete evaluation of the proposed model of the SE turnstile, the main operational modes of the circuit are assessed at 32 nm; the results are shown in Fig. 11. The circuit of a previous model [21] has also been evaluated for comparison with the proposed model; Fig. 12 and 13 show the results. In Fig. 13, the effects of having a disjoint circuit structure for the proposed HSPICE model (made of two parts) are evidenced as V_{SN} is affected only by the electron transfer process. Fig. 14 shows the simulation results to investigate the effect of different values of the input bias V_h on the output voltage of the SN. Simulation is performed at 32 nm by varying the bias voltage in the range from 0.2 V to 1.0 V. The SN voltage is significantly affected by changing the input bias voltage V_h. Differently from Fig. 14, the plot of Fig. 15 is obtained under different values for the capacitance C_{SN}, i.e. from 5 aF to 14 aF. The voltage levels corresponding to the numbers of transferred single-electrons are distinct, thus showing the effectiveness of the proposed circuit to reliably model this process. Fig. 16 shows the simulation results for the voltage of the SEB at different values for the capacitance C_{SEB}. This capacitance has been changed over a range of 0.1 aF to 0.9 aF, so inclusive of the value used in [21] for adequately evaluating the electron transfer capability. Finally, Fig. 17 shows the simulation results to simulate the performance with respect to the feature size for the MOSFET in the proposed model. In all cases, SE transfer using the turnstile is robustly modeled (as reflected in the stable signals). The simulation results plotted from Fig. 9-10 to 13-17 are obtained by utilizing the same evaluation signal pulses shown previously in Fig. 8 at 32 nm feature size.

Next using the above presented simulation results; an evaluation of the proposed model using the experimental data of [19] is pursued. Additionally, a detailed discussion of the functional operation and a comparison with [21] are also presented.

4.1 Simulation with Experimental Data

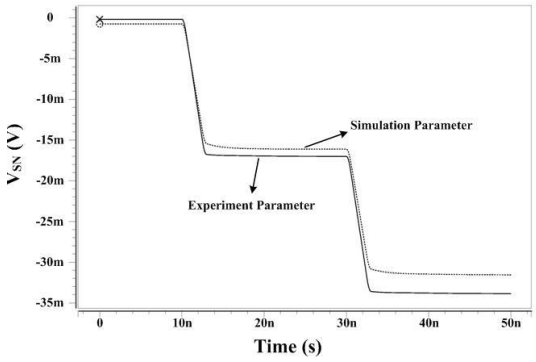

Fig. 10. Simulation results using the experimental parameters of [19]

Table 2. Device Parameters for Comparison

Feature	Parameter	Experimental Value [19]	Simulation Value
Temperature		26 K	26 K
Power Supply	V_{dd}	1 V	0.9 V
	$-V_{dd}$	1 V	-0.9 V
SE turnstile	W_{FET1}, W_{FET2}	80 nm	32 nm
	L_{FET1}, L_{FET2}	30 nm	32 nm
	Vg1, Vg2	1 V	0.9 V
	V_h	1 V	0.9 V
	V_l	0 V	0 V
	C_{SEB}	0.5 aF	0.5 aF
	C_{SN}	4 aF	10 aF

A multilevel memory using a SE turnstile has been experimentally demonstrated in [19]; the turnstile of [19] uses two one-dimensional field effect transistors (FETs) to sequentially transfer electrons into the Memory Node (MN). The MN is equivalent to the Storage Node (SN) as outlined in previous discussion. The fabricated device of [19] is patterned on a 30 nm-thick silicon-on-insulator layer, followed by a pattern-dependent-oxidation (PADOX) [19]. As per [19], the gate length and width of the MOSFETs in the fabricated turnstile are given by 30 and 80 nm, respectively. Similarly to the proposed HSPICE model, a small single-electron box (SEB) was electrically formed in the channel between the two FETs of the fabricated device at a temperature of 26K. A value of 4 aF was used for the SN capacitance in [19] at input bias and supply voltages of 1 V for both.

As part of the evaluation of the proposed model, the experimental parameters of the fabricated MOSFET-based SE turnstile (as reported in [19]) have been utilized as data. These parameters are used to compare the experimental and simulated turnstiles and are given in Table 2. Fig. 10 shows the experimental and the simulated results using the values of [19]; it shows that the proposed model can capture the SE transfer process quite accurately in terms of timing performance as well as the SN voltage. The difference in SN voltage levels between experimental and simulated results reflects a constant DC voltage that does not affect the correctness of the proposed model. This is mostly related to the difference in SN capacitance, i.e. the absolute value of the SN voltage increases by reducing the SN capacitance (in the proposed model, an ideal capacitor is used for simulating its characteristics). However, the reduced MOSFET feature size (affecting mostly the gate width) and the lower supply voltage are also contributing factors. The supply voltage affects the output voltage swing, while the lower feature size of the MOSFET affects the rate of the charging/discharging process. Also the proposed HSPICE model utilizes the switching function of the MOSFET to model the electron transfer event, so it is influenced by the difference in values.

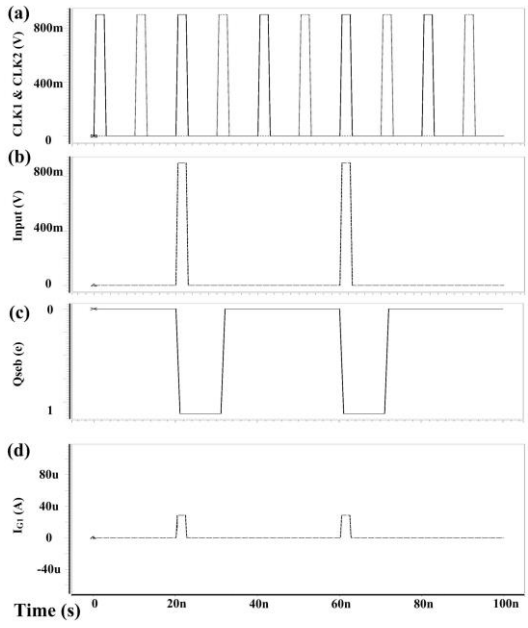

Fig. 11. Simulation results of the operational modes of the proposed model at 32 nm. (a) Applied gate voltage control pulses. (b) Input pulse to start a SE transfer cycle. (c) Amount of charge in SEB as function of cycle time. (d) Transient current through G1 for a SE transfer.

4.2 Functional Operation

To evaluate the proposed model, the modes in the proposed circuit have been analyzed with respect to the functional operation of the SE turnstile. This evaluation is shown in Fig.

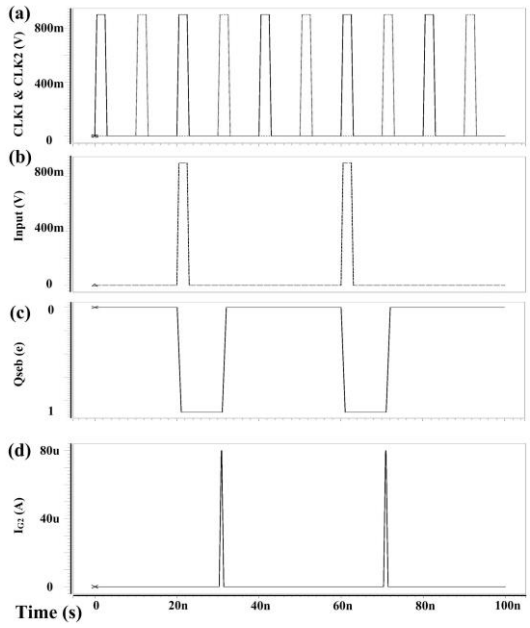

Fig. 12. Simulation results for the model of [21] at 32 nm. (a) Applied gate voltage control pulses. (b) Input pulse to start a SE transfer process. (c) Amount of charge in SEB as function of time. (d) Transient current through G2 to represent a SE transfer.

11 over two cycles for those pulses required for its operational modes, such as for the applied gate voltage control, the input for the amount of charge in the SEB and the transient current through G1 for a SE transfer.

Fig. 11(a) shows the gate voltage pulses for the turnstile at an operational frequency of 50 MHz; together with these two control pulses, an input pulse is then utilized to start the electron transfer (Fig. 11(b)). Fig. 11(c) shows the amount of charge in the SEB as function of time; this is consistent with the transfer event cycles. After a transfer event, the voltage of the SEB rises back to 0, as corresponding to the number of electrons. Therefore as expected, simulation proves that there is no electron stored in the SEB after the electron transfer. Using the same scale for the x-axis (time), Fig. 11(d) shows that when the control pulse on CLK1 is high, the voltage-controlled current source G1 is open and a transient current flows in the turnstile, leading in most cases to an electron to be transferred into the SEB. Similarly, this electron will transfer into the SN through the current source G2 when next, the voltage level of the control pulse on CLK2 becomes high.

The operational modes of the proposed HSPICE model have been implemented by simulation; based on a 50 MHz operational frequency for the SE turnstile, the inputs pulse is imposed on the source node with a longer time interval. So for example, in the first cycle for the operation of the turnstile in Fig. 11(d), the current does no change without a variation in the value of the input signal, i.e. no electron is transferred through G1. As no electron is transferred, then the SEB is still empty (Fig. 11(c)). Differently from the first cycle, when the input signal is high, the control pulse on CLK1 opens the current source G1; hence, an electron is transferred into the SEB during the second cycle. So, changes in I_{G1} and the number of electrons stored in the SEB (Fig. 11(c) and 11(d)) correctly simulate the SE transfer process. This shows that the proposed HSPICE model works correctly by utilizing the control pulses on CLK1 and CLK2 and the operation of the turnstile are modeled in the proposed model by a robust circuit-level simulation and assessment.

4.3 Comparison with [21]

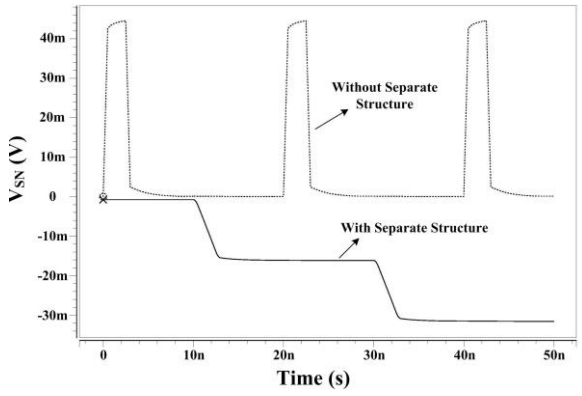

Fig. 13. Effect of single/disjoint parts in the proposed model on V_{SN} at 32 nm

A comparison is pursued with respect to [21] based on the above discussion of the operational modes of the proposed model. The simulated operation of [21] is shown in Fig. 11. Based on the simulation results the following two features are considered as part of the comparative discussion presented in this section.

4.3.1 Model Structure

A HSPICE model of the SE turnstile (Fig. 3) has been proposed in [21] with the main purpose of evaluating single-electron multiple valued memories (SEMVs) [17]. The HSPICE model proposed in this paper is shown in Fig. 6. In the proposed model, the SEB and SN are both modeled as ideal capacitors with capacitance C_{SEB} and C_{SN}, respectively. Compared to the previous HSPICE model [21], the proposed model uses a

symmetric design (made of two separate and almost identical parts) in the circuit to robustly simulate the operation of the SE turnstile. When using HSPICE, the control voltage pulses imposed on CLK1 and CLK2 require a current pulse as encountered in the model of [21]; this transient phenomenon must be carefully handled at circuit level because it may erroneously affect the electron transfer process, thus leading to an erroneous operation. The proposed model operates on a nearly disjoint operation of its two parts to mitigate interactions, i.e. each part operates separately and independently in a voltage-based mode, so there is no negative effect or coupling between each other (such as the current pulses of [22]), thus confirming the robust feature of the proposed model. The difference in circuit model structure has been evaluated in Fig. 13; the model without disjoint and separate parts (i.e. a single circuit structure) shows the voltage pulses generated from the CLK1 signal at the SN voltage. Recall that the model of [21] does not properly operate at 32 nm feature size. The proposed model utilizing two disjoint parts stabilizes the output voltage, thus modeling closely and robustly the operations of the SE turnstile.

4.3.2 Output signal

The output signal operates differently in [21] compared to the proposed model. [21] utilizes a current pulse to represent the SE transfer. When the charge on Ce is larger than e (i.e. $Ne/Ce>V_{SEB}$), the comparator P2 sets the charge on Ce to "0". On a transient basis, the output of the comparator P2 enables the voltage-controlled current source G2, such that G2 outputs a sharp current pulse. These operations are shown in Fig. 4 (taken from [22]) and Fig. 5 with the simulated results in Fig. 12.

Differently from the current pulse for representing the electron transfer process, the output of the proposed model is given by the voltage in the SN (whose level corresponds to the number of transferred electrons). As evidenced by simulation, the proposed model operates correctly in terms of logic and timing. This is in agreement with the expected output (as shown in Fig. 11(c) for the discharge event of a SEB). The model of [21] utilizes a current pulse to represent the transfer event, but current pulses occur in the circuit [22]; this phenomenon leads to a transient in the path and a pulse signal to appear in the output node. Simulation results of the proposed SE turnstile model in Fig. 7 and 8, show more stable output signals (in which the negative voltage levels of the SN corresponds to the number of electrons that have been moved sequentially through the turnstile). Again, the robust feature of the proposed model is in evidence.

5. Limitations of Proposed Model

The proposed model is affected and limited by different features as related to the circuit parameters and the operational modes evaluated in the previous section.

5.1 Clock bias voltage V_h

Fig. 14 shows the plots of the SN voltage corresponding to different clock bias voltages V_h (from 0.2 V to 1.0 V); with an increase of the bias voltage, the voltage of the SN decreases, thus also increasing the stability of the output. In Fig. 14, a small change in the voltage value appears in the output; this is mostly due to the control pulse on CLK1 (this effect is mitigated by the disjoint parts of the proposed circuit model). The changes in the output voltage are in a range of 10 microV; they can be tolerated within the operational limits of the proposed model, because the changes in the SN voltage are in the milliV scale (so with negligible effects). However, further scaling of V_h is limited, because its reduction leads to a decrease of the output voltage range. Moreover by reducing this voltage, changes on the output voltage may become significant (as evidenced in Fig. 12).

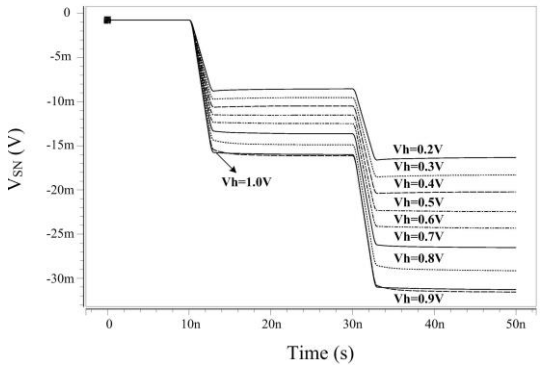

Fig. 14. V_{SN} by varying V_h at 32 nm

5.2 Capacitance C_{SN}

In this paper, the Storage Node (SN) is an essential element of the SE turnstile and is modeled as an ideal capacitor with capacitance C_{SN}. Initially, it is used to store the single-electron(s) after each transfer cycle; hence, the various levels of the SN voltage correspond to different numbers of electrons (i.e. N). Fig. 15 shows

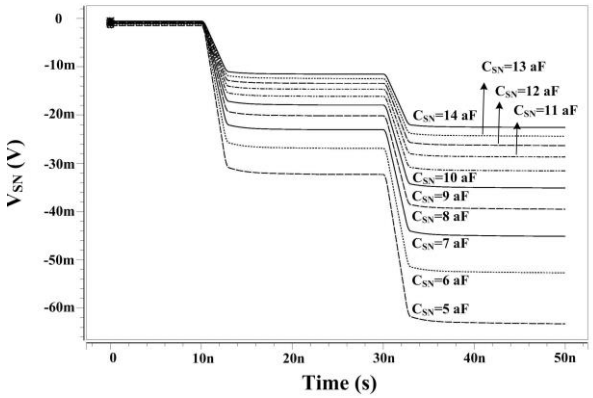

Fig. 15. V_{SN} by varying C_{SN} at 32 nm

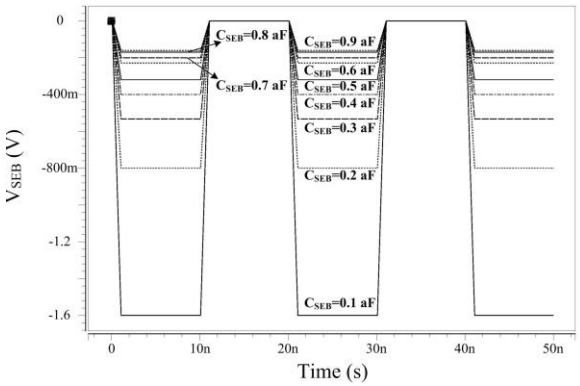

Fig. 16. V_{SEB} by varying C_{SEB} at 32 nm

the simulation results of the SN voltage caused by different values for the capacitance C_{SN} (from 5 aF to 14 aF).

In Fig. 15, the (absolute) value of the SN voltage decreases with an increase of C_{SN}; this confirms the original design objective to use voltage levels to represent the stored electron(s) according to the relation between the capacitance C_{SN} and the SN voltage V_{SN} (i.e. $Q=NC_{SN}V_{SN}$). Based on this relation and by modifying the capacitance, the voltage should have a reverse dependency when it is varied. As the SN voltage in the proposed model has been set to a negative value (as result of the charge of the electrons stored in the SN), then the value of the SN voltage V_{SN} increases by reducing C_{SN} from 5 aF to 14 aF, i.e. its absolute value correctly decreases. The variation of V_{SN} at different values of C_{SN} is plotted in Fig. 15.

5.3 Capacitance C_{SEB}

In general, the voltage of the SN changes with the input pulses of the turnstile; moreover, the value of the capacitance C_{SEB} does not influence the SN voltage, the stability of the output signals and its range. This is mostly caused by modeling the SEB and SN as ideal capacitors. While not affecting the SN, a change in the value of C_{SEB} will affect the performance of the electron transfer process, because the proposed model utilizes a voltage-controlled source as comparator to accomplish the function of monitoring the voltage in the nodes. Hence, the effect of the voltage at the SEB is further investigated.

The effects of a change in C_{SEB} are shown in Fig. 16. In this figure, the voltage V_{SEB} decreases by reducing the capacitance C_{SEB}. However, this corresponds to an increase in the absolute value of V_{SEB} in accordance with the relation in an ideal capacitor between C_{SEB} and V_{SEB} ($Q=C_{SEB}*V_{SEB}$, for a single electron transfer). So, V_{SEB} depends on C_{SEB} and by simulation, it has confirmed the correct functional operation of the SE turnstile in a transfer cycle.

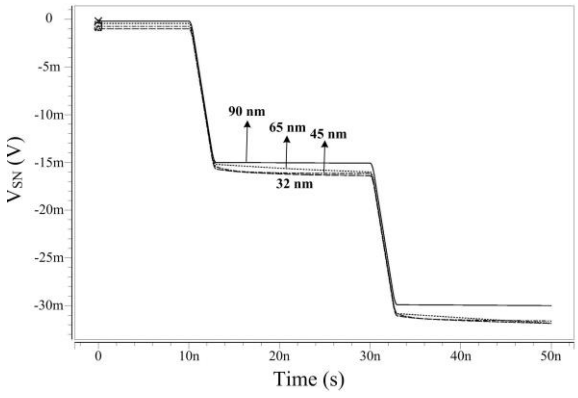

Fig. 17. V_{SN} by varying MOSFET Feature Size

5.4 MOSFET Scaling

Depending on the desired characteristics of the SE turnstile, an important component of the proposed HSPICE model is the MOSFET. As shown in Fig. 6, MOSFETs are utilized, hence the effects of scaling to smaller feature sizes must be also considered. Fig. 17 shows V_{SN} for the transfer cycle at a fixed supply voltage over a feature size range from 90 nm to 32 nm. In these cases as expected, the proposed model shows a more stable output voltage with a reduction of the MOSFET feature size. For example, during each cycle in Fig. 17, V_{SN} has a nearly constant value at 32 and 45 nm; at 90 nm, it shows that

V_{SN} has been seriously affected by the control pulses.

6. Conclusion

This paper has presented a HSPICE circuit model for a single-electron (SE) turnstile. The proposed model captures the sequential transfer of electrons through the turnstile using a nearly symmetric circuit that shows stability at nanometric feature sizes (32 and 45 nm) using a voltage level output as mode of operation. This ensures that the proposed circuit-level model is robust in its operation, so avoiding the transient (current-based) nature of a previous model [21]. It has been shown that by using experimental data (taken from [19]), the proposed model captures the single-electron transfer process with excellent accuracy.

The proposed model is HSPICE compatible and its assessment has shown that it can operate at nanometric scales, while correctly simulating the process of single-electron transfer. The proposed circuit model has been compared with [21]. It has been shown that the nearly disjoint operation of the proposed circuit model (consisting of two nearly independent parts) results in a stable output; stability has also been accomplished when changing many parameters such as capacitance, feature size and voltages. Current research deals with the utilization of the proposed model for efficiently designing novel memory architectures that exploit the SE transfer process; a preliminary evaluation of one of these memory cell designs has been presented in [23]. This hybrid cell [23] utilizes a sequential transfer of electrons by utilizing the SE turnstile for multi-value memory operation; its design has been simulated using HSPICE together with the turnstile model proposed in this paper.

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