DATE 18
DESIGN, AUTOMATION & TEST IN EUROPE
19 – 23 March, 2018 · ICC · Dresden · Germany
The European Event for Electronic
System Design & Test

Adaptive Approximation in Arithmetic Circuits: A Low-Power Unsigned Divider Design

Honglan Jiang*, Leibo Liu[†], Fabrizio Lombardi[‡] and Jie Han*
***University of Alberta, Edmonton, AB, Canada**
[†]Institute of Microelectronics, Tsinghua University, Beijing, China
[‡] Northeastern University, Boston, MA, USA

Outline

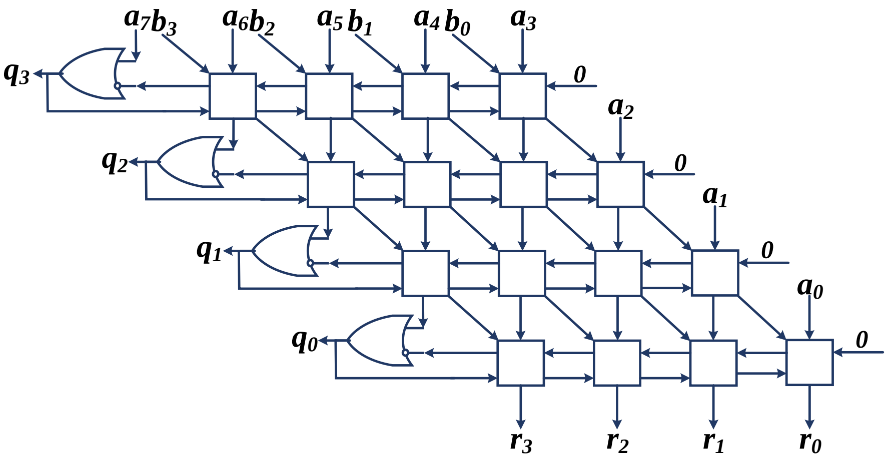
- Introduction
- Proposed Approximate Divider
- Simulation Results
    - Error Characteristics
    - Circuit Measurements
- Image Processing Applications
    - Change Detection
    - Foreground Extraction
- Conclusion

Introduction

- Precise computing is not required for many applications, e.g., image processing, clustering and recognition.
- Many approximate designs have been proposed for multiplication and addition [1].
- A **static approximation** leads to either a hardware-efficient design with a low accuracy or a very accurate design with a limited hardware saving.
- An **adaptive approximation** approach is proposed for the design of a divider.

Motivation

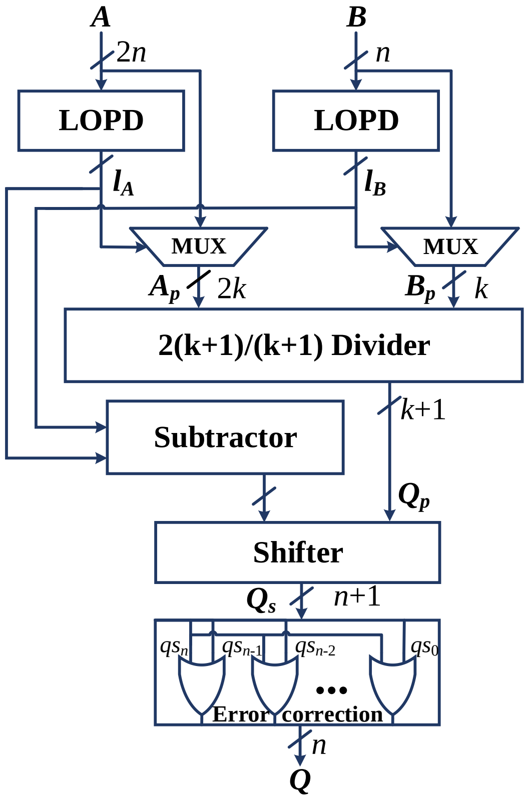
- For a 2*n*/*n* array divider, the circuit area and critical path are in **$O(n^2)$**.
- **Truncation** is an efficient approach to reducing hardware consumption for approximations in an adder or a multiplier [1,3].
- The traditional truncation results in **large relative errors**.
- The **adaptive approximation** by selectively discarding some LSBs of the inputs is proposed.



An 8/4 unsigned restoring array divider [2].

Proposed Adaptive Approximation-based Divider (AAXD)

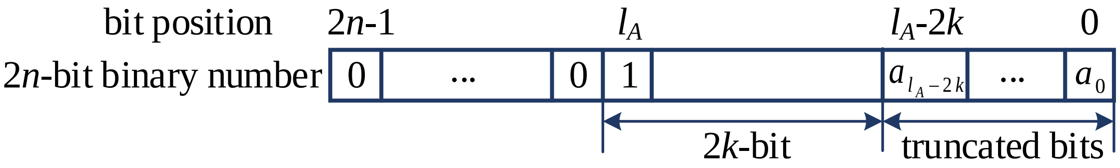
- Input are pruned using leading one position detectors (LOPD) and multiplexers (MUX).
- Using a reduced-width divider to compute the division.
- A subtractor is used to compute the number of bits needed to be shifted.
- The quotient of the reduced-width divider is shifted by a shifter.
- The error correction unit consisting of OR gates is used to recover the error caused by shifting.



Circuit structure of AAXD.

Proposed Approximate Divider -- Input Pruning (1)

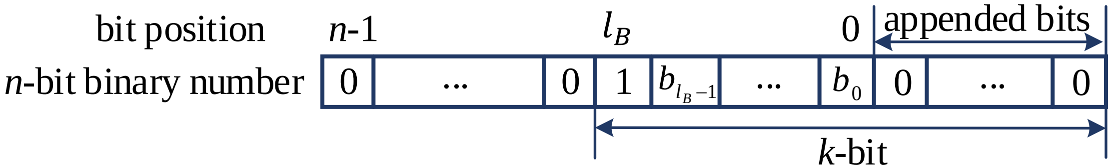
- **Case 1: $l_A \geq 2k - 1$ and $l_B \geq k - 1$**
  - 2k/k bits (A_p/B_p) are selected starting from the most significant ‘1’.
  - The redundant least significant bits (LSBs) are truncated.
  - The largest quotient of $\frac{A_p}{B_p}$ is $\left\lfloor \frac{2^{2k}-1}{2^{k-1}} \right\rfloor = 2^{k+1} - 1$.
  - A 2(k+1)/(k+1) divider is used to compute the division of A_p/B_p.
  - A/B is obtained by left shifting A_p/B_p for $(l_A - l_B - k)$ bits.



Pruning scheme for a 2n-bit unsigned number A when $l_A \geq 2k - 1$ [4].

Proposed Approximate Divider -- Input Pruning (2)

- **Case 2: $\boldsymbol{l_A \geq 2k-1}$ and $\boldsymbol{l_B < k-1}$**
  - 2k/k bits are selected starting from the most significant ‘1’, A_p/B_p.
  - Zeros are appended to the LSBs of B_p.
  - A 2(k+1)/(k+1) divider is used to compute the division of A_p/B_p.
  - A/B is obtained by left shifting A_p/B_p for $(l_A - l_B - k)$ bits.



Pruning scheme for a n-bit unsigned number B when $l_B < 2k-1$.

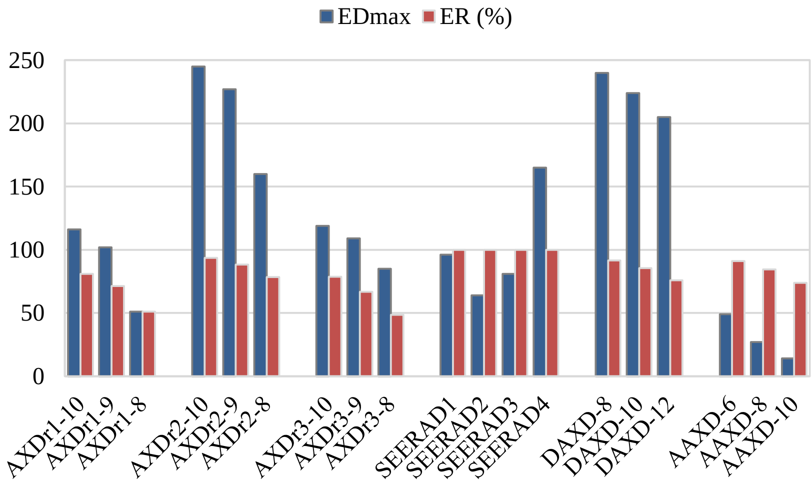
Proposed Approximate Divider -- Input Pruning (3)

- **Case 3: $\boldsymbol{l_A < 2k - 1}$ and $\boldsymbol{l_B \geq k - 1}$**
  - When the dividend A is zero, l_A is set to 0 (i.e., with the same leading one position as number $(0 \cdots 01)_2$)

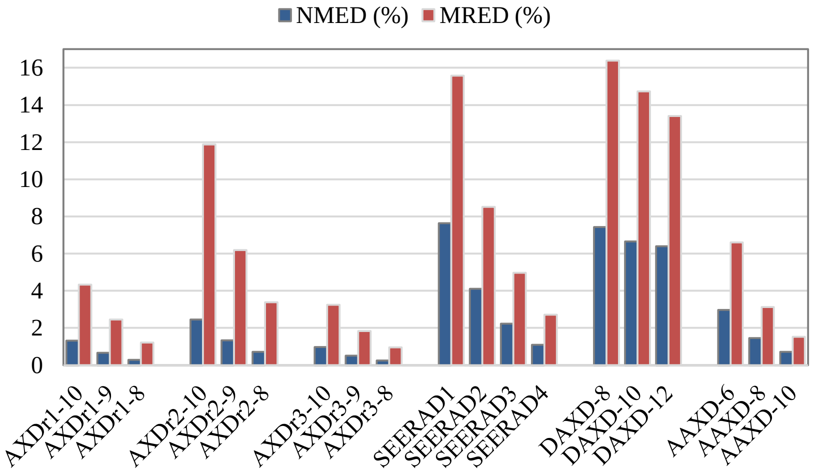
- **Case 4: $\boldsymbol{l_A < 2k - 1}$ and $\boldsymbol{l_B < k - 1}$**
  - An accurate 2n/n division is performed by using a 2(k+1)/(k+1) divider.
  - A/B is obtained by left shifting A_p/B_p for $(l_A - l_B - k)$ bits.

Simulation Results -- Error Characteristics

- Smallest maximum error distance, ED_{max}
- Relatively smaller error rate, ER
- Moderate NMED and MRED



ED_{max} and ER of approximate 16/8 dividers.

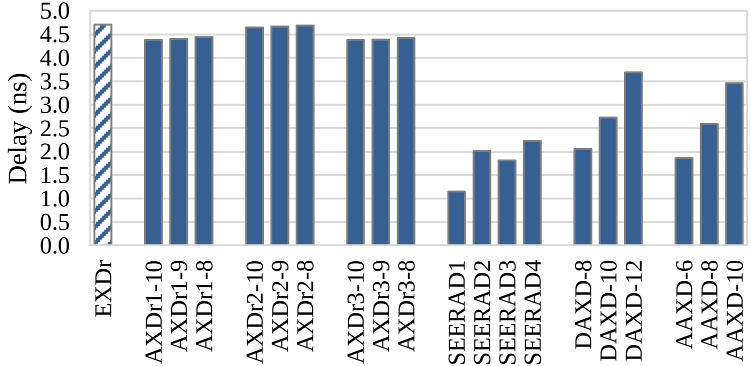


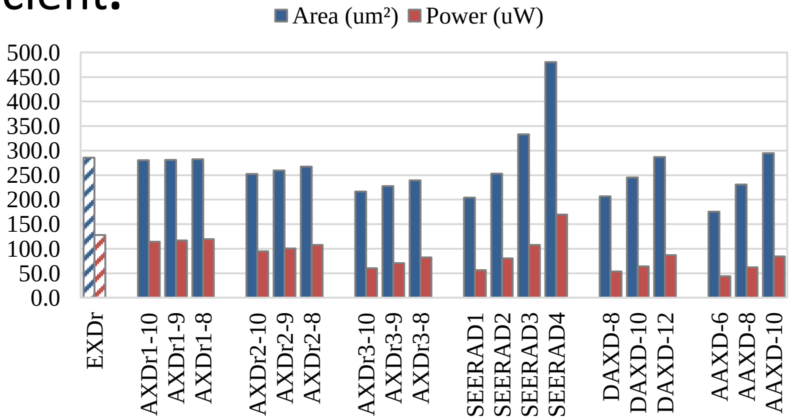
NMED and MRED of approximate 16/8 dividers.

NMED: the mean value of the error distances normalized by the maximum possible accurate output.
MRED: the mean value of the relative error distance.

Simulation Results -- Circuit Measurements

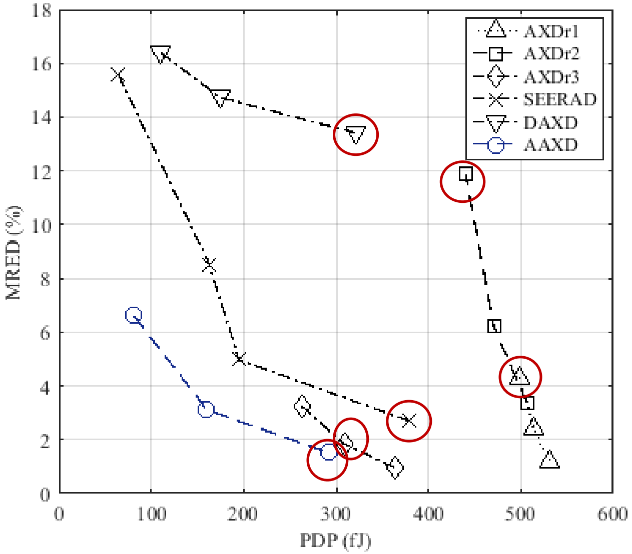
- **Compared to the exact design, EXDr**
  - 27%-61% improvement in critical path delay
  - 34-66% reduction in power dissipation
  - 52%-86% improvement in power-delay product (PDP)
- **Compared to the other approximate dividers**
  - AAXD is faster and more power-efficient.





Simulation Results -- Discussion

- The MRED and PDP are selected as representatives to show the error and circuit characteristics.
- The proposed AAXD has a much **smaller value of MRED** than the other approximate designs when a similar PDP is considered.

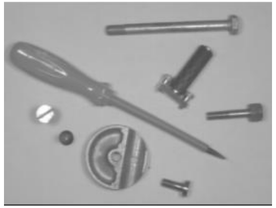


A comparison of approximate dividers in PDP and MRED.

Image Processing Applications -- Change Detection

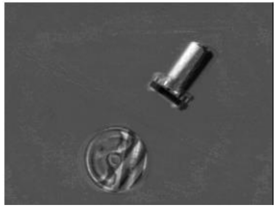
- AAXD-10 and AXDr3-9 perform similarly well as an accurate divider.

- AXDr2-10 and DAXD-12 produce results with a low quality.

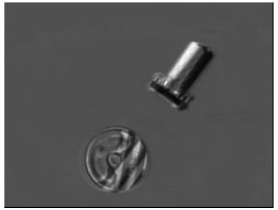

Input image 1

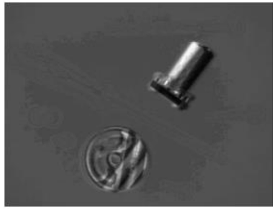

Input image 2


Accurate output


AXDr1-10 (32.14 dB)


AXDr2-10 (18.39 dB)

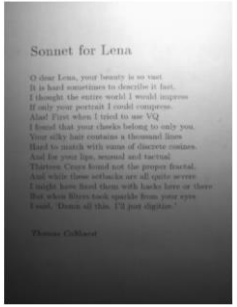

AXDr3-9 (39.27 dB)


SEERAD-4 (36.61 dB)

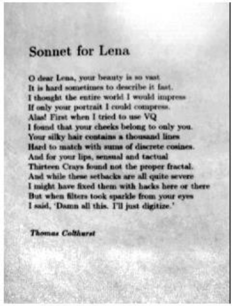

DAXD-12 (23.56 dB)

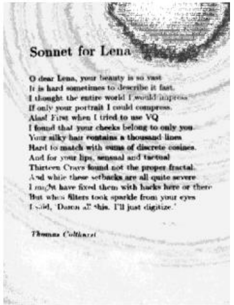

AAXD-10 (40.16 dB)

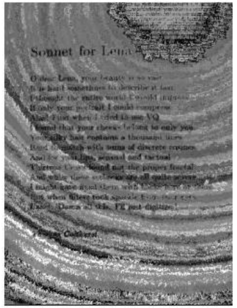
Image Processing Applications -- Foreground Extraction

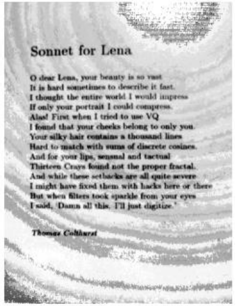

Illuminated image

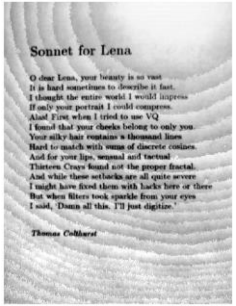

Background

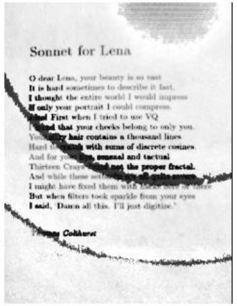

Accurate output

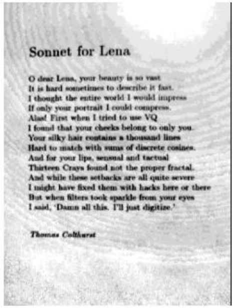

AXDr1-10 (15.00 dB)


AXDr2-10
(8.19 dB)


AXDr3-9
(18.80 dB)


SEERAD-4
(23.46 dB)


DAXD-12
(14.42 dB)


AAXD-10
(26.42 dB)

Conclusion

- An approximate unsigned divider using adaptive approximation is proposed.
- A novel pruning scheme and error correction circuits are utilized for the divider to attain a high accuracy.
- The proposed design is very power-efficient with a high-performance.
- With a similar PDP, the proposed design is **more accurate** than the other approximate dividers.
- The proposed divider **outperforms** the other approximate designs in image processing.

References

[1] H. Jiang, C. Liu, L. Liu, F. Lombardi, and J. Han, “A review, classification, and comparative evaluation of approximate arithmetic circuits,” ACM JETC, vol. 13, no. 4, p. 60, 2017.

[2] B. Parhami, Computer arithmetic. Oxford university press, 2000.

[3] B. Barrois, O. Sentieys, and D. Menard, “The hidden cost of functional approximation against careful data sizing–A case study,” in DATE, pp. 181–186, 2017.

[4] S. Hashemi, R. Bahar, and S. Reda, “A low-power dynamic divider for approximate applications,” in DAC, 2016.

[5] L. Chen, J. Han, W. Liu, and F. Lombardi, “Design of approximate unsigned integer non-restoring divider for inexact computing,” in GLSVLSI, pp. 51–56, 2015.

[6] L. Chen, J. Han, W. Liu, and F. Lombardi, “On the design of approximate restoring dividers for error-tolerant applications,” IEEE Transactions on Computers, vol. 65, no. 8, pp. 2522–2533, 2016.

[7] R. Zendegani, M. Kamal, A. Fayyazi, A. Afzali-Kusha, S. Safari, and M. Pedram, “SEERAD: a high speed yet energy-efficient rounding-based approximate divider,” in DATE, pp. 1481–1484, 2016.

Thanks for your attention.