On the non-volatile performance of Flip-Flop/SRAM cells with a single MTJ

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***Abstract*—In this paper, three non-volatile flip-flop (NVFF) /SRAM cells that utilize a single MTJ (magnetic tunneling junction) as non-volatile resistive element are proposed. These cells have the same core (i.e. 6T) but they employs different numbers of MOSFETs to implement the so-called 'instantly on, normally off' mode of operation. The additional transistors are utilized for the restore operation to ensure that the data stored in the non-volatile circuitry can be written back into the flip-flop core once the power is made available. These three cells (7T, 9T and 11T) are extensively analyzed in terms of their operations in 32nm technology, such as operational delays (for the write, read and restore operations), the static noise margin (SNM), critical charge and process variations (in both the MOSFETs and the resistive element). Simulation results show that an increase in the number of MOSFETs in the cells causes improvements in critical charge and tolerance to process variations at the expense of an increase in power dissipation. The SNM and the delay of the restore operation however do not necessarily increase with the number of MOSFETs in the cell, but rather on the control of access to the storage nodes from the single MTJ.**

***Index Terms*— Non-volatile Flip-flop, magnetic tunneling junction, SRAM, resistive switching**

I. Introduction

The decrease of supply and threshold voltages with MOSFET dimensions had led to a very large increase in subthreshold leakage; hence, leakage power is rapidly becoming a substantial component of the total power dissipation of a circuit [1]. Hence, leakage power has become a challenge for achieving low power operation in many critical systems.

Power gating has been advocated as one of the possible solutions; in this technique, inactive blocks are turned off by adding a high threshold device (often known as the "sleep" transistor) between the power supply and the operational circuit. This scheme is efficient for reducing the leakage power when a large functional block is in a sleep state [2]. However, part of the block may still need to be powered on due to the often volatile nature of the retention registers. A nonvolatile version provides a solution to retain the states of the registers, thus the whole block can be fully powered off during the sleep mode. Moreover, if the functional blocks are clock-synchronized [3], non-volatile operation of the SRAM cells and flip-flops (FFs) ensure consistency.

Gating techniques using MTJ-based (magnetic tunneling junction) non-volatile circuits (such as flip flops) have been proposed in [4] to further decrease the static power. When the processor is in an idle state, the data is stored in the MTJ-based non-volatile circuits and the power supply is cut off to stop the leakage current. However, both the energy and the time for storing data into the MTJs are significantly larger than for a MOSFET-based SRAM; moreover, the power dissipation of these non-volatile circuits unfortunately increases at high frequencies compared with the corresponding volatile circuits, thus causing a decrease in performance of the processor.

In this paper, three memory cells that utilize a single MTJ as non-volatile resistive element are proposed. These cells have different numbers of MOSFETs to implement the so-called 'instantly on, normally off' mode of operation [5].Under this mode, a sequence of operations must be performed; the data is initially written in both the CMOS volatile part and the MTJ based non-volatile part. Once the data is written to both the volatile and the non-volatile storage, the memory is powered down (i.e. by shutting down the power supply). When the power is reestablished, the stored data is written from the MTJ-based non-volatile circuit to the CMOS. The proposed non-volatile cells are assessed in terms of different figures of merit for performance (restore as well as read/write), stability (the Static Noise Margin, SNM) and tolerance to a single event upset (critical charge) and process variations. Simulation results show that an increase in the number of MOSFETs in the memory cells causes improvements in critical charge and tolerance to process variations at the expense of an increase in power dissipation. The SNM and the delay of the restore operation however do not necessarily increase with the number of MOSFETs in the cell but rather on the control of access to the storage nodes from the single MTJ.

II. Review

A. Magnetic Tunneling Junction (MTJ)

The MTJ is a device made of two ferromagnets separated by a thin insulator. If the insulating layer is thin (typically a few nanometers), electrons can tunnel from one ferromagnet into the other [5]. The direction of the magnetizations of the ferromagnetic films can be switched individually by an external magnetic field; if the magnetizations are in a parallel orientation it is more likely that electrons will tunnel through the insulating film than if they are in the opposite (antiparallel)

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orientation. This junction can be switched between two states of electrical resistance (one with low and one with very high values), hence binary storage is accomplished [6]. The resistance of the MTJ depends on the relative orientation of the magnetization directions of the two ferromagnetic layers due to the spin-dependent tunneling involved in the electron transport process between the majority and minority spin states. The switching operations of a MTJ can be implemented by utilizing three distinct methods: Field Induced Magnetic Switching (FIMS), Thermally Assisted Switching (TAS) and Spin transfer Torque (STT). FIMS utilizes two perpendicular currents passing above or below the MTJ to generate a magnetic field and change the magnetization direction. TAS uses also two currents for the switching operations; one current passes through the MTJ and heats the storage layer for switching the magnetic field generated by the other current. STT exploits the spin-magnetization interaction and requires a low current passing through the MTJ to switch the magnetization of the storage layer. The change in the resistance of the MTJ is measured by the so-called TMR ratio, this is defined as $\Delta R/R = (R_{high} - R_{low})/R_{low}$. Using a MgO oxide barrier, the TMR ratio is in a range of 70% to 500% at room temperature and 1010% at 5K [7]. However, a range of 70% to 200% has been reported recently for the TMR ratio of MTJ-based memories [8][9]. In this paper, a FIMS-based MTJ is employed, because this device does not use a passing current to program it, so in a NVFF both the CMOS part and the MTJ can be written simultaneously. A TMR ratio of 150% (i.e. a middle range value [8] [9]) is utilized for the MTJ, while the 32nm HP Predictive Technology Model (PTM) is used for the CMOS transistors at minimum size. As for area, the MTJs are placed on a different plane than the MOSFETs (using stacking). [8] has reported a MTJ of 100nm dimension and with an area of $0.02\mu m^2$. A 6T cell requires an area of $0.146\mu m^2$ at 32 nm feature size [10]. Hence, the 6T has a larger area and therefore it is the limiting factor in the density of a NVFF.

B. Previous Design

[5] has proposed a memory cell in which two RRAMs are employed as resistive elements (Figure 1).

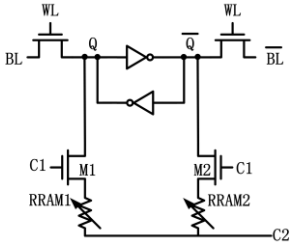

Figure 1. 8T2R cell of [5]

The cell of [5] is an 8T2R NVSRAM cell because it needs 8 MOSFETs in a complementary scheme (a conventional 6T SRAM is used as memory core). The two resistive elements are connected to the two data nodes of the SRAM cell through two control transistors (M1 and M2) and are programmed according to the data stored in the SRAM cell. The two elements are always in different resistive states, i.e. when one is in High (Low) state, the other is in Low (High) state.

- During power down, the SRAM loses the stored data, but the two resistive elements store the data due to their non-volatile nature.
- When the power turns on, the data is written back to the SRAM according to the resistance state of the two RRAMs.

This cell has a complementary structure, so it operates on both storage nodes of the SRAM core, i.e. RRAM1 and RRAM2 are connected to Q and $\overline{Q}$ respectively, each with a transistor as an access device. The resistance range between the SET and RESET state is large, so during the restore operation the difference in voltage drops across RRAM1 and RRAM2 is large too and this can be used to improve the corresponding SNM for stability purposes; however, if a MTJ is used as resistive element, the resistance range is not sufficiently large. So in the restore operation, the voltage difference between Q and $\overline{Q}$ is relatively small. The restored values of Q and $\overline{Q}$ are 419mV and 399mV respectively during the restore '1' operation at 32nm feature size; they are very close and therefore, the cell is susceptible even to a small amount of noise to change in stored data.

III. PROPOSED NVFF/SRAM CELLS

The cell of [5] employs two MTJ to implement the restore operation; however, a MTJ consumes more power than a MOSFET. So, in this section, different cells that utilize only a single MTJ as non-volatile element connected to the 6T core are proposed; these cells differ in the number of MOSFETS used in their circuits. Circuit complexity (in terms of the number of MOSFETs) as well as other operational features and metrics are also addressed. In this section, the operations of the two cells are presented and simulated. The MTJ in this paper has R_{high}=12.5kΩ; R_{low}=5kΩ, while the MTJ model proposed in [11] is employed. The programing circuit for the MTJ is not shown in Figure 2; the interested reader should refer to [9] for more detail on this circuit.

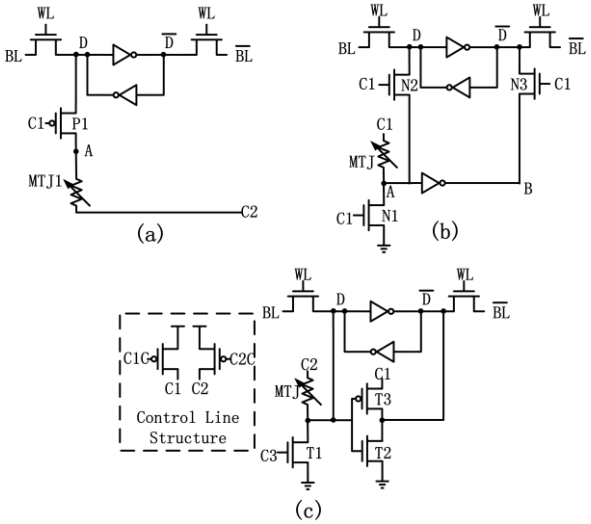

Figure 2. Proposed NVFF/SRAM (a) 7T1R cell; (b) 11T1R cell; (c) 9T1R cell;

A. **7T1R.** As discussed in a previous section, the MTJ-based 8T2R cell is not very robust. The cell shown in Figure 2(a) is proposed as modification to [5].This cell employs a 6T core; a

single MTJ is connected to Q through a control transistor P1, hence this cell is a 7T1R scheme. Similar to the 8T2R structure, the 6T forms the basic storage circuit and the MTJ is used to keep the data during power-off. The MTJ is programmed properly according to the data stored in the 6T. When the power turns on again, the data can be written back to the SRAM through P1. The operation principles of this cell are similar to the previous cell; however, it has two significant differences.

- The power-on operation is executed earlier than the restore operation. The reason is that if the restore operation occurs prior to the power-on operation, then node Q is changed irrespective of the resistance value of the MTJ. Hence, the voltage value of Q must be higher than $\overline{Q}$ before the power-on operation. Once the power-on operation starts, then Q is pulled to '1' irrespective of the previously stored value in the cell.
- During the restore operation, P1 is turned on simultaneously with the supply Vdd, C2 is then applied for a short time (1ns in this case). The goal of the new scheme is to have $\overline{Q}$ to be high following the supply Vdd. In the current scheme, Q or $\overline{Q}$ is high randomly during the power-on operation, because both Q and $\overline{Q}$ are fixed to '0' prior to it. This may cause a malfunction to occur when Q is pulled high during the restore '0' operation. In this case, when C2 is applied, both Q and C2 are high at the same time. This causes no voltage difference between these two nodes and the restore operation may not correctly execute. In the new scheme, $\overline{Q}$ is high every time the power is reestablished. When restoring a '0', the high resistance of the MTJ prevents the value of Q to change to a '1' while keeping $\overline{Q}$ at '0'.When restoring a '1', the low resistance of a MTJ makes Q to change to a '1' and drive $\overline{Q}$ to '0'.

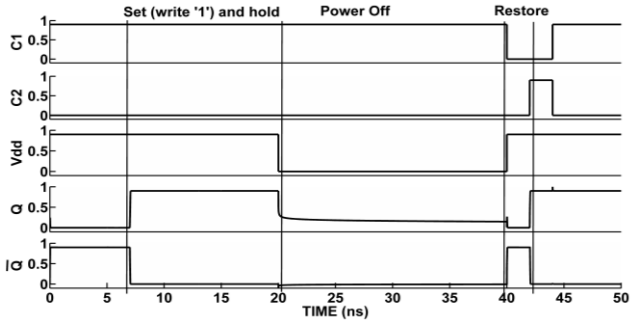

Figure 3. Simulation of proposed NVFF/SRAM 7T1R cell; timing diagrams of C1, C2, Vdd, Q and $\overline{Q}$ for the restore '1' and power-on operations

Figure 3 shows the restore '1' and power-on operations of the 7T1R cell.

1. During the first 7ns, the cell is in the initial state, i.e. Q is '0' and $\overline{Q}$ is '1'. C1 is high to turn off P1.
2. At 7ns, CLK is applied (not shown in the timing diagrams) to access the 6T core. Thus, a '1' is written into Q and $\overline{Q}$ is '0'. This is the same as the write operation of a 6T SRAM; so, the MTJ stores the value of the 6T cell.
3. From 20ns to 40ns, the power supply is removed. Both Q and $\overline{Q}$ are '0'.
4. At 40ns, the supply is reestablished and C1 drops to '0' to turn P1 on. C2 is still '0'; so, Q is connected to C2 and is '0'. Thus, $\overline{Q}$ changes its state
5. At 42ns, C2 is high. Since the MTJ is in the low resistance state, the voltage drop across the MTJ and P1 is relatively small to drive Q to '1'. Therefore, $\overline{Q}$ is also changed.
6. After 44ns, all control signals (C1 and C2) are removed. The cell successfully restores a '1'.

B. **11T1R.** As discussed previously, a cell with a single-side restore operation may incur in a problem during the restore '0' operation; in this case, Q cannot be pulled to a low value. To address this problem, a complementary scheme is designed next, in which both storage sides of the CMOS core are used. Consider the TMR ratio of a MTJ; this is significantly smaller than for an Oxide based RRAM, so the scheme of [5] cannot be used. However, the MTJ is a four-port resistive device in which the programming and the evaluating ports are separate. This feature is used next for a new design of a complementary cell. This cell requires a larger number of MOSFETs, i.e. it is an 11T1R cell.

As shown in Figure 2(b), the MTJ and N1 make a 1T1R MTJ in which the value written in the MTJ is based on the data stored in the 6T core. When the power is off, the data in the 6T core is lost, while the MTJ retains such data. When the power is reestablished, the value stored in the MTJ determines the node (either A or B) that has the highest voltage value. The 6T core can be restored by the difference in these voltage values. The main operational principles of the 11T1R cell are similar to the 8T2R cell; moreover, the 11T1R cell causes the voltage difference between A and B to increase, thus making its operation more robust than in previous schemes. Figure 4 shows the timing diagrams for the restore '1' operation.

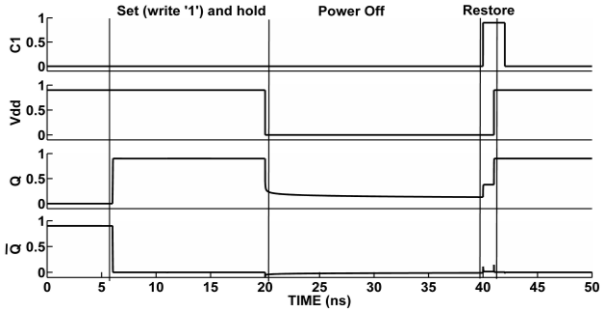

Figure 4. Simulation of proposed NVFF/SRAM 11T1R cell; timing diagrams of C1, Vdd, Q and $\overline{Q}$ for the restore '1' and power-on operations

(1) During the first 6ns, the cell is in the initial state; so, Q is '0' and $\overline{Q}$ is '1'. All other signals are not applied. (2) At 6ns, CLK is applied (not shown in the timing diagrams) to access the 6T core. Thus, a '1' is written into Q and $\overline{Q}$ is '0'. It is the same as a 6T SRAM write operation. So, the MTJ stores the value of the 6T core. (3) From 20ns, the power supply is shut down. Both Q and $\overline{Q}$ change. (4) From 39ns to 40ns, C1 is high. N2 and N3 are turned on. The voltage at A is higher than at B because the MTJ is in the low resistance state. Q is at 0.38V. (5) From 40ns, the power is supplied again; Q is much higher than $\overline{Q}$, i.e. Q is '1'. $\overline{Q}$ is '0'. (6) After 41ns, C1 is deactivated; the 6T core has successfully executed the restore '1' operation.

C. **9T1R.** In the 11T1R cell, the two transistors N2 and N3 are used to isolate the 6T core from the operation of the non-volatile element; however, control signals can be used to

achieve the same function as N2 and N3, such that these transistors can be removed. As shown in Figure 2(c), the circuit in the dotted box on the left hand side generates the control lines (where C1C and C2C are the switch signals). The paths are formed only during the restore operation; thus, when the 6T holds data, Q and $\bar{Q}$ cannot be changed. The 9T1R cell is based on the 11T1R cell by removing the two access transistors, but it still retains the voltage divider scheme (and therefore the resistance range of the MTJ). Thus, the resistance values of the MTJ are the same as for the 11T1R cell. The sequence for the restore '1' operation is shown in Figure 5.

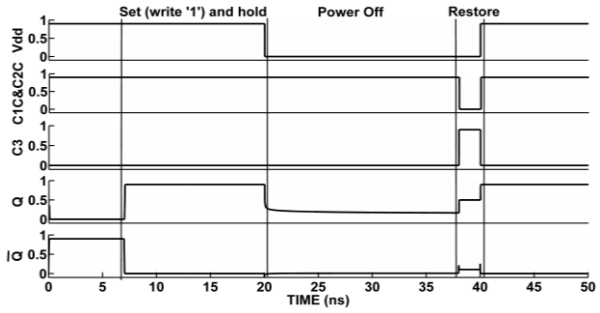

Figure 5. Simulation of proposed NVFF/SRAM 9T1R cell; timing diagrams of Vdd, C!C/C2C, C3, Q and $\bar{Q}$ for the restore '1' and power-on operations

IV. Comparative Evaluation

In this section, the 3 NVFF/SRAM cells (9T1R, 7T1R and 11T1R) are evaluated. Delay, power, static noise margin and process variability are addressed in this section.

A. Delay

Different operations are evaluated for the proposed cells. The definitions of the delays of these operations in the non-volatile cells are presented.

- *Read Time:* The read operation only occurs in the 6T, thus the read delay is the same as for the SRAM.
- *Write Time:* the MTJ and the 6T core are written separately. The write operation of the SRAM is the same as the 7T1R write operation. When the access transistors are turned on, Q and $\bar{Q}$ connect to D and $\bar{D}$. The MTJ also employs D and $\bar{D}$ in the write operation, i.e. the current orientation for writing the MTJ is determined by the value of D and $\bar{D}$.
- *Restore Delay:* the restore delay is the delay between the start of the restore signal and the availability of the restored data. For the 7T1R cell, the restore delay is the latency between the signal C2 and the data at Q when executing the restore '1' operation. For the 11T1R cell, the restore operation is divided into two steps and the restore delay is the sum of the delays of both steps.

TABLE I
Delay of 3 NVFF/SRAM Cells

	7T1R	11T1R	9T1R
Set (Write '1')	24.4ps	24.3ps	24.4ps
Reset (Write '0')	24.4ps	24.3ps	24.4ps
Read '1'	23.2ps	23.9ps	23.1ps
Read '0'	23.2ps	23.9ps	23.1ps
Restore '1'	112.8ps	38.3ps	16.4ps
Restore '0'	-	38.5ps	16.9ps

The simulation results are reported in Table I. The write and read delays of the three cells are very similar, because they utilize the 6T SRAM as volatile core. A marginal improvement in the read delay is accounted by the 9T1R cell. As discussed in a previous section, the 7T1R structure has only a restore '1' delay; among the three cells, the 7T1R (9T1R) cell has the larger (shorter) restore delay.

B. Restore Power

In this case, the measured power is the average power during the restore operation (both for the restore '1' and '0' cases). The simulation results are shown in Table II. As expected an increase in the number of MOSFETs in a cell results in an increase of power dissipation for the restore operation.

TABLE II
Restore power of 3 NVSRAM structures

	7T1R	11T1R	9T1R
Restore '1'	26.7uW	50.7uW	29.3uW
Restore '0'	13.9uW	45.6uW	36.2uW

The 7T1R (11T1R) cell consumes less (more) power than the other two cells; in addition to the larger number of transistors, the non-volatile part of the 11T1R cell is a voltage divider that consumes static power during its operation.

C. SNM

Two types of SNM are considered in this manuscript for the evaluation of the proposed cells. (1) The conventional SNM (denoted as 6TSNM) as applicable to a 6T SRAM core for the read (RSNM) and write (WSNM) operations. (2) During the restore period, the noise margin at A in the 7T1R cell, and A and B in the other two cells is assessed for the restore operation. This shows the noise the cell can tolerate during the restore operation and is defined as the rstSNM. For 8T2R and 11T1R cells, the rstSNM is the average voltage difference between A and B in the restore '1'and '0' operations. For the 7T1R cell, the rstSNM is the difference voltage value between A and the threshold voltage that can drive Q to '1'.

TABLE III
SNMs of 3 NV FF/SRAM structures

		7T1R	11T1R	9T1R
6TSNM	*WSNM*	322.4mV	312.4mV	314.8mV
	RSNM	117.3mV	117.3mV	117.3mV
rstSNM		130mV	245.3mV	471.4mV

The simulation results are shown in Table III; the 7T1R cell has the weakest restore operation. The 11T1R cell is the most stable scheme for the restore operation. For the 6TSNM, the three cells show little difference in values because the core executes the Read and Write operations in all of these three schemes.

D. Process Variation

Variations in both the MTJ and the MOSFETs are evaluated for the cells to assess their impact on the memory cells' operations using Monte Carlo simulation. Since all the three cells utilize the 6T SRAM as core, the read and write operations are nearly the same; so only the restore operation is assessed as pertinent to the so-called 'instantly on, normally off' mode of operation. In the Monte Carlo simulation, the process variation

of a MOSFET considers the channel length and the threshold voltage. The variations in percentage for the MOSFET's parameters are taken from [12]; the variations in resistance for the non-volatile elements are reported in [12]. They are both shown in Table IV. In all variability cases, the global behavior of a circuit is considered

TABLE IV
VARIATION PERCENTAGE

	Vth	**L**	**R_{high} ,R_{low}**		
32nm	3%	2%	10%	5%	1%

TABLE V
VARIABILITY PERCENTAGE ON GLOBAL BEHAVIORS OF THREE CELLS (RESTORE '1' DELAY)

3σ/μ(%)		**7T1R**	**11T1R**	**9T1R**
R_{low}	10%	26.99	25.70	23.9
	5%	13.79	15.23	16.4
	1%	3.16	3.55	1.9
L		*	7.31	15.3
V_{th}		36.91	8.73	11.2

*The 7T1R cell may fail in the restore '1' operation

The simulation results (Table V) for the restore '1' show that the 7T1R cell has the least tolerance to process variations for both the MOSFET and the resistive element; the 7T1R cell has a very high variability percentage with respect to the threshold voltage. As shown in a previous section, the 7T1R cell may also fail when executing the restore '1' operation. The results for the restore '0' operation are given in Table VI; the 7T1R cell does not execute the restore '0'operation, so the delay cannot be measured. For the other two cells, the percentage variability of the MTJ is more pronounced for the 11T1R cell compared to the 9t1R cell; the reverse is applicable for the MOSFET variability.

TABLE VI
VARIABILITY PERCENTAGE ON GLOBAL BEHAVIORS OF THREE CELLS (RESTORE '0' DELAY)

3σ/μ(%)		**7T1R**	**11T1R**	**9T1R**
R_{low}	10%	-	9.1	8.3
	5%	-	4.3	4.2
	1%	-	1.3	1.6
L		-	5.0	15.2
V_{th}		-	13.8	17.2

V. CONCLUSION

This paper has presented three novel designs of a NVFF/SRAM cell with a restore operation that allows for non-volatile storage to write to a SRAM core once the power is reestablished. A 6T SRAM is employed as core (i.e. to execute the read and write operations) and write the data to the MTJ based non-volatile circuitry. A MTJ cannot be used as non-volatile element in the complementary cell of [5] due to its resistance features (such as range). Hence, the three cells that have been investigated in this paper utilize only a single MTJ, while using additional MOSFETs to improve different figures of merit. Different circuits are utilized for the restore operation but all cells employ a single MTJ as resistive device for non-volatile storage. The rankings of these cells are shown in Table VII. Simulation results have shown that an increase in the number of MOSFETs in the memory cells causes improvements in critical charge and tolerance to process variations at the expense of an increase in power dissipation. The SNM and the delay of the restore operation however do not necessarily increase with the number of MOSFETs in the cell but rather on the control of access to the storage nodes from the single MTJ.

TABLE VII
PERFORMANCE RANKING

	7T1R	**9T1R**	**11T1R**
Power	**1**	2	3
Restore Delay	3	**1**	2
SNM	3	**1**	2
Process Variation (Restore)	3	2	**1**

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