Evaluating the Impact of Spike and Flicker Noise in Phase Change Memories

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Abstract—This paper presents a simulation-based analysis of spike and flicker noise in a Phase Change Memory (PCM); this investigation is based on HSPICE simulation by taking into account cell-level (with its neighbors) and array-level considerations. State switching phenomena in binary PCM memories are dealt in detail to assess the impact of these two types of noise. It is shown that a lower feature size is of concern for flicker noise in terms of value and percentage variation (while not substantially affecting array-level performance). This paper also shows that spike noise has a radically different behavior: spike noise shows a dependency on the PCM resistance more than the type of state of the PCM. It increases substantially when the amorphous resistance increases and has a nearly constant value when the memory cell is changing to an amorphous state

Index Terms—Flicker noise, Spike noise, Phase Change Memory (PCM), Resistance, Frequency.

I. Introduction

The rapid growth and demand on portable storage require non-volatile memory (NVM) operation, Emerging NVM technologies have been proposed in the technical literature; they include the ferro-electrical random access memory (FeRAM), the magneto-resistive RAM (MRAM), and the phase change memory (PCM). PCM is regarded as an excellent candidate for the next generation NVMs due to its high density, fast speed, supply voltage requirements, excellent scaling capability and compatibility with a complementary metal oxide semiconductor (CMOS) fabrication process [1]. Recently, PCM has been proposed for replacing flash memory and DRAM due to its higher reliability/endurance [2] and lower cost than a conventional magnetic recording storage [3]. A PCM is usually fabricated by using a chalcogenide material with crystalline and amorphous phases and resistance state values of several orders of magnitude in difference [4]. However, there has been no study to assess the impact of noise in the operation of a PCM both at memory cell- and array-levels.

This manuscript deals with flicker and spike noise in a memory consisting of 1T1P cells (each cell is made of a MOSFET and a PCM). Flicker noise is one of the extrinsic mechanisms present in electronic devices due to the MOSFET device structure; flicker noise is depended on frequency and has been widely analyzed and modeled. Spike noise is the most common noise occurring during state switching.

In this paper, both these types of noise are analyzed at cell- and array-levels by considering different features, such as PCM resistances, MOSFET feature size and operating voltage. Simulation is utilized to assess the effects of noise within the nearest neighbors of a PCM cell as well as the whole memory array. The conditions in binary state switching (‘1’ to ‘0’ and ‘0’ to ‘1’) correspond to different resistance values in the PCM, hence impacting memory operations at different levels. This paper shows that at lower feature sizes, the flicker noise increases; however, it does not substantially change from cell- to array-levels. The increases in both value and percentage are substantial at a lower feature size; so, the percentage variation of this noise shows a direct relationship with its value. This is significant phenomenon because it could be problematic once smaller feature sizes are employed in memory design. When considering spike noise and switching, this paper shows that the state change from ‘1’ to ‘0’ generates a smaller spike compared to the other case; the spike noise increases substantially when the amorphous resistance increases, but it has a nearly constant value when the memory cell is changing to an amorphous state. Moreover, the variations of spike noise for crystalline and amorphous resistances have similar values, so it is shown that spike noise shows a stronger dependency on the PCM resistance rather than on the type of state of the PCM.

This paper is organized as follows. Section II deals with a brief review of the literature as related to PCM and noise. The PCM cell is assessed in Section III for both flicker and spike noise phenomena; array-level assessments of noise and variation analysis are pursued in Section IV. Section V concludes this manuscript.

II. Review

A. PCM

This section reviews different aspects as related to a phase change memory (PCM). As described previously, the phase change memory (PCM) is regarded as one of the most viable candidate for the next generation of non-volatile memories. A PCM relies on the reversible phase transformation of the

chalcogenide alloy (e.g. $Ge_2Sb_2Te_5$, GST) between the amorphous and the crystalline states. The amorphous state has a high resistance and is commonly referred to as the *reset state*; the crystalline phase has a low resistance and is referred as the *set state* [5]. The PCM device is fabricated by using a thin film chalcogenide layer in contact with a metallic heater. When a programming voltage/current pulse is applied to the PCM, a high current density flows in the resistive heater, thus raising the temperature of the active region as per the Joule effect [5]. The Joule heat generated in this region melts or crystallizes the phase change material to an amorphous, or a crystalline state. The temperature dependence of the phase change (PC) process is shown in Figure 1 [5].

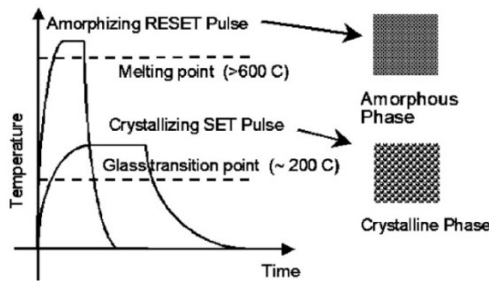

Figure 1. Temperature/time dependence of phase change process [5]

In Figure 1, the pulse with a high amplitude is used to melt and quench the PC element to an amorphous state (*Reset State*), while the longer pulse with a low amplitude is used to crystallize the PC element (*Set State*) [5]. Since switching between amorphous and crystalline states is based on the crystalline fraction of the PCM, the *electrical resistance* of the PCM cell is given as $R_{PCM} = (1 - C_x)R_a + R_c C_x$ [6] where R_c and R_a are the resistances of the PCM when it is fully crystalline and amorphous, respectively. C_x denotes the so-called *crystalline fraction*: when C_x is zero, then the PCM is fully amorphous; when C_x is equal to one, the PCM is fully crystalline [1]. If the PCM is in the Reset state (amorphous) and the voltage across the PCM cell is higher than the *threshold value* (V_{th}), then a snapback behavior occurs and the resistance of the PCM is switched to the R_{ON} (ON state) value. If the PCM is in the ON state, it will switch back to the OFF state if and only if the voltage across the PCM is less than the so-called *ON/OFF Intersection Point* [6].

B. Noise

Noise is usually defined as an unwanted disturbance that obscures or interfaces with the desired signal. Noise can be classified into four types: thermal noise, low frequency (1/*f*, flicker) noise, generation recombination (G-R) noise, and shot noise [7]. In this paper, flicker and spike noise are considered as applicable to electronic/resistive devices such as found in the 1T1P memory cell and array.

Flicker Noise: Flicker noise is a type of noise that is caused by material defects in electronic devices. Since its first experimental demonstration in the early 1960's, it has been extensively analyzed in the technical literature. This noise affects the n-MOSFETs rather than the p-MOSFETs [8], leading possibly to failure of this type of device [9]. In a transistor, flicker noise is one of the extrinsic mechanisms that manifest itself due to the intrinsic structure of the MOSFET [8]. It is also the main cause of phase noise for an oscillator or a phase lock loop; this leads to jitter [10]. There is a correlation between flicker noise and different properties of semiconductor materials and devices; so, this noise serves as a very sensitive measure of defects of semiconductor materials and devices, as well as quality and reliability [11]. It is also know as 1/f noise [12] because flicker noise is present in electronic devices and defines the principal threshold of a small signal at low frequencies. The actual value of flicker noise increases during the lifetime of a transistor [13]; the widely used model of this noise in MOSFETs is given by [14]

$$\text{flicker noise} = \frac{K_f}{C_i \cdot f^{\alpha_f}}$$

where K_f is an intrinsic process parameter for flicker noise, $\propto_f$ is an exponent (it usually has a value between 0.8 to 1.2), and C_i is the gate oxide capacitance (whose value depends on the size of MOSFET) ($C_i = C_{ox} \cdot W \cdot L$),where $C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox}}$.

Spike Noise: Spike noise shows as a high-frequency ripple; it is caused by a switching event [15]. It originates from both material and signal sources. Spike noise is caused by unevenness in circuit elements to exhibit random variations in structural features, such as MOSFET parameters (length, width and depth), as well as doping concentration, mobility of charge carriers and dielectric constant for a device. Moreover, the mobility of charge carriers depends on several secondary effects, such as density of scattering, crystal purity and applied voltage [16]. A spike voltage may cause the failure of a MOSFET and in some cases incorrect switching. In a memory, the characteristics of a spike may affect the read/write process causing errors in some cases [16-18].

III. Cell Level Evaluation

Consider a memory cell consisting of a transistor and a PCM (1T1P). In this cell, the source of the transistor is connected to the PCM, its drain to the Bitline (BL) and its gate to the Wordline (WL) [19]. The neighborhood of a cell (referred to as the *center cell*) consists of 8 cells (Figure 2), hence arranged as a 3x3 neighborhood array.The features of the PCM considered in this manuscript are given in Table 1; for modeling and simulation, each MOSFET has its own noise source (represented by a noise-current generator from drain to source [17]).

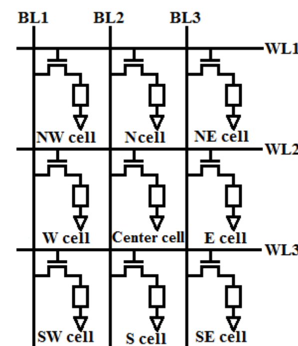

Figure 2. 3x3 PCM memory array.

Parameters	***Value***
R_a (Fully Amorphous Resistance)	200k Ohm.
R_c (Fully Crystalline Resistance)	7k Ohm.
R_{on} (On-Resistance)	1k Ohm.
V_{hold} (Holding Voltage)	0.45 V.
V_{th} (Threshold Voltage)	0.78 V.
T_g (Glass transistion point)	473 K (200 celsius)
T_m (Melting point)	873 K (600 celsius)

Table 1.PCM parameters used in the simulation.

To control a cell, the bitline and wordline voltages are connected to a signal and a controlled voltage value. When the memory cell changes a state, the surrounding cells are affected by a voltage input on both the Bitline and the Wordline. In the simulation, all cells are set to '0'; then the center cell (Figure 2) is set to the on-state (as '1'). The Bitline voltage is affected by the N and S cells, because the Bitline voltage can be sufficiently large to turn the MOSFETs on in both states. The voltage at the Bitline consists of two components: the voltage across the MOSFET and the voltage across the PCM. If the input voltage is set to a proper value, the voltage across the PCM will not be sufficiently large to change the state without the wordline voltage, as the voltage level required to turn on the MOSFET. However, when considering the E and W cells, the wordline voltage is equal to V_{dd} and the MOSFETs of the E and W cells are on.

Consider Figure 2 and the output voltages of the cells. When the center cell undergoes a state change, noise appears (Figure 3), but it is not sufficiently large to cause an error.

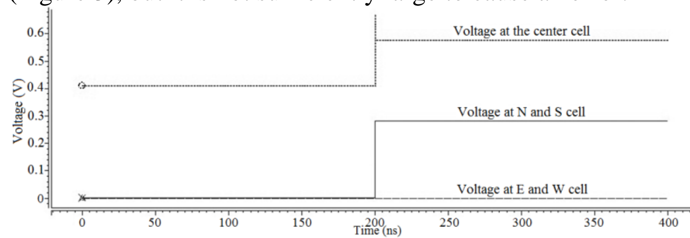

Figure 3. Output voltages of the cells.

In the nano ranges, both the PCM (as resistive element) and the MOSFET exhibit variability in many parameters, such as length (L), crystalline resistance (R_c), amorphous resistance (R_a) and threshold voltage (V_{th}). Table 2 shows the percentage variation of the different parameters of a MOSFET for various feature sizes [20]. The variations of R_c and R_a are fixed to 5% as representing the worst case [17].

Parameter / Feature size	L	V_{th}
16 nm	3%	5%
22 nm	2.5%	4%
32 nm	2%	3%
45 nm	2%	2%

Table 2. Percentage variation of MOSFET parameters at feature size

A. *Flicker Noise*

At cell-level, flicker noise is simulated by considering the center cell in Figure 2; Table 3 shows the parameters used in the simulation of the flicker noise. Figure 4 shows the plot of the flicker noise at a feature size of 32nm for the MOSFET. The PCM changes from state '1' to state '0' with a bias (bitline) voltage of 5V dc (Table 4) and 1μV ac for measuring the noise.

Parameter	***Value***
MOSFET (Level)	32 nm
Width (W)	32 nm
Length (L)	32 nm
t_{ox} (Oxide thickness)	1 nm
ε_{ox}	3.9
ε_0	8.854E-12
Flicker noise exponent ($\propto_f$)	1

Table 3. Device parameters for flicker noise simulation.

The small ac voltage is required for generating the frequency (from 1 to 1T Hz); the wordline is at 0.9V as V_{dd} of the MOSFET. The simulation results (Figure 4) show that the flicker noise appears at a low frequency and decreases exponentially with frequency (as expected).

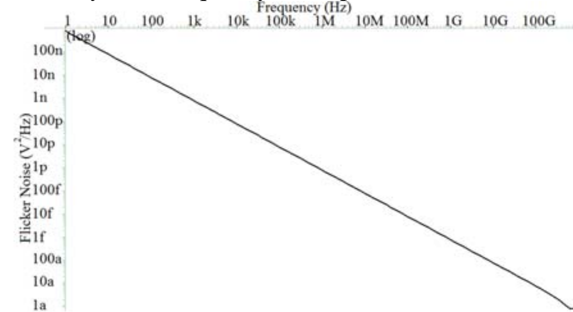

Figure 4. Flicker noise vs. frequency in PCM memory cell.

Switching / Feature size	**'0' to '1'**	**'1' to '0'**
16 nm	3.2V	4.3V
22 nm	3.5V	4.7V
32 nm	3.9V	5.0V
45 nm	4.2V	5.3V

Table 4 Bias voltage when changing the PCM resistance.

Figure 5 shows that at lower feature sizes, the flicker noise increases too, so possibly becoming of concern for the correct operation of nanoscaled memories.

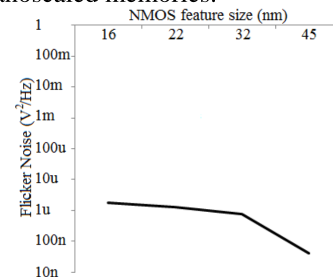

Figure 5 Flicker noise of 1T1P memory cell vs. feature size

However as the flicker noise is small, the value K_f is usually given by 0 (as default); however, simulation and the analytical equation for the flicker noise show that K_f is a sensitive non-zero parameter [14, 21]. The approximate value

of K_f in a short-channel device at 45nm is given by 1.62×10^{-24}. Table 5 shows its values at different feature sizes.

Feature size	***16nm***	***22nm***	***32nm***	***45nm***
K_f	1.35×10^{-23}	1.59×10^{-23}	1.76×10^{-23}	1.62×10^{-24}

Table 5. K_f at different feature sizes

B. Spike Noise

Spike noise may occur when the input voltage switches from one state to the other. The signal at the wordline is given as a square voltage from '0' to V_{dd} of the MOSFET under consideration; this is different from the simulation setup for the flicker noise. Spike noise is considered with respect to the feature size of a MOSFET and the value of R_a. The noise is measured for both state switching conditions ('1' to '0' and '0' to '1') in a cell. State switching generates a spike noise due to the changing voltage (that may also affect the operation of the cell [17]). To reduce the effect on other neighboring cells and any additional noise, the bitline voltage is given in Table 4 to change the data in the memory cell and state of the MOSFET (with same width and length), while the wordline voltage is given by a square signal (so of amplitude between 0 to V_{dd}). The plot of spike noise versus feature size is shown in Figure 6 for both cases of state switching.

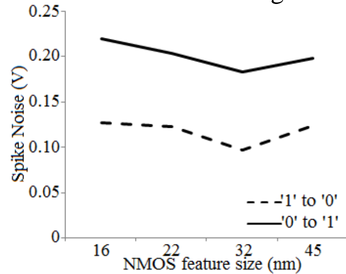

Figure 6.Spike noise when the memory cell changes from '0' to '1' and from '1' to '0' vs. feature size

When considering spike noise and switching, the state change from '1' to '0' generates a smaller spike compared to the other case. The simulation results for the spike noise in Figure 6 show that for switching from '1' to '0' requires a larger bias voltage and moreover, the voltage across the PCM at the reset state ('0') is higher than for the set state ('1').

The voltage for a state changes from '0' to '1' is lower than for '1' to '0', because it requires a lower voltage to change the data. The voltage across the PCM when its data is '1' has a smaller value, this causes a spike noise that is lower than for '0', i.e. the switching from '0' to '1' causes a larger spike noise than for the other case. Moreover, spike noise also depends on other parameters, such as the value of R_a. Figure 7 shows the spike noise when varying R_a. When the amorphous resistance R_a increases (while maintaining all other parameters constant), the spike noise increases substantially. When simulating this case, the crystalline fraction decreases with an increase of R_a; so, the PCM becomes less crystalline if the value of R_a is higher. When the frequency (f) increases there is no sufficient time to change the PCM from the amorphous to the fully crystalline states. Furthermore, the spike noise occurs only at the switching time of the PCM, thus a change in frequency does not affect the spike noise.

Figure 8 shows the value of spike noise of a 1T1P cell when the state of the PCM is changed from '0' to '1' at different values of V_{dd}. Only this state change is considered, because this state produces the highest value of spike noise.

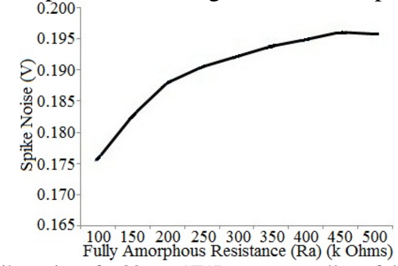

Figure 7. Spike noise of a 32 nm 1T1P memory cell vs. fully amorphous resistance R_a

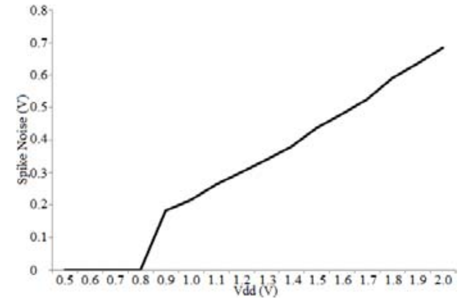

Figure 8. Spike noise of a 1T1P memory cell at 32nm vs. V_{dd}.

In this simulation, a feature size of 32nm is used (the nominal value of V_{dd} is 0.9V); the results show that between 0.5V and 0.8V, the voltage is not high enough to turn on the gate of the transistor, so the voltage at the bitline will not affect the PCM of the memory cell. The values between 0.9V and 2V correspond to a voltage range that can turn the PCM on and change its state from '0' to '1'; however, the cell cannot write '1' at the higher voltage, because these high values of voltage require higher temperatures to the PCM, so a '0' rather than '1' is best applicable as erroneous state switching.

IV. ARRAY LEVEL EVALUATION

In this section, the 1T1P cell is considered within a square array of dimension n; the effects of flicker and spike noise are then considered within an nxn memory array to assess the impact when different operational features are varied.

A. Flicker Noise

The same parameters as outlined previously for cell-level simulation are considered; simulation has shown that the flicker noise does not substantially change at array-level, so the same results as presented previously at cell-level are also applicable. This implies that flicker noise is only a concern with the cell neighbors (as shown in Figure 2 previously).

The flicker noise variation is simulated by a Poisson distribution that takes into considerations many physical parameters [13]. Figure 9 shows the flicker noise at different feature sizes. Simulation is pursued under the condition that the initial state of the PCM is the fully crystalline state, and the write voltage is set to a value that changes the PCM to be more amorphous.

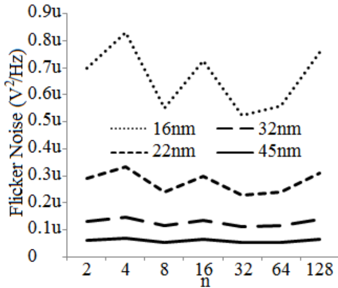

Figure 9. Flicker noise for different feature sizes vs. dimension of the array n

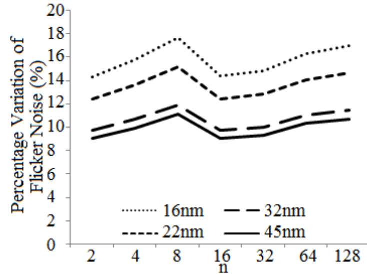

Figure 10. Percentage variation of flicker noise across PCM for different feature sizes vs. dimension of the array n

However, the flicker noise will be smaller for the initial opposite state (i.e. fully amorphous state) and a write voltage to have a more crystalline state, due to the smaller write voltage. The trend of the flicker noise in Figure 9 shows that at a lower feature size, the flicker noise increases (both in value and percentage); this is caused by the smaller values in MOSFET parameters due to scaling. Figure 10 shows the percentage variation of the flicker noise when the parameters are simulated by Monte Carlo. Moreover, the percentage variation of this noise shows a direct relationship with noise value; this is significant because it shows that it may be problematic once smaller feature sizes are employed in memory design.

B. Spike Noise

In this section, spike noise is considered at a feature size of 32nm for an nxn PCM memory array. It is well known that spike noise and the crystalline fraction (C_x) are not dependent on array size, hence, the impact of changing the fully amorphous resistance is considered. Figure 11 shows the results; spike noise increases rather modestly in the memory array at a 32nm feature size; moreover, the spike noise at different values of R_a is inversely proportional to the Signal-to-Noise Ratio (SNR), because the SNR decreases for an increasing R_a (Figure 12). Therefore, R_a can take a large value while still keeping a nearly constant SNR. Even though not specifically addressed in this manuscript, this feature confirms that a greater resistance range permits a multi-level implementation in a memory.

Figures 13, 14 and 15 show the spike noise when the dimension n is varied at different feature sizes and under different conditions; the simulation results are pursued when the state changes occur for either crystalline or amorphous. Figure 13 shows the spike noise when the feature size is varied versus n. A comparison between Figures 13(a) and 13(b) confirms that the change from the amorphous to the crystalline states results in a higher spike noise. This difference is related to the change in PCM resistance due to state switching.

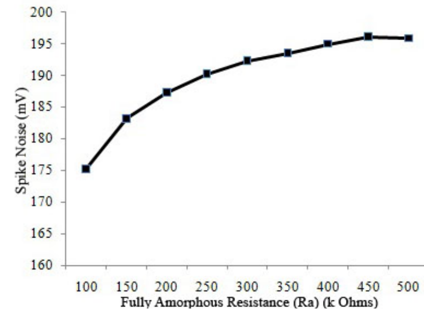

Figure 11. Spike noise vs fully amorphous resistance (Ra) of PCM cell at 32nm in an array of dimension 100.

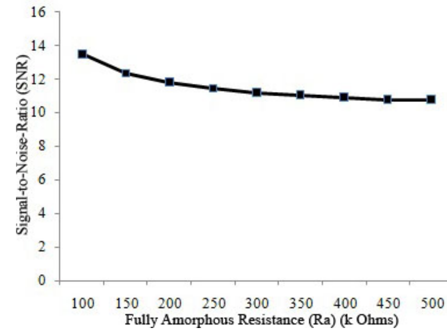

Figure12. Signal-to-Noise-Ratio (SNR) Vs. Fully Amorphous Resistance (R_a).

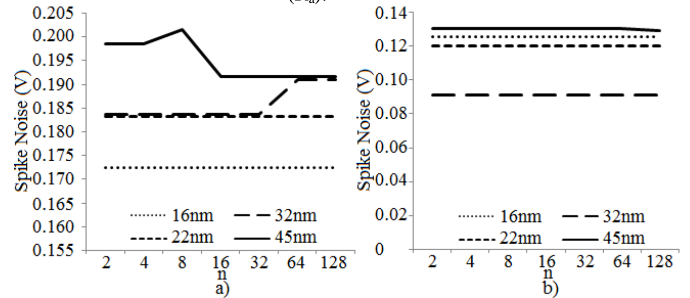

Figure 13. Spike noise when changing state to a) crystalline b) amorphous at different feature size vs. n.

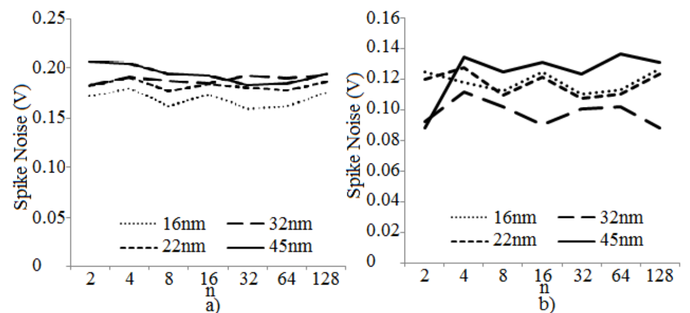

Figure 14. Spike noise when changing state to a) crystalline b) amorphous at different feature size vs. n.

Figure 14 shows the spike noise when simulation takes into account the variations in MOSFET (Table 2) and PCM

resistance. The trends are similar to Figure 13, even though now the spike noise is not as constant as in Figure 13(b).

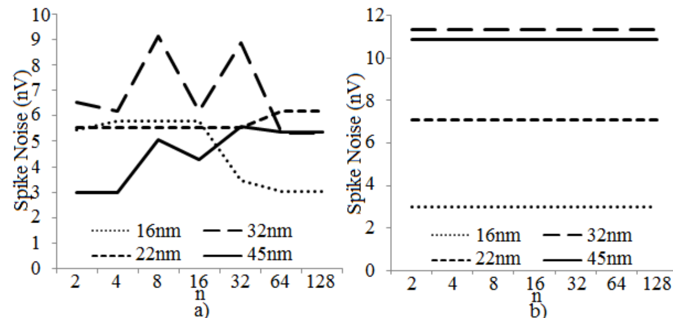

Figure 15. Spike noise when changing state to a) crystalline b) amorphous at variation of the threshold voltage (V_{th}) vs. n.

Figure 15 shows the simulation results when only the threshold voltage is changed (as in Table 2). A variation in V_{th} does not cause a significant amount of spike noise; these simulation results also show that also in this case, spike noise has a nearly constant value when the memory cell is changing to the amorphous state.

V. Conclusion

This paper has presented a simulation-based analysis of spike and flicker noise in a Phase Change Memory (PCM); this investigation was pursued using HSPICE simulation. In this paper, both these types of noise have been analyzed at cell- and array-levels by considering different features, such as PCM resistances, MOSFET feature size and operating voltage. The following conclusions can be drawn from the simulation results:

- *Flicker noise:* this noise is inversely proportional to MOSFET feature sizes, but for PCM memories, it does not substantially change from cell- to array-levels. The increases in both value and percentage are substantial at a lower feature size and the percentage variation of this noise shows a direct relationship with its value. As memory technology moves to the nanoscales, this phenomenon could be of serious concern.
- *Spike noise:* when considering switching, this paper has shown that the state change from ‘1’ to ‘0’ generates a smaller spike compared to the other case; the spike noise increases substantially when the amorphous resistance increases, but it has a nearly constant value when the memory cell is changing to an amorphous state. Moreover, the variations of spike noise for crystalline and amorphous resistances have similar values, so it has been shown that spike noise has a stronger dependency on the PCM resistance rather than on the type of state of the PCM.

Current research deals with assessing the effects of thermal noise; note that thermal noise in a PCM is mostly due to an external component (i.e, the heater) for a state transition (as shown previously in Figure 1).

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