A 6.0-13.5 GHz Alias-Locked Loop Frequency Synthesizer in 130 nm CMOS

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***Abstract*—A 6.0-13.5 GHz Alias-Locked Loop (ALL) frequency synthesizer is designed and simulated in 130 nm CMOS. Using an aliasing divider, the ALL architecture makes it possible to create high-speed frequency synthesis circuits without relying on a traditional divider clocked at f_{VCO} in the feedback path. In this implementation, a new architecture of high frequency ring oscillator is proposed with a feedforward path and selectable modes of operation for different frequency ranges. This ring oscillator provides both a high oscillating frequency and a wide tuning range. Simulation results have shown that the design synthesizes the desired frequencies and consumes 30.01 mW @13.0 GHz with a 1.2 V power supply.**

***Index Terms*—Alias-Locked Loop (ALL), Ring oscillator, Subsample, Phase-Locked Loop (PLL).**

I. Introduction

THE phase-locked loop (PLL) is a critical component in many circuits and systems as it provides the timing basis for functions such as clock control, data recovery, and synchronization. With the fast development of radio frequency and millimeter wave communications, high frequency synthesizers have become more important in recent years. A 410 GHz CMOS Push-Push oscillator has already been demonstrated [1]. In a traditional PLL implementation, a divider in the feedback path converts higher frequencies to lower frequencies. Unfortunately, a traditional divider in PLL is based on flip-flops and will not work at such high frequencies. Designers usually resort to regenerative dividers [2] or injection locked dividers [3] to extend the operating frequency of their devices. However, both injection locked dividers and regenerative dividers typically rely on shunt peaking inductors that cost large areas and have limited tuning range.

To alleviate this problem, a new frequency synthesizer architecture, the Alias-Locked Loop (ALL), was proposed in [4]. Previous sub-sampling based PLLs resort to analog samplers and are aimed at better power and noise performance [5] [6] [7]. In the ALL architecture, the traditional divider is replaced by an aliasing divider, implemented with a high speed digital sampling latch, although a D flip-flop (D-FF) can be used. This sampling circuit uses a stable reference clock to sample the voltage-controlled oscillator (VCO) signal. Since the sampling frequency is significantly lower than the sampled signal, the VCO signal will be subsampled, creating an alias frequency. In this way the high frequency of the output signal of the VCO can be lowered, which in turn can be fed into a CMOS divider or directly to a conventional phase-frequency detector (PFD). Similar to a PLL with a fractional-N divider or a bang-bang PFD, the ALL structure gains a lower cost in area and power consumption compared to a traditional PLL.

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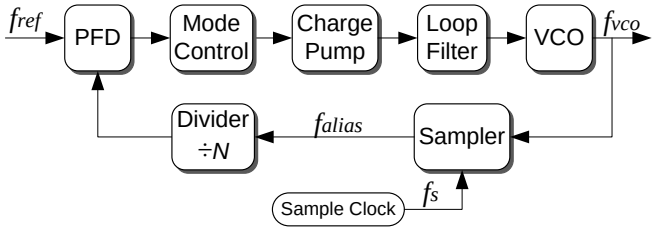

Fig. 1. A general block diagram of an ALL [4].

In this paper, a 6.0-13.5 GHz ALL frequency synthesizer is proposed. In particular, a high frequency, wide tuning range ring VCO is implemented based on the feedforward loop ring VCO in [8] and motivated by the design in [9] [10]. The circuit is designed in IBM CMRF8SF 130 nm bulk CMOS process. All schematic simulations were performed using Spectre/SpectreRF with normal threshold voltages, V_{DD} = 1.2 V, temperature = 27 °C and nominal transistor models. Simulation has shown that the design synthesized frequencies from 6.0 GHz to 13.5 GHz with a power consumption of 30.01 mW @13.0 GHz.

This paper is organized as follows: Section II gives a review of the ALL structure and its mathematical model. Section III presents the design considerations and circuit realizations. Section IV provides the simulation results and discussions. Finally, Section V concludes the paper.

II. Background

Fig. 1 shows a general structure of an ALL. Most of the modules in an ALL are the same as in a traditional PLL. A phase-frequency detector (PFD) compares the phase (frequency) of the reference clock with the feedback signal and then generates a control signal for a charge pump. The charge pump converts the phase difference to current that controls the charging or discharging operation of the capacitor in the loop filter, thereby the control voltage of the VCO is tuned. Differently from a traditional PLL, however, the *N*-divider between the VCO and the PFD is replaced by a high speed sampling circuit. In addition, a divider is applied after the sampling circuit. With the help of an additional module named Mode-Control which causes a continuously negative feedback

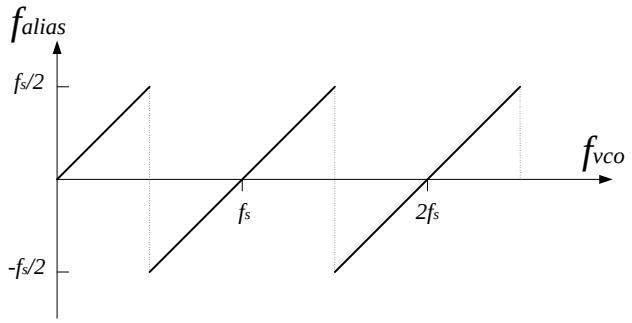

Fig. 2. Frequency produced by the aliasing divider [11]

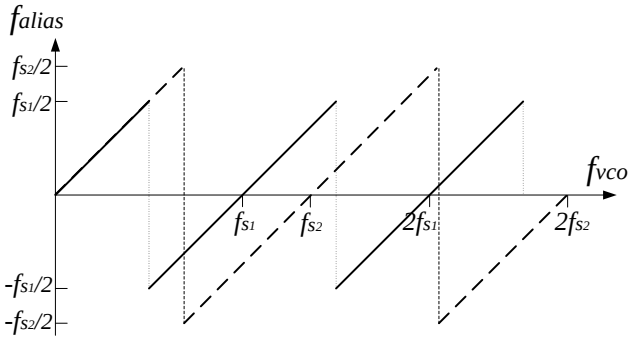

Fig. 3. Frequency produced by two sampling frequencies

loop, an ALL is able to lock the desired frequency after a period of time.

As shown in Fig. 1, the output of the VCO is subsampled with a pulse clock, whose frequency is much lower than the VCO signal. The output of the sampling circuit is a so-called alias signal of the VCO output. The frequency of the alias signal f_{alias} is determined by both the VCO frequency f_{VCO} and the sampling frequency f_s, as shown in Fig. 2 [11]. **We describe f_{alias} as being negative, if when the frequency of the input of the sampler increases, the output of the sampler decreases. Detailed analysis of negative alias frequencies will be covered in Section II.**

Therefore, the frequency can be calculated as:

$$f_{alias} = f_{VCO} - f_s \times round(\frac{f_{VCO}}{f_s}), \tag{1}$$

where round(x) rounds to the nearest integer value. The phase difference of the divided alias signal and the reference signal is detected by a PFD. Since the frequencies of both the two signals are not high, a conventional PFD is sufficient. When the loop is locked, the absolute value of the divided alias frequency f_{alias}/N will be equal to the reference frequency f_{ref}, i.e.,

$$\frac{|f_{alias}|}{N} = f_{ref}. \tag{2}$$

(1) and (2) lead to the following equation:

$$f_{VCO} = \begin{cases} M \times f_s + N \times f_{ref}, & for\ f_{alias} \geq 0, \\ M \times f_s - N \times f_{ref}, & for\ f_{alias} < 0, \end{cases} \tag{3}$$

where *M* can be any positive integer.

Once the loop is locked, the frequency determined by (3) is synthesized. Multiple values of *M* can, however, satisfy (3). Therefore for a given reference signal and a constant sampling signal, there exist a number of VCO frequencies that can meet all the requirements and finally make the loop locked. This is different from a traditional PLL. In fact, different initial conditions of the control voltage of VCO result in different *M*, and thus result in different output frequencies. So in an ALL architecture, careful considerations should be taken on choosing initial conditions of the VCO. Designers can initialize the charge pump with a digital-to-analog converter (DAC) fed from a lookup table, so the ALL will start out and lock in the correct frequency range (correct value of *M*).

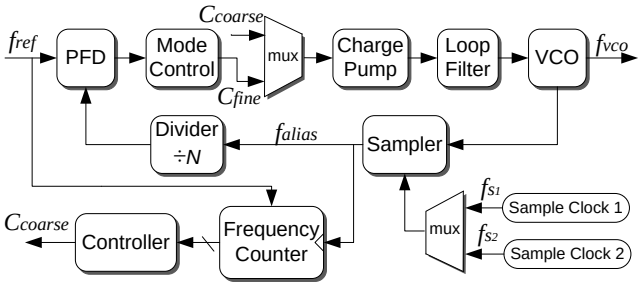

Fig. 4. An ALL with two sampling frequencies

Alternatively, f_{VCO} can be uniquely determined if two sampling frequencies f_{s1} and f_{s2} are used to produce two alias frequencies as shown in Fig. 3. Fig. 4 illustrates the functional blocks of an ALL using two sampling frequencies. With a multiplexer and a frequency counter, the frequency of the VCO can be uniquely determined within the tuning range of the VCO by choosing two appropriate sampling frequencies. The controller, using the multiplexer, measures f_{alias} with f_{s1} and f_{s2}, determines f_{VCO} and makes a coarse adjustment (C_{coarse}) to f_{VCO} until f_{VCO} is in the correct frequency range. Then the ALL loop is closed (C_{fine}), bringing the synthesizer into lock.

Having two sampling frequencies to select between is also useful to avoid $f_{alias} = 0$ or $f_{alias} = 0.5f_s$ where lock is not possible as discussed in Section IV. A.

III. Implementation

A. Sampler

The original idea of a high speed sampler is based on a sense-amplifying flip-flop (SAFF) [13] [14]. A sense amplifier is typically applied in the SRAM implementations, because it can detect a subtle voltage difference. Combined with CMOS differential logic, sense-amplifying structures can significantly reduce delay, size and power.

It should be noted that it is different when an SAFF is applied as a digital sampler and when it is applied to implement a divider. Generally, the highest frequency at which the SAFF can function properly is determined by the precharge period. When applied as a digital sampler, the precharge phase in an SAFF is constrained by the sample frequency. However,

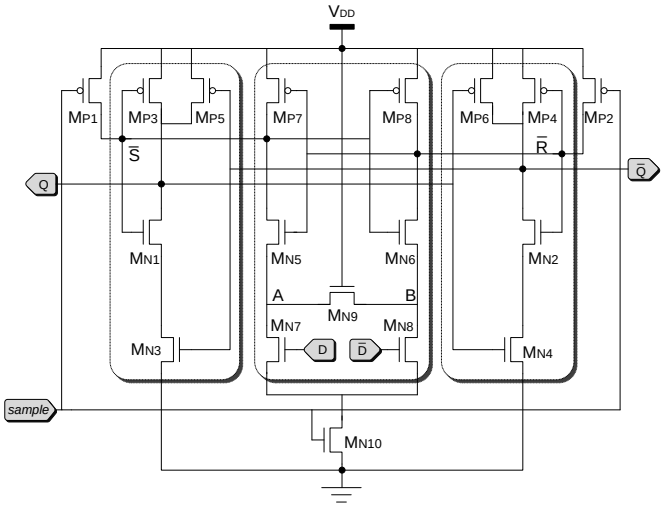

Fig. 5. Sense-amplifying flip-flop based sampling circuit [14]. The first stage (in the center) senses a differential input, while the second stage (on either side) provides a full-swing output signal.

when applied in a divider, the precharge phase of the SAFF is determined by f_{VCO} because it should recognize every edge of the VCO output. It is the SAFF structure that makes it possible to reach more than 70 GHz operating frequency in the proposed ALL design, compared to a highest operating frequency of 5.0 GHz for a TFF under the same condition in the same 130 nm process.

As shown in Fig. 5, the circuit of the sampler is composed of two cascaded latches. The sense-amplifying master latch consists of M_{P7-8} and M_{N5-9} with dynamic logic. The dynamic logic requires two phases: precharge phase when the clock signal is low and evaluation phase when it is high. During precharge phase, M_{P1} and M_{P2} turn on and M_{N10} turns off. Since M_{N9} always turns on at this phase, nodes $\bar{\text{S}}$, $\bar{\text{R}}$, A and B are all charged to high. In the evaluation phase, M_{P1} and M_{P2} turn off and M_{N10} turns on. The differential input voltage of D and $\bar{\text{D}}$ determines that A and B have different voltages before they are completely discharged. During this tiny discharge time delay on M_{N9}, the state of the input is latched. The cross transistor, M_{N9}, forces the whole differential tree precharge and discharge rapidly in every clock cycle, regardless of the state of input data [14]. Therefore, the delay of M_{N9} will affect the speed of latching. **With any sampler differential input offset error less than the VCO signal in, the f_{alias} signal will continue to be produced, albeit with an asymmetric duty cycle. Observing the active (e.g. rising) edge of the output of the sampler, the asymmetric duty cycle would be observed as a constant phase offset compared to an ideal sampler, which would not affect the loop behavior.**

Sense amp output nodes Q and $\bar{\text{Q}}$ stay high during the precharge phase. Hence, there is a need to condition these signals with a NAND RS-latch, producing stable latched differential data before proceeding to the divider or PFD.

Generally, the frequency of the sample clock f_s is much lower than that of the input signals, i.e., D and $\bar{\text{D}}$ from the VCO. Since sampling occurs at the rising edges of the sample clock, only is the residue frequency (which is obtained by dividing the frequency of input by the frequency of the sample clock) reflected into the output of the sampler.

One explanation can be given as follows. Assume that

$$f_{VCO} = x \times f_s, \tag{4}$$

where x is a positive fraction.
Let

$$x = L + r, \tag{5}$$

where L is a positive integer, r is a fraction and $0 \leq r < 1$. Further assume

$$r = \frac{P}{Q}, \tag{6}$$

where both P and Q are positive integers, and $0 \leq P < Q$. Applying equations (5) and (6) into (4), we obtain

$$f_{VCO} = L \times f_s + \frac{P}{Q} \times f_s. \tag{7}$$

Noting that the period $T = 1/f$, equation (7) implies

$$Q \times T_s = Q \times L \times T_{VCO} + P \times T_{VCO}. \tag{8}$$

Equation (8) shows that during a time of $Q \times T_s$, the sampler gets Q samples of the inputs. Among the Q samples, the outputs get the same voltage value ('0' or '1') for P times, while for the other $Q-P$ times, the other voltage state ('1' or '0') is sampled. So when $P < \frac{Q}{2}$, the sampled output voltage flips P times; when $P > \frac{Q}{2}$, the sampled output voltage flips $Q-P$ times. This means that with a total of Q samples within each $Q \times T_s$ time period, the sampled output voltage flips $min(P, Q-P)$ times. Therefore, the average period of output signal, $\overline{T}_{out}$, is

$$\overline{T}_{out} = \frac{Q \times T_s}{min(P, Q-P)}. \tag{9}$$

Thus, the average frequency of output, $\overline{f}_{out}$, is

$$\overline{f}_{out} = \frac{min(P, Q-P)}{Q} \times f_s. \tag{10}$$

However, it should be noted that when $P > \frac{Q}{2}$, if the frequency of the input of the sampler increases, the output of the sampler is lowered instead of being increased, which is different from the condition when $P < \frac{Q}{2}$. This is the reason that some of the alias frequencies are negative, as shown in Fig. 2. Actually, these negative frequencies can invert the PFD output and cause the ALL to be a positive feedback loop, which is unstable. Detailed analysis and solutions are presented in Section III. C.

Particularly, when $P = 1$, we have $min(P, Q-P) = 1$, and the output frequency is as follows:

$$\overline{f}_{out} = \frac{min(P, Q-P)}{Q} \times f_s = \frac{1}{Q} \times f_s. \tag{11}$$

This corresponds to the condition that the sampling frequency is a multiple of the alias frequency. In this condition, the alias output could be directly reached by the sample clock instead of resorting to a fast signal and a slow signal.

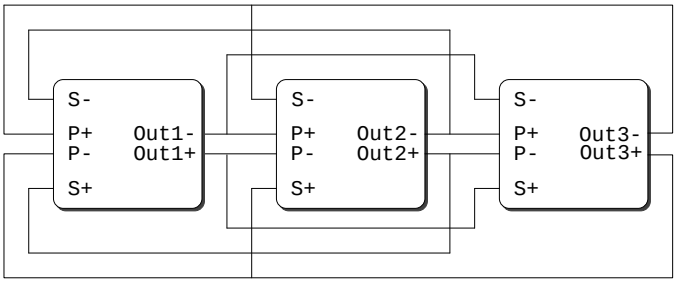

Fig. 6. Block diagram of the three-stage feedforward ring oscillator [9]. Unlike conventional ring oscillators, inputs are connected to forward outputs as well as previous outputs.

Assume that a 10.4 GHz signal is sampled by a 1 GHz clock. According to (4) - (6), P = 2 and Q = 5. With T_s = 1 ns, the output T_{out} should be 2.5 ns. However, the output period must be a multiple of T_s in a digital sampling circuit. Therefore, the period of the output will alternate frequently between 2 ns and 3 ns to achieve an average of 2.5 ns. However, if the input is a 10.1 GHz signal and is sampled by a 1 GHz clock, then we have P = 1, Q = 10, $Q - P$ = 9, and $\overline{f}_{out}$ = 100 MHz, which could be easily achieved by the 1 GHz clock itself.

According to the above transient behavior analysis of the sampler, the frequency of the output is the residue of the input frequency divided by the frequency of the sample clock.

B. VCO

Ring oscillators have higher phase noise than typical LC oscillators, but require less silicon area and typically have a higher tuning range. For traditional ring VCOs, the highest frequency is limited by the delay of the number of modules, which is typically the delay of three inverters. For comparison purposes, an optimistic design for a three-inverter based ring oscillator (each inverter with a optimized ratio of W_{pmos} : W_{nmos} = 1.6 : 1) without frequency control operates at 8.3 GHz, unloaded, under nominal conditions.

Fig. 6 shows a block diagram of the 3-stage feedforward ring oscillator proposed in [9] (and based on the design in [8]). Unlike traditional ring VCOs, feedforward oscillators have two feedback loops. For every stage, the phase of the signal in the second loop stays ahead of that of the main loop, which makes the circuit oscillate at a higher frequency. Instead of inverting the signal after each stage as in traditional ring oscillators, a feedforward design implements phase shifting after each stage. The phase shift of each stage can be calculated as the total phase shift divided by the number of stages.

Fig. 7 shows the proposed implementation of the single stage in Fig. 6. It consists of 9 NMOS transistors and 6 PMOS transistors. The inputs and outputs are all differential. P+ and P- are the inputs of the main feedback loop, while S+ and S- are the inputs of the second feedback loop. The NMOS latch makes the outputs of each stage (OUT+ and OUT-) differential. The proposed design works in **multiple** modes to cover a wide range of tuning frequency. **In the following part, two extreme scenarios corresponding to a V_{mode} of 0.35 V and 1.2 V, named high mode and low mode, are discussed.**

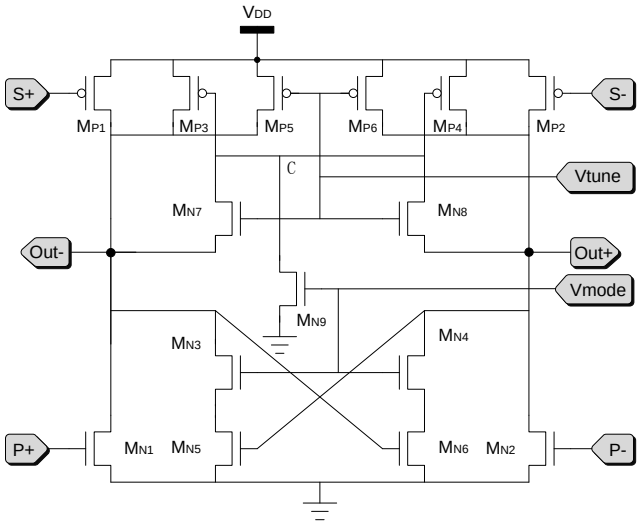

Fig. 7. Proposed implementation of each ring oscillator stage. Each stage consists of 6 PMOS transistors and 9 NMOS transistors.

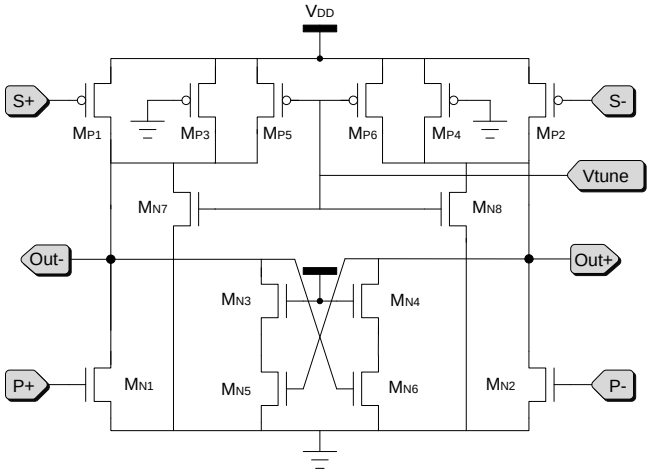

Fig. 8. Simplified architecture of Fig. 7 in low mode when Vmode = V_{DD}

1) Low mode ($V_{mode} = 1.2$ V):

When $V_{mode} = 1.2$ V, M_{N3} and M_{N4} are fully turned on, therefore M_{N3}, M_{N4}, M_{N5} and M_{N6} consist of a latch. M_{N9} is also turned on. Since M_{N9} is rather large compared to other transistors, node 'C' is clamped to GND. Therefore the circuit can be simplified as shown in Fig. 8 and is improved from the design in [10].

Compared with the design in [10], the design in Fig. 8 has an additional pair of NMOS transistors M_{N7} and M_{N8}, which are also controlled by the tuning voltage V_{tune}. In this mode, the output frequency is tuned by the driving capability of each stage. This is done by adjusting the current from PMOS to NMOS in each stage.

At a high voltage, V_{tune} turns on M_{N7}, M_{N8} and turns off M_{P5}, M_{P6}. While it prevents generating extra current by turning off M_{P5} and M_{P6}, it discharges part of the total current directly to ground by turning on M_{N7} and M_{N8}. Therefore, the total current in the NMOS transistors becomes less when V_{tune} is at a high voltage. This leads to a smaller driving capability at each stage, and therefore state transitions

at the output become slow. As a result, a high tuning voltage results in a low oscillating frequency in this mode. On the contrary, when V_{tune} is low, it will turn off M_{N7}, M_{N8} and turn on M_{P5}, M_{P6}, thus resulting in more current in the NMOS transistors. This in turn increases the driving capability of each stage. The delay at each stage is thus decreased. Consequently, a low tuning voltage yields a high oscillating frequency. Simulation results have shown that in this mode, the VCO can oscillate from 5.92 GHz to 9.2 GHz with a power consumption from 24.91 mW to 30.86 mW.

2) High mode ($V_{mode} = 0.35$ V):

When $V_{mode} = 0.35$ V, M_{N3}, M_{N4} and M_{N9} work in the sub-threshold region. Although the strength of the NMOS latch (consisting of M_{N3}, M_{N4}, M_{N5} and M_{N6}) is very weak, it still makes Out+ and Out- differential. The frequency of the output is tuned by the current travelling from PMOS to NMOS. M_{N9} provides a path from node 'C' to ground. This path is slow and weak, yet it prevents the floating of node 'C'.

When the tuning voltage is low, M_{N7} and M_{N8} are turned off, whereas M_{P5} and M_{P6} are turned on to provide more current to the NMOS. Also it should be noticed that the voltage at node 'C' is close to 0 since the only path to ground is provided by M_{N9}. Therefore, M_{P3} and M_{P4} are turned on and thus generating extra current. Since M_{N3} and M_{N4} are "off", the increased current will travel through M_{N1} and M_{N2} to ground. More current through the path leads to a larger driving capability and therefore results in faster transitions between different states. As a result, the oscillation frequency is rather high when the tuning voltage is low. However, when the tuning voltage is high, M_{N7} and M_{N8} are turned on and work as pass transistors; the outputs Out+ and Out- travel through M_{N7} and M_{N8} respectively, and merge at node 'C'. Since the two outputs are differential signals, the voltage at node 'C' will be close to half of V_{DD}, which is about 0.6 V. Compared to the previous situation in which node 'C' is close to 0, the current generated by M_{P3} and M_{P4} is much weaker. Therefore the current in M_{N1} and M_{N2} is weaker and this results in slower transitions between different states. Consequently, the frequency of the oscillator is low when the tuning voltage is high.

However, when V_{tune} is close to V_{DD} , both M_{P5} and M_{P6} are off, and therefore the current changes little when V_{tune} changes. At the same time, M_{N7} and M_{N8} are both on, so the voltage at node 'C' should be stable when the tuning voltage changes. This limits the tuning range of the proposed Ring VCO. Simulation results have shown that in this mode, the VCO can oscillate from 9.1 GHz to 13.52 GHz with a power consumption from 14.12 mW to 31.69 mW.

As stated above, there can be multiple possible values for V_{mode}. In fact, continuously tuning V_{mode} between 0.35 V and 1.2 V can ensure the oscillator covers the full frequency tuning range even with process, voltage, and temperature (PVT) variations. For instance, simulation has shown that the oscillator can oscillate from 7.65 to 11.16 GHz when V_{mode} = 0.8 V.

Fig. 9 shows the simulation results of the differential outputs at each stage and the 120° of phase shift after each stage. Fig. 10 shows how the oscillation frequencies change with

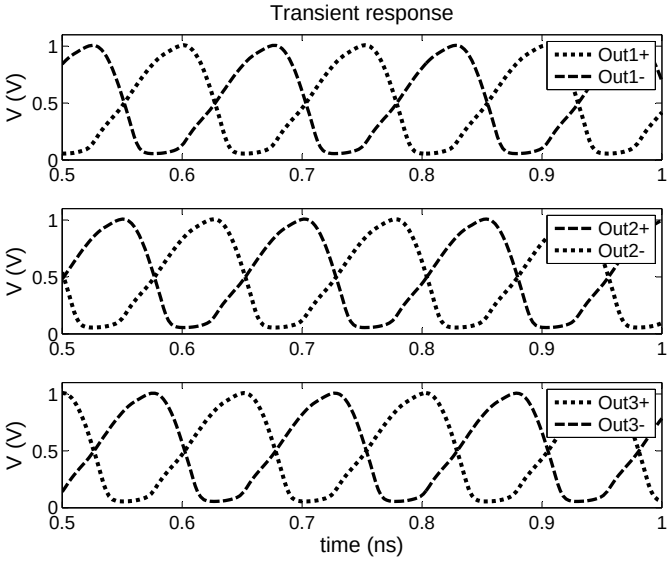

Fig. 9. Transient simulation results of the three stages of the proposed VCO are shown with each stage shifting the phase by 120°.

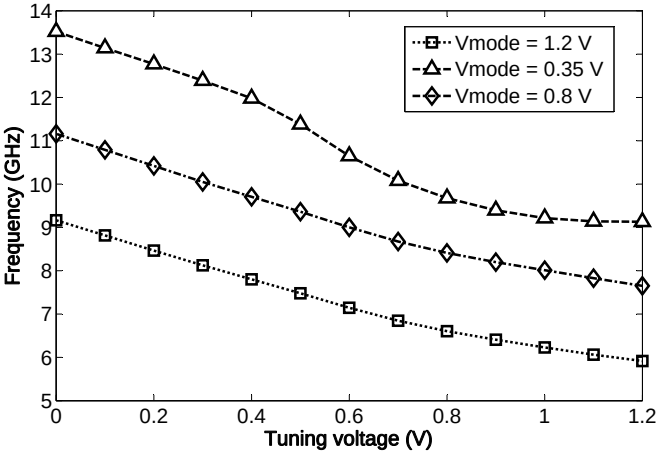

Fig. 10. Simulation results of different modes **at normal PVT corners**: when V_{mode} = 1.2 V, the VCO oscillates from 5.92 to 9.2 GHz; when V_{mode} = 0.35 V, the VCO oscillates from 9.1 to 13.52 GHz; **when V_{mode} = 0.8 V, the VCO oscillates from 7.65 to 11.16 GHz.**

different tuning voltage at different modes. Consequently by controlling V_{mode}, the proposed design can oscillate from 5.92 GHz to 13.52 GHz **at normal PVT corners. The oscillator can oscillate from 8.22 GHz to 17.26 GHz at the highest speed corner (FF, -40 °C, +10% V_{DD}), and from 4.93 GHz to 10.74 GHz at the lowest speed corner (SS, 110 °C, -10% V_{DD}).**

Phase noise simulation was performed using SpecterRF phase noise analysis, normal process corners and process device noise models. The results, shown in Fig. 11, show a phase noise of -69.36 dBc/Hz @ 1 MHz offset and -96.15 dBc/Hz @ 10 MHz offset from an f_c of 13.0 GHz. One downside of a wide continuous tuning range within any mode is that the large K_{VCO} comes with larger phase noise than a ring oscillator with a more narrow continuous tuning range.

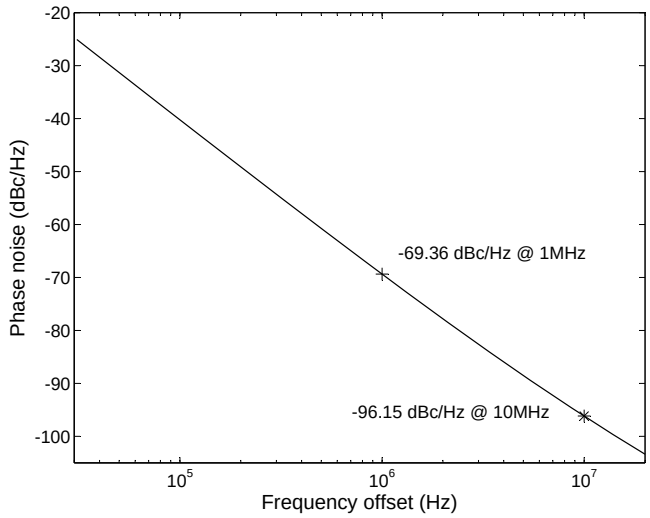

Fig. 11. **Phase noise of the proposed VCO at 13.0 GHz**

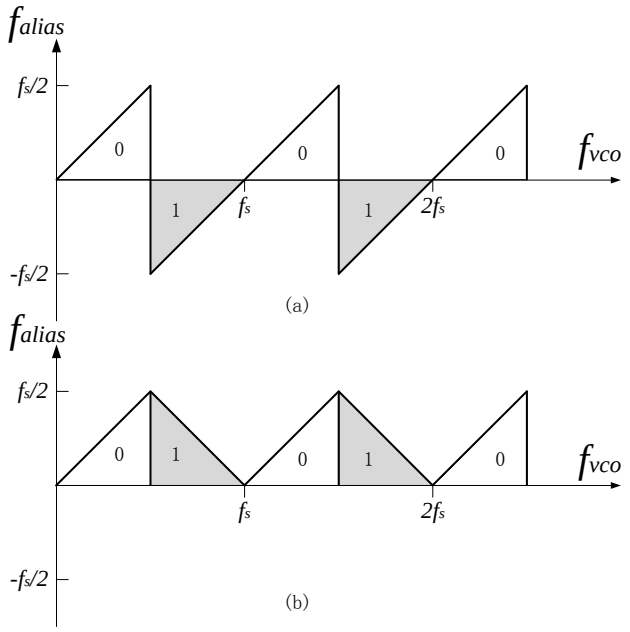

Fig. 12. (a) Frequencies produced by the aliasing divider without Mode-Control. (b) Equivalent frequencies produced with Mode-Control.

C. Mode control

As shown in Section II, the sampler in an ALL utilizes the residue function. For the positive alias frequencies (Region 0 in Fig. 12(a)), the ALL becomes a negative feedback loop. This means that the loop is stable and therefore it can synthesize the desired frequencies. However, if the alias frequencies are negative (Region 1's in Fig. 12(a)), it forms a positive feedback loop.

To solve this problem, a module named Mode-Control (Fig. 1) inverts the sense of the PFD output (swaps the two PFD outputs: $'UP'$ and $'DOWN'$) for Region 1's in Fig. 12(a), restoring stable, negative feedback control. Fig. 12(b) shows the equivalent frequencies produced when Mode-Control is applied.

It should be noted that the sampling frequency directly determines the number of regions in Fig. 12. If a lower frequency signal, i.e., the reference clock, is applied as the sampling clock, then there will be more Region 0's and Region 1's within the VCO tuning range, which requires a high resolution DAC to initialize the VCO into the correct frequency range. However, if a higher frequency sampling clock is applied instead, there will be fewer Region 0's and Region 1's, therefore easing the requirement of the DAC resolution. Another drawback of a lower sampling frequency is that it will result in more special frequencies that require an alternate f_s to achieve lock, which will be discussed in detail in Section IV. A.

D. Other components

Other modules in the ALL architecture are implemented with conventional static CMOS designs. A conventional PFD is used to compare the phase difference between the divided alias signal and the reference clock. The charge pump applies the improved single-ended design [12] and the loop filter is a second-order passive low pass filter. In addition, an extra module of a **divide-by-4** implemented with conventional D-flip-flops is added after the sampling circuit to **further reduce the frequency of the feedback signal and then lower the frequency of the reference clock. Another important function of the divider is to adjust the phase of the alias signal. However, problems such as additional power consumption, extra area cost, longer lock-in time and potential higher phase noise should be taken into careful consideration.**

The oscillator and sampler in the ALL require careful circuit design and optimization. The other components in Fig. 1 do not operate at the high frequencies so available standard cells will suffice.

IV. SIMULATION AND DISCUSSION

In this Section, simulation results are reported to show the proposed ALL design is able to synthesize the desired frequencies. An example is given to illustrate how the architecture works. A discussion of noise property that is different from a traditional PLL follows.

A. Simulation of the synthesizer

As discussed in Section II, different initial conditions of the tuning voltage of VCO will result in different *M* in (3), therefore resulting in different output signals. So the initial condition of the VCO is important to the function of an ALL.

It is shown in the following how the desired frequencies are synthesized. Take 10.7 GHz as an example. Using 1 GHz as the sampling frequency, the frequency of the alias signal is: f_{alias} = -300 MHz, and the frequency of the reference signal is f_{ref} = 300 MHz/4 = 75 MHz. Since the alias frequency is negative, the Mode-Control module should swap the PFD outputs $'UP'$ and $'DOWN'$ to ensure the ALL is a negative feedback loop. With such information, however, it is likely that the ALL will not be able to get the expected frequency

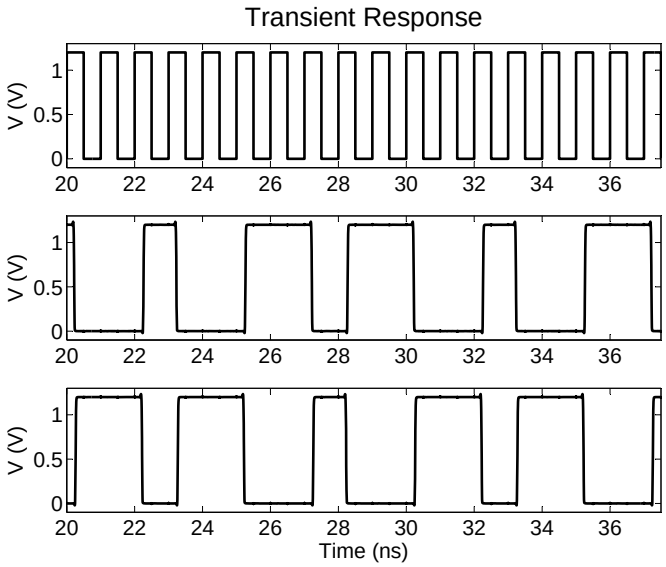

Fig. 13. Alias output of 10.7 GHz input sampled by the 1 GHz clock. The upper signal is the 1 GHz sample clock, and the lower two signals are the differential alias signals. We can see that the 300 MHz (period = 3.3 ns) alias signal is obtained from the mean value of one period of 250 MHz(period = 4 ns) and two periods of 333 MHz(period = 3 ns) every 10 ns.

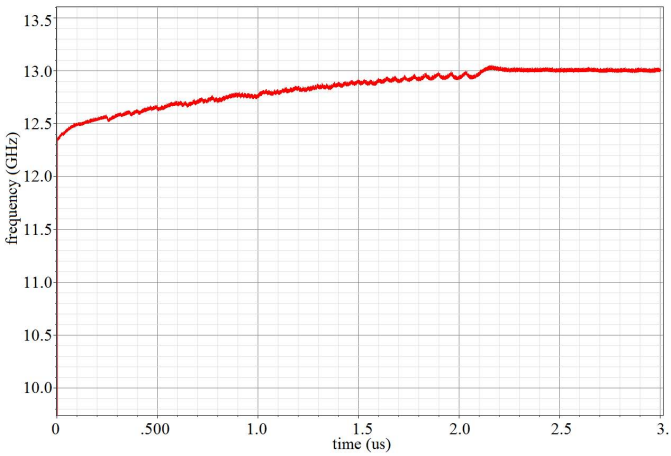

Fig. 14. Transient lock-in behavior when synthesizing a 13.0 GHz signal with f_s = 1.25 GHz, f_{ref} = 125 MHz and a **divide-by-4**.

since some other frequencies, such as 9.7 GHz, also satisfy the above requirements. By setting an initial frequency of the VCO, the ALL can successfully select and synthesize the expected frequency. This is realized by initially charging the loop capacitor and thereby setting the initial value of the tuning voltage of the VCO in this design. Initial conditions are set according to the look-up table of the VCO as shown in Fig. 10.

However, some special frequencies need additional considerations. These frequencies are multiples of one half of the sampling frequency. As analyzed in Section III, the alias frequency of such a signal is 0. Take a sampling frequency of 1 GHz for example. If a 13 GHz (or 13.5 GHz) signal is desired to be synthesized, it can be seen in Fig. 12(a) that the loop is not a continuous negative feedback loop around the target frequency for either mode. Hence, the sampling frequency of 1

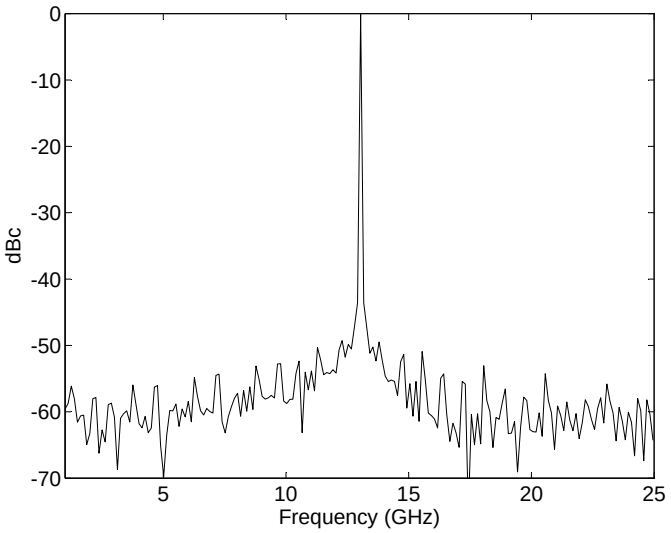

Fig. 15. Frequency domain analysis of the synthesized 13.0 GHz signal

GHz cannot be used to synthesize this frequency. As a result, for these frequencies, another sampling frequency has to be applied. Fig. 14 shows the simulation results of synthesizing a 13.0 GHz signal with a sampling frequency of **1.25 GHz** and a reference clock of **125 MHz**.

Without buffering, the sample clock can feed backwards and modulate the VCO signal, producing spurs on both sides of the synthesized signal. Fig. 15 shows the frequency domain analysis of the synthesized signal, which can satisfy the requirements of wireline communications. As for applications that require lower phase noise, such as RF communications, LC VCOs are preferred.

B. Discussion of phase noise

In most cases, an ALL synthesizes frequencies by the mean value of higher frequencies and lower frequencies. The simulation results of the alias signal are shown in Fig. 13. Take 10.7 GHz for example. The 300 MHz (period = 3.3 ns) alias signal is obtained from the mean value of one period of 250 MHz (period = 4 ns) and two periods of 333 MHz (period = 3 ns) every 10 ns. As a result, the 10.7 GHz VCO signal is reached by the mean value of 10.75 GHz and 10.67 GHz. Simulation results also show that the voltage of the loop filter reaches a rather stable state that fluctuates between two values. This is consistent with the transient behavior of the alias signal in Fig. 13, and different from traditional PLLs, in which the synthesized frequencies are expected to be a single value once locked in an ideal situation. So, compared to traditional PLLs, an ALL has the advantage of not using inductors, but it may suffer from the problems of additional phase noise and jitter.

However, there are potential solutions to lower the phase noise. The first is to carefully design and optimize the loop filter so that the fluctuation of the voltage is reduced. Low pass filters can be designed to meet the requirements of the phase noise.

A second possible solution is to properly choose the sampling frequency. As shown in equation (9), when the period

of the reference is not a multiple of the sampling period, the alias clock will alternate between two clock periods so that the average alias period matches the reference clock. However, if the period of the reference is a multiple of the sampling period, which means $P = 1$ in equation (11), then the expected alias clock will be given as the alias frequency itself. For example, if a 9.3 GHz signal is expected to be synthesized, 900 MHz will be a good choice for the sampling frequency. Since the expected alias frequency is 300 MHz, (i.e., a period of 3.33 ns), it can be easily obtained using a 1.11 ns period sampling signal. As a result, there is no need to apply two alternating signals. This corresponds to only one single frequency at the VCO output when locked in an ideal condition. However, a sampling frequency of 1 GHz would not be as good as 900 MHz. Although the expected alias signal is also 300 MHz with a period of 3.33 ns, according to [8], the alias signal could only be the mean value of one period of 250 MHz signal (period = 4 ns) and two periods of 333 MHz signal (period = 3 ns) in every 10 ns. This corresponds to the scenario where two stable frequencies alternate frequently at the VCO output when locked in an ideal condition. Therefore, a sampling frequency of 900 MHz results in a better design that provides a better phase noise and timing jitter performance.

V. Conclusion

We have designed and simulated a high frequency alias-lock loop with a novel oscillator in a 130 nm CMOS process. The proposed feedforward ring oscillator **has multiple selectable modes** to obtain a wide tuning range (6.0 GHz - 13.5 GHz) and has no passive components. It is capable of oscillating much faster than an inverter-based ring oscillator whose frequency is no higher than 8.3 GHz in the same process.

The high speed digital sampler in the feedback path provides wide range control of frequency without the need of a flip-flop or counter clocked by f_{VCO}. This will be particularly important for millimeter wave communications and radar circuits.

VI. Acknowledgements

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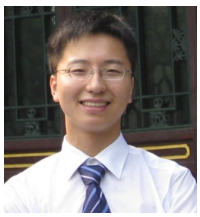

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