Feedback-Based Low-Power Soft-Error-Tolerant Design for Dual-Modular Redundancy

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Abstract—Triple-modular redundancy (TMR), which consists of three identical modules and a voting circuit, is a common architecture for soft-error tolerance. However, the original TMR suffers from two major drawbacks: the large area overhead and the vulnerability of the voter. In order to overcome these drawbacks, we propose a new complementary dual-modular redundancy (CDMR) scheme for mitigating the effect of soft errors. Inspired by the Markov random field (MRF) theory, a two-stage voting system is implemented in CDMR, including a first-stage optimal MRF structure and a second-stage high-performance merging unit. The CDMR scheme can reduce the voting circuit area by 20% while saving the area of one redundant module, achieving at least 26% error-rate reduction at an ultralow supply voltage of 0.25 V with 8.33% faster timing compared to previous voter designs.

Index Terms—Markov random field (MRF), soft-error tolerance, triple-modular redundancy (TMR).

I. INTRODUCTION

Triple-modular redundancy (TMR) was first proposed by Von Neumann et al. [1], and has since been adopted as a technique to improve error tolerance at the cost of increased circuit area. TMR can only tolerate soft errors when the probability of three or two modules failing simultaneously is much lower than that of a single module. However, one obvious drawback is the increased area overhead. Therefore, partial TMR [2] (PTMR) was proposed to reduce the area overhead by trading off reliability. The dual-modular redundancy (DMR) scheme presented in [3] uses a three-module structure with self-feedback. Robust C-elements [4] and multiplexers [5] are used, respectively, to form voters in two different DMR designs. An algorithmic noise-tolerant (ANT) technique [6] was proposed to solve the problem of soft errors caused by voltage over scaling. Algorithmic soft-error tolerance (ASET) [7] and fine-grain soft-error tolerance (FGSET) designs [8] are both extended ANT designs. The designs in [1]–[3] and [5]–[8] suffer from two drawbacks. First, they still consume large area overhead. Second, reliability loss is incurred by soft errors in the voting circuit. The reason is that redundancies in [1]–[5] and estimator-based redundancies in [6]–[8] work only well when voters never fail, which might be an unrealistic assumption if the circuits are designed using a deep submicron technology or an ultralow supply voltage is used. Under such conditions, it is likely that such a failure could occur in the voting circuit, which is a main cause of TMR failure [9]. For a multistage design, three identical voters could be used in each stage to tolerate errors that occur in one of the TMR voters, but this would add undesirable overhead to the design. Some approaches, such as generalized modular redundancy [10], approximate TMR [11], and a simulation-based synthesis scheme [12], improve the original TMR, but they only offer either an optimal implementation strategy or tradeoff accuracy.

A number of error-tolerant methods, such as Markov random field (MRF) [13]–[15], differential cascode voltage switch (DCVS) [16], and DCVS-MRF [17], have been proposed. In these designs, the basic elements include feedback loops that help them to achieve high soft-error tolerance. However, these implementations require higher area overhead than traditional structures. To solve soft-error issues in the voter and save area overhead, we propose a new complementary DMR (CDMR) scheme, as shown in Fig. 1. The CDMR scheme ensures the significance of soft-error tolerance even for the voting circuit. This is achieved by separately processing one module (M1) through a structure with a stable logic “1” as output (referred to as structure A in Fig. 1, and processing another identical module (M2) through a structure with a stable logic “0” as output (shown in Fig. 1 as structure B). A second-stage feedback structure is then used to merge the stable logic “1” and stable logic “0” outputs from the first stage, ensuring the best performance from the first stage (shown in Fig. 1 as structure C). The CDMR scheme outperforms existing designs in two key aspects by: 1) tolerating many soft errors propagated to the voting circuit and 2) saving the area overhead.

The remaining material is organized as follows. Section II briefly reviews background. Section III describes the design of the proposed two-stage structure and explains how such a structure works together to improve the soft-error tolerance and the reliability of the voter. Section IV presents the simulation results. This brief is concluded in Section V.

II. BACKGROUND

Distinct from the methods in Fig. 2, the proposed MRF-based design achieves soft-error tolerance by using a feedback structure based on the energy function [13], specifically the clique energy $U(\text{In}, \text{Out})$. In a logic circuit, the clique energy describes the energy
function of a clique referring to as a subset formed by fully related logic nodes (e.g., inputs and a corresponding output) [14]. The rules for an MRF-based design ensure that the clique energy of correct logic states is lower than that of wrong logic states. These rules state that first, all the input–output states should be considered including correct and incorrect input–output combinations. Assume that there is a transformation rule from Boolean to algebraic operation: $\mathbf{x} \rightarrow (1 - \mathbf{x})$, $x_1 x_2 \rightarrow x_1 x_2$. Let $f(x_0, x_1, \ldots, x_n)$ be an operation function for nodes $X = \{x_0, x_1, \ldots, x_n\}$, where $f = 1$ represents a correct operation; otherwise $f = 0$. Second, define the clique energy to be $U(x_c) = -\sum f_i(x_0, x_1, \ldots, x_n)$ over all the states of the operation, where $i$ indexes the different node values. The MRF-based elements are designed based on function $U(x_c)$, where $f_i = 1$. For example, the clique energy of an inverter is $U(x, y) = -x^2$ by only summing the valid states. Note that valid states remain at the lower energy "−1" relative to the invalid states at "0." When circuits tend to enter and remain in the lower valid energy states, the circuit has a high probability of operating correctly despite the presence of soft errors [13]–[15].

III. MRF-INSPIRED TWO-STAGE FEEDBACK DESIGN

In this section, we present an MRF-inspired two-stage feedback voter by substituting an inverting module for one of the identical modules in Fig. 1. MRF circuit design has been demonstrated to effectively stabilize the circuit into correct states to tolerate soft errors by lowering the energy of the correct states. For stage 1 in Fig. 1, we implement the MRF design and produce a NAND–NAND-based feedback structure.

Assume that an $n$-bit-input one-bit-output function $M$ is a clique, and $\gamma = \gamma_{\text{out}} + \sigma(\text{Noise})$ represents the sum of the noise-free output $\gamma_{\text{out}}$ and environmental noise. The clique energy is $U(X_{\text{in}}, y)$, where $X_{\text{in}} = \{x_1, x_2, \ldots, x_n\}$ are input signals and $\gamma_{\text{out}}$ is the output of a logic function $U(X_{\text{in}}, y)$.

Theorem: Assume that $\gamma_{\text{out}} = M(X_{\text{in}})$ is the simplest representation of the Karnough map simplification (canonical sum of minterms). In a noisy environmental the clique energy is

$$U(X_{\text{in}}, y) = -M(X_{\text{in}}) \cdot y - M(X_{\text{in}}) \cdot \overline{\gamma}.$$

Proof: According to the findings in [13]–[15], in an MRF-based design, valid states have a lower energy than that of invalid states and so, those designs will tend to operate correctly despite the interference of soft errors from noise. Thus, ideal input $\gamma_{\text{out}}$ should be equal to actual output $y \cdot \gamma_{\text{out}} = M(X_{\text{in}}) = y$, as shown in Table I. Then, $U(X_{\text{in}}, y) = -M(X_{\text{in}}) \cdot y - M(X_{\text{in}}) \cdot \overline{\gamma}$ is the clique energy that will help the structure settle into the valid states which have the lower energy "−1."

According to the above theorem, we propose the NAND–NAND structure shown in Fig. 3 to improve soft-error tolerance in the first stage. The clique energy

$$U(X_{\text{in}}, y) = -M(X_{\text{in}}) \cdot M(X_{\text{in}}) \cdot y - M(X_{\text{in}}) \cdot \overline{\gamma}$$

can be inferred from $U(X_{\text{in}}, y) = -M(X_{\text{in}} - y - M(X_{\text{in}}) \cdot \overline{\gamma}$. We assume that output $x_a = M(X_{\text{in}})$ and $\overline{x_a}$ is $M(X_{\text{in}})$ under noisy conditions. The structure in Fig. 3 satisfies the clique-energy requirement, and thus helps keep the circuits in the correct state.

From a probability perspective, we consider errors affecting one module at a time in this brief because, for a fair comparison, TMR only tolerates errors occurring in one module [3]. The one error condition is defined as the condition where only one module is erroneous at the input to the voting circuit. Under this condition, we will first analyze the error tolerance of the first stage. $g_1$ in Fig. 3 has a higher error tolerance of a noisy "0" at an input since the correct output probability with noisy inputs {0,0,0,1,10} is larger than that with noisy {11} in a NAND gate.

Proof: The probability of an input being incorrect under the effect of noise is $p_e$ ($0 \leq p_e \leq 0.5$); $p(y|x_1 x_2)$ represents the conditional correct probability of output $y$ when the inputs are $x_1$ and $x_2$ in a NAND; $p(1|00) = 1 - p_e^2 \geq p(1|01) = p(1|10) = 1 - p_e(1 - p_e) \geq p(0|11) = (1 - p_e)^2$.

Assume that the correct input pair $\{x_a, \overline{x_a}\}$ for the previous redundant modules, $M$ and $\overline{M}$, is {0, 1}. If $M$ is corrupted by noise, the incorrect output from $(M, \overline{M})$ momentarily becomes {1, 1}. In this case, $g_1$ can still tolerate the error by the inverter as long as the output of $M$ remains correct, while $g_2$ cannot. However, the second-stage structure in Fig. 4 can complement the loss of the error tolerance in $g_2$ for the first stage using its latching property. The proposed structure benefits from the presence of stage 2 to improve its reliability, which is a feature that TMR, DMR, or other designs lack.

Let us extend the single-error assumption for stage 1 by assuming that only one error can emerge from one of the complementary propagation chains at the same time. In other words, when an error occurs from stage 1, the latch structure of $g_3 - g_4$ in stage 2 does not propagate errors received from stage 1. With respect to our proposed CDMR, the two redundant inputs to the voter must be complementary.

<table>
<thead>
<tr>
<th>$y_{\text{in}}$</th>
<th>$y$</th>
<th>State</th>
<th>Clique Energy $U(X_{\text{in}}, y)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M(X_{\text{in}}) = 0$</td>
<td>0</td>
<td>Valid</td>
<td>-1</td>
</tr>
<tr>
<td>$M(X_{\text{in}}) = 0$</td>
<td>1</td>
<td>Invalid</td>
<td>0</td>
</tr>
<tr>
<td>$M(X_{\text{in}}) = 1$</td>
<td>0</td>
<td>Invalid</td>
<td>0</td>
</tr>
<tr>
<td>$M(X_{\text{in}}) = 1$</td>
<td>1</td>
<td>Valid</td>
<td>-1</td>
</tr>
</tbody>
</table>

Fig. 3. Proposed first-stage structure.
and will propagate through stages 1 and 2 as complementary signals in the absence of errors. For example, an ideal input bit stream for \( x_d(x_a = x_b) \) is \([x_0 \sim x_4 = 0 \text{ and } x_5 \sim x_9 = 1]\). Four bits, \( x_7 \) and \( x_9 \) of \( x_d \) and \( x_1 \) and \( x_2 \) of \( x_e \) are flipped by noise, as circled by a small circle in Fig. 4. Their corresponding bits in the other branch are robust “1” because of the high tolerance of noisy input bit “0” in both NAND gates \( g_1 \) and \( g_2 \). This is why we only consider the cases where errors occur in weak “0” in \( x_d \) or \( x_e \). This condition causes the second stage \( g_3-g_4 \) to remain in the hold state in Table II acting as an RS latch, thus protecting the final output results from the influence of the error bits in \( x_d \) and \( x_e \) based on the previous correct outputs. We adopted the widely used double-exponential current source to simulate the above cases where a charged or ionizing particle hits the output “0” of stage 1 circuit [18]

\[
I(t) = \frac{Q_{\text{total}}}{\tau_f - \tau_r} (e^{-t/\tau_f} - e^{-t/\tau_r})
\]

where \( Q_{\text{total}} \) is the total charge caused by the particle strike, and \( \tau_r \) and \( \tau_f \) are the rising time constant and the falling time constant, respectively. As \( \tau_r \) and \( \tau_f \) are generally set to 50 and 164 ps for different process technologies, we used the current source \( Q_{\text{total}} = 70 \text{ fC} \) in our simulation. Regardless of whether \( x_d \) and \( x_e \) are both high or low, when a charged particle attacks \( x_d \) or \( x_e \), there is one single peak shown in Fig. 5 in output \( x_f \). Compared with a much longer pulse at the output of a TMR voter when an error hits on one of its inner branches, it can be regarded to be less harmless in the proposed voter after sampling, as the error is too short to be sampled multiple times. The results in Fig. 5 confirm the same error tolerance as what we deduced from the proposed structure in Fig. 4. In the extended one error condition, the output of our module can achieve correct operation as long as the two inner complementary signals are not in error at the same time. This is what TMR, DMR, or other voting circuits are incapable of. Thus, the proposed voting design is more reliable. Assuming that the error probability of module \( M \) is \( P_e \) when the voting circuit never fails, the error probability of our proposed structure is \( P_{\text{proposed}} = P_e^2 \). Comparing this with the error probability of TMR

\[
P_{\text{TMR}} = P_e^3 + 3(1-P_e)P_e^2 \geq P_{\text{proposed}}
\]
and strong $\rho = 0.5$ as a noise source to each input to inject soft errors. We also set the temperature to 50 °C instead of room temperature to simulate the presence of thermal noise, while our operating supply voltage is set as 0.25 V to achieve near-threshold computation. The injected noise is with respect to the period of the input signals, and it covers all the possible transient “double error” cases and “single error” cases occurring at different times. It aims to show that our design can handle soft errors arising from any random noises, such as crosstalk noise, thermal noise, and particle strike noise.

The results in Fig. 8 are an example that shows each output of the proposed structure in Fig. 4, where the noise is an independent Gaussian source with zero mean and 170-mV standard deviation. The seven curves in Fig. 8 represent three noisy input signals (first–third curves), and four voting outputs of the proposed design in Fig. 4 (fourth–seventh curves). The remaining two curves are the eighth curve showing the results of self-voting in Fig. 2(b) and the ninth curve depicting the result of TMR voter as in Fig. 2(a). Both the fourth and fifth curves are the outputs from stage 1 of our design. The fourth curve shows the high probability of a correct “0” in $x_a$ while the fifth curve shows the high probability of a correct “1” in $x_b$. Both the sixth and seventh curves are outputs from stage 2 of our design. They have the same performance shown in Fig. 8 but are much better than the performance of self-voting [3] and TMR [1] (the eighth and ninth curves).

We simulated the performance of different voting designs in Fig. 9. Compared to TMR [1], the results show that the proposed structure achieves on average 64.5% (68.2% for $\rho = 0.1$ and 61% for $\rho = 0.3$) reduction in error rate, 20% area reduction, and 8.33% delay reduction according to Synopsys Design Compiler. Compared to the self-voting in [3], our design achieves 36.3% (41.6% for $\rho = 0.1$ and 31% for $\rho = 0.3$) lower error rate, with 20% area saving and 15% delay reduction. Evidently, the proposed design presents a significant improvement over the TMR and self-voting. In Fig. 9, the reduction in error rate of the proposed voter achieves at least 26% compared to those of other voters.

We also simulated the performance of different schemes using an RCA in Fig. 10 under different input SNR conditions at a 0.25-V supply voltage. The results show that the proposed voter achieves a reduction in the error rate by at least 26% compared to those of other voters.
The multiplexer circuits would select the outputs of modules separately from stages 1 and 2. These challenges could be solved together if two bypass multiplexers were to be added after the two outputs of stage 2. In the “normal” position, the two multiplexers would select the outputs of modules \( M \) and \( \bar{M} \) respectively. To permit ATPG algorithms to run, you would resynthesize the circuit with the multiplexer control signal fixed at “bypass”; this would cause stages 1 and 2 to be pruned away by the synthesis tool, leaving a circuit that could be sent to ATPG to produce the test vectors. In production, those test vectors could be applied in “bypass” mode to test modules \( M \) and \( \bar{M} \) only, and then reapplied in “normal” mode to test the full circuit with DMR. The multiplexer circuits would increase the testability of the design, at the cost of the area for the voter. In this brief, a novel CDMR scheme is proposed for soft-error tolerance. The proposed design combines MRF theory and the inherent ability of the error tolerance of the logic gate with traditional redundancy techniques. It avoids the higher hardware cost of previous redundancy approaches, and it also improves the reliability of the voter. The proposed two-stage voter saves at least 20% in area and 8.33% in timing compared to the conventional redundancy design with at least 26% improvement in error tolerance at an ultralow supply voltage 0.25 V compared to previously reported voter designs. Implemented in a 4-bit RCA, the proposed CDMR scheme achieves at least 12.5% reduction in the error rate while it saves at least 30% of the area compared with previous DMR approaches when a voter is added at every stage. In the future, when the proposed CDMR is applied to chip implementations, multiplexers could be added to increase the testability of the design.

V. CONCLUSION

In this brief, a novel CDMR scheme is proposed for soft-error tolerance. The proposed design combines MRF theory and the inherent ability of the error tolerance of the logic gate with traditional redundancy techniques. It avoids the higher hardware cost of previous redundancy approaches, and it also improves the reliability of the voter. The proposed two-stage voter saves at least 20% in area and 8.33% in timing compared to the conventional redundancy design with at least 26% improvement in error tolerance at an ultralow supply voltage 0.25 V compared to previously reported voter designs. Implemented in a 4-bit RCA, the proposed CDMR scheme achieves at least 12.5% reduction in the error rate while it saves at least 30% of the area compared with previous DMR approaches when a voter is added at every stage. In the future, when the proposed CDMR is applied to chip implementations, multiplexers could be added to increase the testability of the design.

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