A Memristor-based TCAM (Ternary Content Addressable Memory) Cell

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***Abstract*—This paper presents a Ternary Content Addressable Memory (TCAM) cell that employs memristors as storage element. The TCAM cell requires two memristors in series to perform the traditional memory operations (read and write) as well as the search and matching operations for TCAM; this memory cell is analyzed with respect to different features (such as memristance range and voltage threshold) of the memristors to process fast and efficiently the ternary data. A comprehensive simulation based assessment of this cell is pursued by HSPICE. Comparison with other memristor-based CAMs as well as CMOS-based TCAMs shows that the proposed cell offers significant advantages in terms of power dissipation, reduced transistor count and search/match operation performance.**

Keywords—Memory Cell, Modeling, Memristor, Ternary Content Addressable Memory, TCAM.

I. INTRODUCTION

Ternary Content Addressable Memories (TCAMs) are widely employed in networking circuits for address classification and packet filtering [1]. High-performance network routers require fast and high capacity TCAMs for improved look-up performance of routing tables. However, the fabrication and design of TCAM chips with a large storage capacity have encountered substantial problems in CMOS. A significant problem is related to the design itself; ternary logic requires additional supply voltages if implemented by CMOS circuitry. Without the use of additional power rails, the size of the ternary memory cell is increased due to the utilization of two binary cells (i.e. at least 12 transistors, or 12T) and additional transistors for the related comparison circuit. While a TCAM cell with a reduced transistor count has been reported [2], stability problems are encountered if this cell is used in large storage chips. Also, a TCAM consumes significant power due to its operations such as a fully parallel search throughout the memory array)

. Power consumption may degrade chip reliability and affect packaging costs due to heat dissipation hardware. Although many approaches addressing power consumption have been reported [3-5], they result in circuit techniques that have substantial area overhead or deficiencies in noise immunity. Therefore, the high speed of a TCAM comes at a cost of increased silicon area and power consumption, two design parameters that designers strive to reduce. The power problem is further exacerbated as TCAM applications grow (with an ever increasing demand on large storage). A reduction in power consumption without sacrificing speed or area is one of the main threads of recent research in large capacity memory design such as for TCAMs [6].

The memory cells in a TCAM can store three states (i.e. '1', '0', '2'). The additional state '2' is also referred to as the "mask" or "don't care" state; it is used for matching to either a '0' or '1' in the input search data process. The search operations of a TCAM are performed by comparing in parallel the input (searched) data against the entire list of entries stored in memory. A TCAM is best suited for network applications such as a Network Intrusion Prevention System (NIPS), Ethernet address lookup, data compression, user privileges and routers [7].

This paper proposes a new hybrid design for a ternary CAM (TCAM) that utilizes both MOSFETs and memristors. This memory cell is analyzed with respect to different features (such as memristance range and voltage threshold) of the memristors to process fast and efficiently ternary data. A comprehensive simulation based assessment of this cell is pursued by HSPICE. Comparison with other memristor-based CAMs [8] as well as CMOS-based TCAMs shows that the proposed cell offers significant advantages in terms of power dissipation, reduced transistor count and search/match operation performance.

II. REVIEW OF MEMRISTOR

In circuit theory, the memristor (or memory resistor) is the 4th fundamental element that utilizes for its operation the relationship between flux and electric charge. This element was postulated by Chua in 1971[9] based on the concept of symmetry with other circuit elements, such as the resistor, inductor and capacitor. The relationship between the flux and the electric charge of a memristor is given by [8]

$$d\phi = M*dq \quad (1)$$

where M is the memristance or memristor value (in Ω), ϕ is the flux through the magnetic field, and q is the electric

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charge, i.e. the current moving through the memristor is proportional to the flux of the magnetic field that flows through the material. Therefore, the magnetic flux between the terminals is a function of the amount of charge (i.e. q) that flows through the device. (1) is equivalent to V=MI, where V and I are voltage and current across the memristor, respectively [8].

A memristor operates as a *variable resistor* whose value depends on the current or voltage across it, i.e. if there is a positive voltage across the memristor, its memristance will reduces to a small value (given by R_{ON}); if there is a negative voltage across the memristor, its memristanceincreases up to a high value (given by R_{OFF}). Hereafter, the memristor is considered as a switching resistance device; as applicable to the HP Labs implementation [10], the rate of change for the memristance is usually linear, provided its value is not close to the extreme values (R_{ON} and R_{OFF}). If the memristance value is close to the extreme values (R_{ON} or R_{OFF}), non-linearity is likely to occur for its rate of change.

As physical implementation of a memristor, HP Labs has fabricated a device based on a titanium dioxide film sandwiched between two platinum electrodes[11].The memristor consists of two parts (or regions), the doped region and the undoped region. The widths of the doped region (w) and the undoped region (L - w) change depending on the direction of the current or voltage across it. Let R_{ON} be the resistance for a completely doped memristor and R_{OFF} be the resistance for a completely undoped memristor; so, the current-voltage relationship of a memristor is given as follows.

$$v(t) = \left\{R_{ON}\frac{w(t)}{L} + R_{OFF}\left(1 - \frac{w(t)}{L}\right)\right\} i(t) \quad (2)$$

where w(t) is the width of the doped region, and L is the TiO_2 thickness [10]. As function of time, the width of the doped region is given by

$$w(t) = \mu_v \frac{R_{ON}}{L} q(t) \quad (3)$$

where μ_v represents the average dopant mobility (~10^{-10} $cm^2/s/V$). By differentiating w(t) in (3) with respect to time, the rate of change for the width of the doped region is given by

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{ON}}{L} i(t) \quad (4)$$

To model the characteristics of a memristor, different HSPICE models have been proposed in the technical literature [12-14]. These HSPICE models are based on window functions to simulate behaviorally and macroscopically a memristor according to its physical model. In this paper, the memristor model of [11] is used, because it has been shown to closely resemble the HP Labs memristor parameters and operation [9].

III. Proposed TCAM Cell

Due to its non-volatile characteristic, the memristor can be used as a storage device. A Ternary Content Addressable Memory (TCAM) cell is proposed in this paper. The three states of the TCAM are defined using 2 memristors as follows.

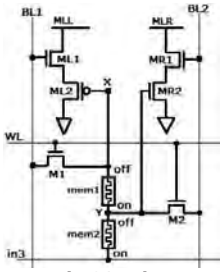

Figure 1. Proposed TCAM design using memristors

- For state ‘0’, both memristors must be fully biased to the R_{OFF} state. Total resistance of the memory cell is $2R_{OFF}$.
- In state ‘1’, both memristors must be in the R_{ON} state. So, the total resistance of the memory cell is $2R_{ON}$ i.e. a very low value compared with the resistance in state ‘0’.
- For state ‘2’ (i.e. the don’t care state), one memristor must be in the R_{ON} state, while the other memristor must be in the R_{OFF} state. Therefore, the total resistance of the TCAM cell in state ‘2’ is $R_{OFF} + R_{ON}$. As the value of R_{OFF} is significantly larger than R_{ON}, the total resistance of state ‘2’ TCAM is approximately equal to R_{OFF}, i.e. a value in the middle of the range between those for state ‘0’ and state ‘1’.

Next the detailed treatment of the write and matching operations of the proposed TCAM cell are presented.

A. Write Operation

The proposed TCAM cell has two memristors connected in series. The write operation consists of two distinct parts. In Figure 1 the write line (WL) is high during the write operation, data is provided through bit line 1 (BL1), bit line 2 (BL2) and input 3 line (in3) as follows.

1) Write ‘0’

To write a ‘0’, both memristors have to be in the R_{OFF} state. Then, WL must be enabled (ON or high), while BL1 and in3 are low and high, respectively. During the first part of the write operation, BL2 is low and therefore mem2 is in the R_{OFF} state. In the second part of the write operation, BL2 is high for mem1 to be in the R_{OFF} state. Hence at completion of this process, both memristors are in the R_{OFF} state.

2) Write ‘1’

For writing a ‘1’, both memristors must be in the R_{ON} state. This is similar to the write ‘0’ operation; so, WL is high. BL1 is also high, while in3 is low. BL2 is low during the first part of the write operation, so that mem1 is in the R_{ON} state. During the second part of the write operation, BL2 is high such that mem2 is in the R_{ON} state also. Hence, both memristors are in the R_{ON} state.

3) *Write‘2’*

In this case, one memristor must be in the R_{ON} state while the other memristor must be in the R_{OFF} state. So the write line is high, while BL1, BL2, in3 are low, high and low respectively. Therefore, mem1 is in the R_{OFF} state and mem2 is in the R_{ON} state

B. Search Operation

The search operation in a TCAM cell checks whether there is a match between the searched (provided as input) and stored

data. Two match lines (MLL and MLR) are used (Figure 1); these two lines are shown to better understand the operations of the proposed TCAM cell and the discharge process; in practice these two lines can be combined into a single line. The search operation starts by pre-charging the voltage on MLL and MLR to high. Then, the searched data is input through BL1 and BL2. A high voltage (V_{DD}) is applied from in3 to both mem1 and mem2 to compare the data stored in the TCAM cell with the searched data. If the data stored in the TCAM cell is equal (matched) to the searched data, the match line is discharged. Else (no match), its voltage is kept unaltered.

1) Search '0'

The MLs must be pre-charged to V_{DD} prior to starting the search operation. For the search '0' operation, BL1 and BL2 are high and low respectively, i.e. ML1 is ON and MR1 is OFF. Then, the data input is placed through in3 to check the state of the TCAM cell. In Figure 1, each memristor is fully biased to its required state (R_{ON} or R_{OFF}). When a memristor is in the R_{ON} state, the voltage drop across it has a very low value (especially when compared with the R_{OFF} state). The following cases can be distinguished for the search '0' operation.

- If the TCAM cell is in state '0', both memristors must be in the R_{OFF} state, V_X and V_Y are very low (i.e. ML2 is ON and MR2 is OFF). For the search '0' operation, ML1 is ON and MR1 is OFF, a direct path exists from MLL to GND and MLL is discharged.
- For state '2', mem1 must be in the R_{OFF} state and mem2 must be in the R_{ON} state, so V_X and V_Y are low and high respectively. Then, ML2 and MR2 are ON, a direct path from V_{DD} to GND exists via ML1 and ML2; MLL is discharged.
- For state '1', both memristors must be in the R_{ON} state; so during the search operation, V_X and V_Y are high. Then, ML2 and MR2 are OFF and ON respectively. As MR1 is OFF, there is no direct path from V_{DD} to GND; MLL and MLR retain their values, as result of the no-match.

2) Search '1'

For the search '1' operation, BL1 and BL2 are low and high respectively. So, ML1 is OFF and MR1 is ON. Depending on the data stored in the cell, the match line voltages of the proposed cell are as follows.

- If the TCAM cell is in state '0', both memristors are in the R_{OFF} state; therefore, V_X and V_Y are very low (ML2 is ON and MR2 is OFF). There is no direct path from V_{DD} to GND (i.e. no match is found).
- If the TCAM cell is in state '1' or '2', mem2 is in the R_{ON} state and V_Y is high. Therefore, as MR2 is ON, there is a direct path from MLR to GND, thus causing MLR to discharge.

3) Search '2'

For the search '2' operation, the result is always a match because it is the "don't care" state. So, both BL1 and BL2 are high and ML1 and MR2 are ON. A direct path exists from the MLL and MLR to GND, thus always resulting in a match.

IV. Simulation Results

In this section, the performance evaluation of the TCAM cell of Figure 1 is presented using HSPICE at 32nm CMOS technology. The model of [11] is employed for the memristor with a memristance range of 100Ω-19kΩ.

A. Write Time

The write time is the time for the memristor to be in the desired state. By setting the voltage across the memristor to a constant value (equal to 0.9 V), it has been found that the time for fully biasing a single memristor to its state is approximately 200 ns. To fully charge both memristors, the write time can be found as follows (under the assumption that the voltage drop across M1 or M2 is given by 0.45V).

1) Write '0' Operation

For the write '0' operation, both memristors must be in the R_{OFF} state.

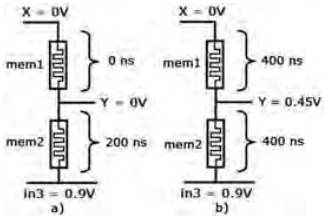

Figure 2. a) First Step of Write '0' Operation b) Second Step of Write '0' Operation

Figure 2 shows the voltages of the TCAM cell of Figure 1 when the write '0' operation is performed. There are two steps for writing a '0': (1) the first step is used to bias mem2 to R_{OFF}, (2) the second step is used to bias mem1 to R_{OFF}. From Figure 2, the time required for both memristors to be in the correct states is given by 600 ns (200 ns for the first step and 400 ns for the second step).However, if the voltage drops across a transistor is reduced (V_Y is increased to 0.72V), the time for the write '0' operation increases. The first step of the write '0' operation takes 200ns, while the second step takes 280ns for writing to mem1 and mem2 respectively; so, the total time of the write '0' operation is nearly 480ns.

2) Write '1' Operation

Similar to the write '0' operation, there are also two steps for the write '1' operation. As shown in Figure 3, the first step is used to bias mem1 to R_{ON}, while the second step is used to bias mem2 to R_{ON}. Due to the voltage drops across M1 and M2 in Figure 1, V_X and V_Y are less than 0.9V. When BL1 and BL2 are both high (0.9V), V_X and V_Y drop to 0.45V. The time for the write '1' operation is 800ns (400ns for the first step and 400ns for the second step). To reduce the time for the write '1' operation, the voltage drop across M1 and M2 must be reduced, i.e. increasing V_X and V_Y. When BL1 and BL2 are high, V_X and V_Y are both equal to 0.72V, then the time is 280ns for each step, i.e. the total time of this process is 560ns.

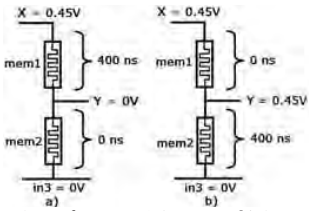

Figure 3. a) First Step of Write '1' Operation b) Second Step of Write '1' Operation

3) Write '2' Operation

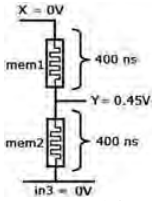

Figure 4. Write '2' Operation

For the write '2' operation (as shown in Figure 4), mem1 must be in the R_{OFF} state, while mem2 must be in the R_{ON} state. Since there is a voltage drop across M2, V_Y is equal to 0.45V. The time for the write 2 operation is 400ns. So, the voltage drop across M2 must be decreased, and V_Y is increased. If V_Y is equal to 0.72V, the time of this operation is 280ns.

From the above discussion, if the voltage drops across M1 and M2 are both 0.45V, the write time (T_W) of the proposed TCAM cell is at most 800ns. However, as the voltage drop is equal to 0.18V (0.9-0.72), then the write time is 560 ns.

Table1. Write time (T_W) of proposed TCAM cell

Current State	*Next State*	T_W *(ns)*
0	1	400
0	2	200
1	0	400
1	2	200
2	0	200
2	1	200

It has been found that the time for changing the memristance from R_{ON} to R_{OFF} is given by 200ns, while the time for changing from R_{OFF} to R_{ON} is given by 165ns. Hereafter, the worst case analysis is pursued, i.e. 200ns is considered. The write '0' ('1') operation requires twice this amount, i.e. 400 ns as shown by simulation in Table 1. The maximum write time occurs when the TCAM cell changes from state 0 to 1 or vice versa, i.e. both memristors must change state, so taking more time than in the other cases.

B. Threshold Voltage Selection

Consider the threshold voltage of ML2, as related to V_X in Figure 1. Simulation has shown that when the TCAM cell is in state '1', both memristors must be in the R_{ON} state, i.e. V_X is nearly equal to V_{DD}. When the TCAM cell is in state '0' or '2' (the total memristance of these states is very high), V_X is just slightly higher than 0V.

For selecting the threshold voltage of ML2, consider V_X during a search operation. V_X slightly increases when mem1 is in state '0' (the TCAM cell is in state '0' or '2'). It is equal to 0.899V if mem1 is in state '1' (i.e. the TCAM cell is also in state '1'). In the proposed design, the threshold voltage of ML2 is set to 0.735V because during the search operation the increase of V_X from 0 to 0.735V is sufficiently large to allow the match line to discharge.

For the threshold voltage of MR2, MLR is discharged if '1' or '2' is searched in the TCAM cell. If the data in the TCAM cell is '1' or '2', mem2 is in the R_{ON} state; then during the search operation, V_Y is approximately equal to V_{DD} (0.899V in this case). So, the threshold voltage of MR2 can be selected to be any value lower than the supply voltage; hereafter the threshold voltage of MR2 is selected to be 0.735V to allow the match line to discharge as ML2. If the search '1' or '2' operation occurs, MLR is then discharged.

C. Search Operation

The search operation for the TCAM cell of Figure 1 is simulated. The match lines MLL and MLR are separate to show the result of the match operation on both sides of the TCAM cell. The match/mismatch outcome of TCAM cell is generated by combining these two lines together into a single line (i.e. the output of an AND gate with MLL and MLR as inputs).

Table 2. Simulation results of the search operation in the TCAM cell; *D* denotes a discharged match line and *S* denotes a stable (unchanged) match line, T_S is the search time of proposed TCAM design

Search	*TCAM State*	*MLL*	*MLR*	*MLL∩MLR*	*Output*	T_S *(ns)*
0	***0***	D	S	D	*Match*	*7*
0	***1***	S	S	S	*No-Match*	*N/A*
0	***2***	D	S	D	*Match*	*7*
1	***0***	S	S	S	*No-Match*	*N/A*
1	***1***	S	D	D	*Match*	*8*
1	***2***	S	D	D	*Match*	*7*
2	***0***	D	S	D	*Match*	*7*
2	***1***	S	D	D	*Match*	*7*
2	***2***	D	D	D	*Match*	*8*

Consider next the search time; the search time depends on the discharging rate of the match lines. Table 2 shows the search time (T_S) in the proposed TCAM cell; the simulation results show that the search time of the proposed TCAM cell is at most 8ns (i.e. less than the 12ns required for reaching the threshold level of a memristor [8]). So during the search operation, the memristors keep their states.

D. Transistor Sizing

The design of the proposed TCAM cell has been evaluated using different feature sizes. The simulation results are shown in Table 3 for different technology scaling. At the same supply voltage, the write time at 32nm is less than at 45 and 65nm; moreover as shown in Figure 5, when the supply voltage is increased, the write time of the proposed TCAM cell decreases. Since the voltage across a memristor is increased, the rate of change in memristance is also faster. Therefore, the write time at a higher supply voltage is lower.

As for the search time, the simulation results in Table 3 show that the search time at 32nm is less than at 45 and 65nm; however at the same scaling, the simulation results show that the search time is higher at a higher supply voltage. This occurs because the match lines will take longer to completely discharge. Also, a memristor slowly changes its voltage as

result of a search operation; however as shown in Table 3, the search time is less than the time for reaching the threshold level, so a state change cannot occur.

Table 3. Comparison between transistor size and write time for a memristor range of 100Ω – 19kΩ

Technology	*V_{DD} (V)*	*Write time (ns)*	*Search time (ns)*
32nm	1	270	6.08
	1.1	210	6.28
45nm	1	300	6.70
	1.1	230	7.20
65nm	1	330	6.81
	1.1	270	7.30

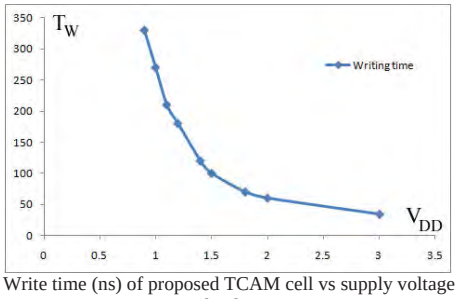

Figure 5. Write time (ns) of proposed TCAM cell vs supply voltage at 32nm technology

The simulation results in Table 3 and Figure 5 show that the proposed TCAM cell can be implemented at 32nm with a low write time. Also correct operation is achieved, because its search time is faster than the time required for reaching the threshold level of the memristor. The rate of change of the memristors is very low if the supply voltage is reduced at low scaling (the supply voltage of 32nm is less than for 45nm and 65nm). This feature is also advantageous for power dissipation as at 32nm, less power is also required.

V. Discussion

In this section, several tradeoffs in TCAM cell design are presented. The state of a memristor may change during the search operation, thus resulting in an incorrect output. To avoid this from resulting in an erroneous outcome, the following tradeoffs must be considered in the design of the cell.

A. Memristor Range Vs Write Time

Consider the write time, i.e. the time to fully bias each memristor to its state; if the memristor range is large, the write time could be large. Since the memristor can change its state during the search operation, the number of search operations could be large too if it has a large memristance range (provided the threshold level of the memristor is not taken into account).

B. Transistor Size (M1 and M2) Vs Write Time

When the size of these transistors is increased, the voltage drop across them decreases. Therefore, V_X and V_Y of the TCAM cell in Figure 1 during the write operation increase; hence, the write time decreases.

C. Transistor Size (M1 and M2) Vs Search Time

When the size of these transistors size is increased, the discharge of the voltage from MLL and MLR to GND will be faster, thus resulting also in a faster search time.

D. Memristance Range Vs Search Time

The search time corresponds to the time that MLL or MLR completely drops from the current value to GND; so if the rate of increase of V_X during the search operation is higher than the decreasing rate of the match line, the match line will not completely discharge, thus resulting in a wrong output. Hence, the memristance range must be large, such that the rate of increase of V_X will be slower (and the match line will have more time to discharge).

E. Supply Voltage Vs Search Time

If the supply voltage is increased, the search time will also increase as at a higher value of supply voltage, a match line will require more time to fully discharge its value (V_{DD}) to GND.

VI. MCAM Operation

In this section, the TCAM design of Figure 1 is extended to MCAM operation and compared with the cell of [8]; a MCAM cell stores data (‘0’ and ‘1’), and searches (for ‘0’, and ‘1’) to perform a match/no-match operation. In this section, two approaches are presented for operating as a MCAM cell.

The first approach utilizes the proposed TCAM cell unchanged, i.e. the same operations as discussed previously are used to store and search ‘1’ and ‘0’ as data. In this case, for writing ‘0’ (‘1’), both memristors must be in the R_{OFF} (R_{ON}) state. By using the same search operation as outlined previously, the write time of the TCAM cell is slower than for the MCAM cell of [8], because two clock cycles are required to completely bias both memristors to the desired states (as shown previously).

To improve the write time, a modification is required to the cell; since a MCAM cell stores only a bit (‘0’ or ‘1’), so the second approach proposed for MCAM operation changes the proposed TCAM cell, such that only one memristor is needed. In this case, mem1 must be in the R_{ON} state, while mem2 is in a state depending on the write operation. As the memristance of R_{ON} is very low, then V_X and V_Y are very close. So for the search operation, V_X and V_Y depend on mem2 as follows.

- If mem2 is in the R_{OFF} state, during the search operation, V_X and V_Y are both low.
- If mem2 is R_{ON}, then V_X and V_Y are approximately equal to V_{DD}

Therefore, the MCAM operation can be accomplished by using the search ‘0’ and ‘1’ features of the TCAM.

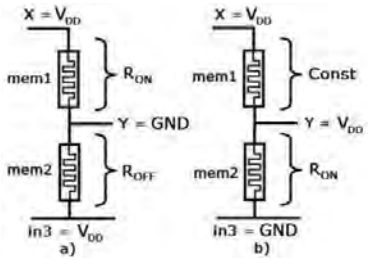

Figure 6. a) Write '0' Operation b) Write '1' Operation

Figure 6 shows the write operation of the TCAM cell by operating as a MCAM cell. By forcing BL1 to V_{DD}, mem1 is placed in the R_{ON} state or kept at the same (constant) value. By adjusting the voltage at BL2 and in3 to control the memristance of mem2, the data ('0' and '1') is written in the TCAM. The write time of the proposed TCAM is the same as the MCAM of [8] so requiring only one clock cycle.

Next, a comparison is pursued between the proposed TCAM cell when operated as MCAM and the MCAM cell of [8].

A. Voltage Supply

The MCAM of [8] requires two voltage supplies (V_{DD} and $\frac{V_{DD}}{2}$) while the proposed TCAM uses only V_{DD}; an additional circuitry for generating half V_{DD} is therefore required for the MCAM design of [8]. Moreover these cells utilize different voltages for V_{DD} : the supply voltage of the MCAM is 3V while the TCAM is only 0.9V (based on CMOS technology).

B. Power Dissipation

The power dissipation of the proposed TCAM is significantly less than the MCAM of [8] due to the lower supply voltage that it is used. Moreover, the number of transistors in the proposed TCAM cell (6T) is less than the MCAM (7T) thus resulting in a lower power dissipation. When compared with a 5T MCAM, the proposed TCAM cell (6T) uses a lower number of input lines (5 lines), thus resulting in a lower noise during the write and read operations.

C. Write/Search Times

When comparing the proposed TCAM operation with the MCAM, the write time of the proposed TCAM cell is higher than for the MCAM cell of [8] because two memristors are connected in series. For the search operation, simulation has shown that due to the lower supply voltage, the search time of the proposed TCAM cell (at most 8ns) is less than the one for the MCAM (12ns). However when comparing the proposed TCAM for CAM operation and the MCAM of [8], by simulating at the same power supply, the write time of the proposed TCAM is less than the MCAM because the voltage across the memristor is higher than for the MCAM. The write time of the proposed TCAM (when used as CAM) is faster than the MCAM of [8]

VII. CONCLUSIONS

This paper has presented a Ternary Content Addressable Memory (TCAM) cell design by using memristors as storage element. Since ternary logic is used, two memristors connected in series are utilized to represent each state of the TCAM. The proposed TCAM has been extensively analyzed by considering memristance range, threshold voltage, transistor size and supply voltage with respect to memory operations such as write and search. The proposed memory cell operates robustly and design considerations involving memristance range and threshold selection have been analyzed to achieve fast operation for writing and searching at 32nm feature size. Simulation results using HSPICE have confirmed that the proposed design offers significant performance improvements compared with other CAM designs utilizing memristors.

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