Abstract— A novel accumulation-mode MOS varactor model used for characterizing the tuning curve of LC-tank voltage-controlled oscillators (VCOs) is presented. The VCO tuning characteristic is seen to depend not only on the C-V characteristics of the varactor but also on losses in the tank. Effects of variations in the tank quality factor (Q) and oscillator’s swing on the VCO tuning curve are discussed. Also a practical SPICE model using a pMOS transistor to describe an accumulation-mode MOS varactor is proposed. The model has been verified in a number of structures manufactured in a standard 0.13µm CMOS process and is suitable for simulation within many circuit design environments.

I. INTRODUCTION

Voltage-controlled oscillators (VCOs) are the heart of many important blocks such as phase-locked loops (PLLs) and clock/data recovery modules (CDR) used in today’s state-of-the-art telecommunication systems. While different VCO implementations such as LC-based, ring and relaxation have been proposed in the literature [1-3], LC based oscillators are still among the best VCOs from the phase noise performance perspective. However, they require careful modeling of their tuning range, which is inherently small.

High performance LC oscillators require low-loss varactors and a wide tuning range. MOS based varactors are becoming increasingly popular over the reversed-biased diode varactors as their equivalent quality factor (Q) improves with every new process generation. This improvement is due to higher doping levels in silicon. Reduced resistive losses result in VCOs with lower power consumption and lower phase-noise. Furthermore, a study on two types of MOS varactors, accumulation-mode and inversion-mode, reveals that VCOs based on the accumulation-mode varactor demonstrate the lowest power consumption and the lowest phase-noise at large offset frequencies from the carrier [4].

Recently, a lot of effort has been placed on modeling C-V characteristics of the MOS varactors, partly due to increasing popularity of CMOS LC VCOs. Some models are based on physically meaningful parameters, which describe the characteristics of the device with different equations for different regions of the varactor operation [5]. However, simulating and using these types of models is not simple in SPICE or similar simulators as they require defining mathematical functions inside the tool. Others have developed models, which are based on sub-circuits utilizing BSIM SPICE models [6]. These models are suitable for simulator implementation within the circuit-design environment and can be easily adapted for future technologies.

C-V characteristics of the MOS varactor can be predicted using 2D/3D numerical simulators. Unfortunately, these simulation tasks require precise knowledge of the underlying doping profiles, which is rarely available. The alternative way is to perform capacitance measurements. However, the measurements of sub-pico Farad capacitances are difficult and requires fairly expensive S-parameter RF measurement set-up. It is therefore, very useful to have the ability to predict the tuning characteristics of the LC based oscillators using standard foundry supplied models for MOS FETs.

This paper is organized as follows: the VCO architecture and the comparison between the measured tuning range and simulated tuning range are discussed in Section 2. Varactor modeling and VCO tuning range calculation are described in Section 3. In section 4, implementation of three different VCOs in a standard 0.13µm CMOS process is reviewed, and the simulated tuning curve using the proposed model is compared to measurement. The concluding remarks follow in Section 5.

II. VCO DESIGN AND TUNING CHARACTERISTICS

In this work, a standard VCO circuit with current source isolating the core of the oscillator from the power supply is used as shown in Fig. 1. The structure is designed for 5-6GHz operation. Inductance L is 1.5nH and varactor capacitance is in the range of 0.6pF to 1.4pF.
It may seem that modeling of the tuning characteristics is a straightforward task as the oscillation frequency is given by the following well-known formula:

$$f_{osc} = \frac{1}{2\pi\sqrt{L \cdot C(V)}}$$

(1)

where $L$ is the inductance and $C(V)$ is the equivalent capacitance for a given biasing point. However, we have performed a simple test to indicate that the modeling process is more involved as it would seem. From the measured tuning characteristics (the experimental devices are described later in this paper) the equivalent capacitance can be extracted using (1):

$$C(V) = \frac{1}{4\pi^2 f_{osc}^2 L}$$

(2)

Having $C(V)$ values, an extracted piece-wise linear model of the voltage-dependent capacitance was reconstructed and fed back to SPICE for simulation. The results of such a comparison, shown in Fig. 2 indicate discrepancies up to 7%.

These discrepancies can be attributed to the effective varactor capacitance. The varactor capacitance gets modulated in time with the large signal swing of the oscillator output, which in turn changes the effective capacitance of the tank [7-9]. We used a method similar to the one reported in [7] to calculate the effective capacitance. In our calculations, we neglect the current components at harmonics of $f_{osc}$ as they play a small role in determining the frequency of oscillation. Equation (3) is the revised version of (1), used to obtain the VCO’s tuning characteristic:

$$f_{osc} = \frac{1}{2\pi \sqrt{L \cdot (C_{av}(V) + C_{par})}}$$

(3)

In this equation, $C_{par}$ is a fixed parasitic capacitance and $C_{av}$ is the average capacitance calculated according to method described in [7]. The average capacitance is the rms value of varactor’s current, $i(t)$, divided by the rms value of $dV/dt$ where $V(t)$ is the voltage across the varactor.

As shown in Fig. 3, if the voltage swing is small (compared to nonlinearities of the C-V characteristics), then the equivalent large signal C-V characteristics closely resemble its small signal counterpart. However, for large values of the voltage swing the equivalent characteristics gets smoothed or averaged over larger voltage range. As a result, the tuning characteristic becomes dependent on the voltage swing that in turn is affected by the magnetic and resistive losses in the tank.
Calculation of the equivalent large signal C-V characteristics depends on the shape of the oscillator’s output (rectangular, sinusoidal, etc.). However, at high frequencies, the current waveform can be approximated by a sinusoid due to the finite switching time and limited gain [10]. Equation (4) shows the relationship between the swing and tank losses in this LC VCO:

\[ V_{\text{tan}k} \approx I_{\text{tail}} \cdot R_{\text{loss}}, \quad (4) \]

where \( R_{\text{loss}} \) is the equivalent parallel resistance of the tank and \( I_{\text{tail}} \) is the source/drain current of the current source transistor (M5 in Fig. 1). The effective C-V characteristics (Fig. 3) and their associated VCO tuning curves are obtained using (3) and (4) and the method proposed in [7].

III. VARACTOR MODELING

As indicated above, modeling of tuning characteristics using (1) becomes very complicated; because not only the varactor C-V characteristics have to be measured, but also the losses of the tank have to be determined to properly find the oscillation swing and hence, the effective tank capacitance. An alternative approach would be to use the equivalent circuit representation of the varactor created from foundry supplied transistor models and SPICE simulation to predict the tuning range. If a varactor is operating in the strong inversion mode, a transistor with tied source and drain can be used as a primitive model since the varactor structure is the same as a MOS transistor. However, varactors that are working in the accumulation mode are usually laid out as shown in Fig. 4. This structure guarantees that the formation of the strong, moderate and weak inversion regions is inhibited. Wider tuning range and lower parasitic resistance are other advantages of this implementation [4]. On the other hand, the use of a plain transistor for modeling this varactor is not viable because the device does not resemble a transistor.

Fig. 5 illustrates the model of this varactor constructed with passive circuit elements, which is based on physical parameters [5]. As mentioned above, using this model requires implementation of non-straightforward equations (e.g., hyperbolic tangent) in the circuit-design environment and may involve other approximations as well. Moreover, the model cannot be easily scaled to future technologies.

We have considered a number of different equivalent models available in the literature and developed a new model that can closely approximate the measured characteristics of the VCO. This improved model is shown in Fig. 6. This model is a modified version of the one proposed in [6].

To model the varactor capacitance, the equivalent circuit contains a voltage source \( V_{\text{offset}} \), a capacitor \( C_{ov} \) and a pMOS with its source and drain connected to the ground with a high impedance (e.g., \( 1 \Omega \)) or a negative power supply is used. The open circuit for the source/drain terminal is required to eliminate the inversion layer capacitance that is present in the channel of the pMOS but absent in the varactor structure (Fig. 4). As a result, the gate to n-well (bulk) capacitance of pMOS represents the
varactor capacitance properly with an additional channel length correction for LDD (Lightly Doped Source/Drain) regions. Unfortunately in this configuration, the gate-source and gate-drain overlap components of the varactor get neglected; so they have to be added back by using the fixed capacitor, $C_{oc}$. $V_{\text{offset}}$ represents a difference of the metal-semiconductor work function $\Phi_{MS}$ as the pMOS has p+ poly gate doping while the varactor has n+ poly doping due to their different source/drain diffusion. As doping levels in the polysilicon layer are typically close to degeneration the $V_{\text{offset}}$ is close to silicon bandgap ($E_g/q$), which is about 1.1V at room temperature. Finally, the junction capacitance of the pMOS transistor has to be scaled down. This can be done either by changing the scaling factor inside the SPICE model or adding a negative power supply between source/drain and the bulk (e.g., -5V) so as to enlarge the depletion area and reduce the junction capacitance.

IV. CMOS IMPLEMENTATION

Three different VCO structures have been fabricated in a standard 0.13µm CMOS process with 1.2V power supply. No special mixed-signal process options have been used. Varactors are implemented as n+ accumulation-mode MOS capacitors with no additional mask required. Thus, the obtained designs are portable to various CMOS processes of different foundries.

The three implementations have similar architecture as Fig. 1 but with different varactor values and different location for the tail current (pMOS or nMOS tail current sources). The one that incorporates an nMOS tail current source (Fig. 1), exhibits higher sensitivity to the power supply noise, while the one with pMOS tail current source (not shown here) has the smallest PSRR due to the extra isolation from the power supply by the current source.

In addition to three VCO circuits, a biasing circuit and an output driver stage was added to drive external 50Ω load.

Individual varactor and inductor test structures have also been included for S-parameter measurements. Open and short de-embedding structures are added for proper extraction of the equivalent circuit.

The tuning characteristics were simulated using the varactor model described in the previous section. Excellent agreement between the model and the measurement has been obtained as shown in Fig. 7.

V. CONCLUSIONS

A new model for CMOS accumulation-mode varactor is presented. The model is used to predict the tuning curve of the LC VCOs. It has been shown that the shape of the tuning curve and the effective varactor capacitance depend on the losses of the tank. The model is SPICE-based and has been verified experimentally in a standard 0.13µm CMOS process with different VCO structures.

ACKNOWLEDGMENTS

The authors would like to thank Roberto Rosales of the University of British Columbia and Mark Hiebert of PMC-Sierra for assisting with the measurement. They would further like to acknowledge the collaboration of Marek Syrzycki of Simon Fraser University.

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