Analog Decoding: State of the Art

Christian Schlegel – Christopher Winstead

Department of Electrical Engineering
University of Alberta
Edmonton, AB, CANADA
Email: schlegel@ee.ualberta.ca

International Symposium on Spread Spectrum Techniques and Applications
Sydney, Australia, August, 30 – September, 2, 2004

supported in part by iCORE Alberta
The Dawn of Analog Decoding?

Advantages of Analog Decoding

• High level of computational parallelism enables high-throughput enabling technology.
• Subthreshold operation allows for extremely low-power devices.
• Performance of the decoder is controllable in a wide range.
• CMOS designs allow fabrication using all-digital processes.
• Device and process mismatches have little effect on performance.

Challenges of Analog Decoding

• High-speed analog input and output interfaces need to be built reliably.
• Built-in self testing of devices needs to be researched.
• Automated design and test procedures do not exist.

Achievements

There are indications that analog decoding can save more two orders of power consumption in high-complexity advanced error control decoders:

![Graph showing required SNR vs. power dissipation for different types of decoders.](image)
**Basic Principle: The Translinear Loop**

**Translinear Principle:**
In a closed loop consisting of translinear devices with equal numbers of clockwise and counter-clockwise currents, the product of currents in the clockwise direction is equal to the product of currents in the counterclockwise direction.

![Diagram of translinear loop](image)

**Enabling Device: MOS FET**
It is operated in the sub-threshold saturated region

\[ I_{DS} \approx I_0 \frac{W}{L} \exp \left( \frac{\kappa V_{GS}}{U_T} \right) \]

Analog Decoding: State of the Art
International Symposium on Spread Spectrum Systems and Techniques 2004, Sydney, Australia
**Basic Circuits: MOS Translinear Loops**

**Current Multipliers:**

\[ I_2 = \frac{I_1 I_B}{I_1 + I_4}; \quad I_2 = \frac{I_2 I_B}{I_1 + I_4} \]

**Normalization:**
- The current \( I_B \) represents unit probability one.
- \( I_2, I_3 : I_2 + I_3 = I_B \) represent complementary bit probabilities.

The Gilbert multiplier calculates all possible products:

\[ I_{ij} = X(i)Y(j) \]

**Gilbert Multiplier** forms the basic computational cell for the analog processing blocks:
LDPC – Analog Design

Low-Density Parity-Check Codes: are graph based powerful error control codes

LDPC have two types of nodes, which execute the following

Processing Rules:

Equality:

\[
\lambda_{out} = \sum_{i} \lambda_{i} + \lambda_{ch}
\]

Parity:

\[
\lambda_{out} = 2 \tanh^{-1}\left(\prod_{i} \tanh\left(\frac{\lambda_{i}}{2}\right)\right)
\]

Parity-Check Node:

\[
Z(0) = X(0)Y(0) + X(1)Y(1)
\]

\[
Z(1) = X(0)Y(1) + X(1)Y(0)
\]

Equality Node:

\[
Z(0) = X(0)Y(0)
\]

\[
Z(1) = X(1)Y(1)
\]
Input and Output Stages

**Input Stage**
The signals have to enter the decoder as LLR values:

\[
\text{LLR} = \log\left( \frac{\Pr(x = 1|y)}{\Pr(x = 0|y)} \right) = \frac{4y}{N_0}
\]

The differential stage converts LLRs in probability currents:

\[
\log\left( \frac{I_{\text{out}_1}}{I_{\text{out}_0}} \right) = \alpha (V_1 - V_2)
\]

**Output Stage**
Probability currents have to be converted into LLRs for decision making:

\[
\Delta V = \exp\left( \frac{I_{\text{out}_1}}{I_{\text{out}_0}} \right) = \lambda
\]

A comparator makes a sign decision on the LLR outputs.
The complete decoder comprises a differential analog input line, serial-to-parallel conversion, and a parallel-to-serial output line:
Experimental Decoder – (256,121) Product Code

Chip Layout Photo:

Chip Data:
- Built in TSMC 0.18 micron process
- Die size is 2.3mm by 2.5mm
- Fabricated through CMC's University program
- Area: 4mm squared

Measurement Behavior:
Measurements were carried out with a custom-built FPGA-based test setup, with importance sampling capabilities.

- Error Floor is due to interface electrical limitations
- Performance is better than that of a digital decoder
Analytical Verification

**Density Evolution:**
is used to verify proper core functioning

![Diagram of Density Evolution](image)

**Numerical Results:**
show that transistor mismatch has only a very minor impact on performance as long as it is not too severe (< 25%)

The LLR are assumed to be Gaussian, their means are numerically calculated:

\[ \mu_z = \int f(x, y, \varepsilon)p_G(x)p_G(y)p_G(\varepsilon)dx dy d\varepsilon \]

Mismatch Model:
\[ I_2 = (1 + \varepsilon)I_1 \]
## Promise of Analog Decoding – Power and Size Efficiency

Analog Decoders have the potential to be extremely power efficient:

<table>
<thead>
<tr>
<th>Who</th>
<th>Technology</th>
<th>Power</th>
<th>Throughput</th>
<th>Energy/Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gaudet et. al. JSSCi’03</td>
<td>0.35 micron</td>
<td>185mW 3.3V</td>
<td>13.3 Mbits</td>
<td>13.9nJ/b</td>
</tr>
<tr>
<td>Winstead et. al. JSSCi’03</td>
<td>0.5 micron</td>
<td>45mW 3.3V</td>
<td>1 Mbit</td>
<td>45nJ/b (core/IO)</td>
</tr>
<tr>
<td>Blanksby et. al. JSSCi’02</td>
<td>0.16 micron</td>
<td>690mW 1.5V</td>
<td>500 Mbits</td>
<td>1.26nJ/b</td>
</tr>
<tr>
<td>Moerz et. al. JSSCi’02</td>
<td>0.25 micron</td>
<td>20mW 3.3V</td>
<td>160 Mbits</td>
<td>0.125nJ/b</td>
</tr>
</tbody>
</table>

| (16,11)$^2$ product code    | 0.18 micron| 7mW 1.8V   | 100 Mbits  | 0.07nJ/b (core/IO) |
| (16,11) Low voltage        | 0.18 micron| 0.036mW 1.8V | 4.4 Mbits | 0.008nJ/b        |

### Remaining Issues:
- The interface is an analog VLSI design challenge — high-speed, sufficient accuracy is required.
- Testing of chips needs to be automated
- Design tools are non-existent
- Integration with SOC needs more work
- Key test applications are needed to spearhead insertion