which can be inverting (like that connected to $x_3$) or non-inverting (like that connected to $x_4$).\(^1\)

When $\phi_1$ is high, the values of the outputs $x_i$ of the 'neurons' are sampled on to the capacitors. While these capacitors hold these values, $\phi_2$ goes high and the output of the neurons is zeroed. Then, when $\phi_2$ goes high, the input capacitors are switched to virtual ground, transferring the charge of one of their plates on to the left-hand plate of capacitor $C$. As long as the inverter operates in its linear region, charge conservation dictates that the output $x_3$ is given by the sum inside the brackets in eqn. 1, multiplied by $\beta$. If the value of this quantity exceeds the saturation limits of the inverter, nonlinearity takes over and the sigmoid function $f(t)$ is automatically implemented. The 'gain' of the sigmoid can be set large enough by choosing $\beta$ appropriately (see Figs. 1 and 2).

The circuit of Fig. 2 has been computer-simulated and was found to work as desired; a simple two-transistor CMOS inverter was employed for simplicity. Several neurons can be interconnected as shown in Fig. 3. Stable states can be programmed into the network using a variety of rules (many of 'neurons' are sampled on to the capacitors. While these capacitors hold these values, their behaviour as associative memories was investigated by computer circuit simulation. The network initial states were set by forcing voltages on to the feedforward capacitors through switches (not shown). The networks worked as expected from theory.\(^1,5\)

Fig. 3 Neural network using neurons of type shown in Fig. 2

The implementation proposed above appears to have a number of advantages. First, it implements directly discrete-time neural networks, which may have interesting properties of their own and which are much easier to analyse by programming eqn. 1 on a computer (as opposed to simulating continuous-time neural networks, which are characterised by nonlinear differential equations). Secondly, no loop is ever closed; there is no continuous-time feedback at any instant, so the possibility of unwanted continuous-time oscillations is avoided. Thirdly, the discrete-time implementation of the neurons may allow for reducing the number of interconnections at the expense of speed (which is very high anyway\(^6,7\)). In general, $N$-neuron networks could have up to $N^2$ interconnections. However, many of the direct connections between neurons can be omitted and the connection 'traffic' can be redirected through the connections of other neurons. The state of such neurons can be temporarily stored on capacitors while such traffic is being handled.

Conclusions: The neural networks field is far from being mature, and it is difficult to know what will eventually prove to be relevant and/or interesting, even as far as principles are concerned (let alone VLSI implementations). We have, however, shown that discrete-time neural network forms which are of interest today can be implemented using switches, capacitors and inverters. The techniques used are akin to those used in switched-capacitor filters, but in addition take advantage of the inherent saturation of the inverters, to implement the neuron nonlinearity without using additional elements. A number of potential advantages of the proposed circuits have been pointed out. It is felt, though, that the proposed technique is but one example of the way in which analogue MOS circuit techniques, accumulated over the past decade, can help in implementing neural network circuitry, or, more generally, analogue circuitry for artificial intelligence.\(^5\)

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MEASURED PULSE-STUFFING JITTER IN ASYNCHRONOUS DS-1/SonetMULTIPLYING WITH AND WITHOUTSTUFF-THRESHOLD MODULATION CIRCUIT

Indexing terms: Telecommunications, Jitter, Multiplexing, Pulse-stuffing jitter, SONET format

The letter reports the measurement of pulse-stuffing jitter levels up to 0.2 UI\(_{max}\) when an asynchronous DS-1 is transported in the current draft-standard SONET format. We then describe a new circuit technique for jitter suppression which does not require format alteration, and report measured jitter reductions of 10-16 dB for asynchronous DS-1/Sonet multiplexing. We offer an explanation as to why the jitter is not significantly reduced by recent SONET format rearrangements, and show illustrative jitter spectra demonstrating the operative principle of our jitter reduction circuit.

Introduction: The purpose of this work is to reduce the jitter introduced by asynchronous pulse-stuffing multiplex techniques without requiring any changes to certain new formats such as SONET and SYNTRAN. The goal is to permit these formats to carry asynchronous (as well as synchronous) payloads while retaining a format which is optimised for synchronous applications. Without the advent of these formats there would be little motivation for new methods of jitter reduction, because asynchronous multiplex jitter has, to date, been easily held to low levels through design techniques which are based on control of the nominal stuff ratio according to Duttweiler.\(^1\)

In such systems the desired stuff ratio is traditionally obtained at design time by appropriate selections of the line frequency and of the multiplex frame repetition rate (strictly, by selection of the stuff-opportunity rate with respect to the difference between the nominal tributary rate and the internally synchronous multiplex tributary rate). It is in this regard that SONET and SYNTRAN introduce an important new constraint in the asynchronous multiplex design problem. The
new constraint is that the multiplex frame period is fixed at 125 μs by the requirement for minimum-cost synchronous applications. In SONET, the time between stuff opportunities is consequently an interval of time during which a nominal DS-1 tributary produces exactly 193 data bits. However, any nominally integer number of payload bits per stuff opportunity is the condition for the worst-possible nominal stuff ratio (namely zero or one) in the theory by Duttweiler.¹

Some workers² have attempted to address this problem through SONET format rearrangement as a means to achieve an apparently improved stuff ratio for the transport of asynchronous DS-1s. The current format proposal incorporates such an attempt, and it must therefore be discussed. The draft SONET version³ which we have prototyped uses a seven-frame superframe for the DS-1 payload mapping in which odd-numbered frames carry 193 data bits, six overhead bits and one stuff opportunity bit, while even-numbered frames carry 192 data bits, seven overhead bits and a stuff opportunity bit. The format was proposed because it was thought to have a stuff ratio of 4/7, yielding some jitter reduction.² However, it can be seen by inspection that odd frames have a nominal stuff ratio of one (a ‘stuff’ is the insertion of a dummy bit in to the stuff opportunity), while even frames have a nominal stuff ratio of zero. Simulation of this format has confirmed that indeed four of the seven stuff opportunities in the above superframe are nearly always seized and the other three are almost never seized.⁴ Therefore, despite the average stuff seizure rate of 4/7, this is really an interleave of a unity-stuff-ratio process and a zero-stuff-ratio process, still equivalent worst cases from the viewpoint of jitter. In addition, such format rearrangements undermine the goal of minimum complexity for synchronous applications, the main purpose for the SONET format.

Accordingly, because neither the DS-1 line rate nor the SONET frame rate can be changed to achieve an improved stuff ratio for asynchronous DS-1/SONET multiplexing, and because format rearrangement is both undesirable and apparently ineffective, we have been motivated to invent a new method for jitter suppression which is not based on format rearrangement or on the fundamental need to control stuff ratio.

**Experimental method**: A prototype synchroniser, multiplex control logic and desynchroniser were constructed according to well known asynchronous multiplex design techniques but designed specifically for the DS-1/SONET application. The conventional synchroniser structure is shown in Fig. 1, with the switch in position (a). The prototype control logic and synchroniser map an asynchronous DS-1 test signal into the SONET format described in Reference 2. The conventional demultiplex logic (not shown) feeds a standard desynchroniser with deinterleaved data and the corresponding gapped clock. The desynchroniser is a PLL elastic store with a single-pole rolloff in the phase transfer function giving approximately 100 Hz jitter noise bandwidth. In each experiment an initially jitter-free DS-1 test signal was slowly swept across the allowable range of asynchronous DS-1 frequencies (1-544 MHz ± 200 parts in 10⁶) and, at each frequency offset from nominal, the RMS jitter of the desynchronised DS-1 signal was measured. The procedure was first performed with the conventional synchroniser and then with a synchroniser circuit modified to implement our jitter-reducing circuit modification (described next). No format changes were made between the two measurements and the same demultiplex and desynchronisation circuits were used in both cases.

**Description of jitter-reducing synchroniser**: The jitter-reducing synchroniser is obtained by a simple modification of the conventional synchroniser. In our experiment this was performed by connection of the circuitry shown in the broken-line box of Fig. 1 to the reference input of the stuff-request comparator (switch position (b)) to create a sawtooth-modulated stuff-request decision threshold as opposed to the usual constant threshold. The threshold modulation waveform was a sawtooth with peak amplitude equivalent to one bit time (one UI) of phase, applied over a period of seven frames. The threshold modulation period was not synchronised to the seven-frame superframe defined in Reference 2.

The conceptual basis for the modified synchroniser is the possibility of achieving a frequency-domain upconversion effect on the jitter spectrum that results from the variable delay due to the pulse-stuffing method of synchronisation. When jitter upconversion is successfully introduced at the synchroniser, the net jitter imparted to a multiplexed tributary may be significantly reduced, if the upconversion effect places dominant jitter components out-of-band of the desynchroniser. We verified the feasibility of this principle through computer simulation of the SYNTRAN⁵ format (the jitter problem is similar in SYNTRAN). Once certain capture effects and modulation waveform dependencies were understood, we were able to repeatably obtain the clear demonstration of jitter spectral shifting that is shown in Fig. 2. In this example jitter power in the band below 200 Hz was reduced by 35 dB due to shifting dominant low-frequency jitter tones to frequencies out of the passband of the subsequent desynchroniser. Having confirmed the basic idea through simulation of a similar nominally synchronous format, we proceeded directly to experimental work for the SONET case and obtained the following results.

![Fig. 1 Experimental synchroniser circuit configurations](image)

| a | Conventional | b | With threshold modulation |

**Experimental results**: Fig. 3a presents measured jitter results for the conventional synchroniser design and shows that RMS jitter up to 0-2 UI is produced with the current proposal for asynchronous DS-1/SONET multiplexing, even though arrangements have been introduced to mitigate jitter. 0-2 UI of RMS jitter implies frequent peak phase excursions that exceed the requirement of 0-3 UI peak.⁶ For comparison, the measured jitter of a conventional DS-1/DS-3 multiplex chain is typically 0-025 UIrms or less. Fig. 3b shows that, with the addition of the synchroniser stuff-threshold modulation circuit, the jitter power due to asynchronous DS-1/SONET multiplexing was reduced by over 11 dB at the highest jitter powers, and up to 16 dB elsewhere in the DS-1 frequency.

![Fig. 2 Jitter spectral upconversion due to stuff-threshold modulation](image)

SYNTRAN, 50 Hz DS-1 tributary offset
a With conventional synchroniser (without threshold modulation)
b With 470 Hz sawtooth threshold modulation

**Experimental results**: Fig. 3a presents measured jitter results for the conventional synchroniser design and shows that RMS jitter up to 0-2 UI is produced with the current proposal for asynchronous DS-1/SONET multiplexing, even though arrangements have been introduced to mitigate jitter. 0-2 UI of RMS jitter implies frequent peak phase excursions that exceed the requirement of 0-3 UI peak.⁶ For comparison, the measured jitter of a conventional DS-1/DS-3 multiplex chain is typically 0-025 UIrms or less. Fig. 3b shows that, with the addition of the synchroniser stuff-threshold modulation circuit, the jitter power due to asynchronous DS-1/SONET multiplexing was reduced by over 11 dB at the highest jitter powers, and up to 16 dB elsewhere in the DS-1 frequency.
range. The 11 dB improvement reduces the probability of a peak jitter excursion of 0.3 UI to roughly that of 4e event in the worst case encountered. We expect that further improvements will be obtainable with optimisation.

Conclusion: We have shown experimentally that up to 0.2 UI rms pulse-stuffing jitter results from asynchronous DS-1/SONET multiplexing according to the format in Reference 2. This RMS jitter level implies peak excursions that exceed requirements. To address this problem we have described a circuit technique which achieved 11–16 dB reduction of jitter in an asynchronous DS-1/SONET multiplex prototype, significantly reducing the probability of excessive jitter peaks. The principle of the method is jitter spectral upconversion through modulation of the synchroniser stuff-request decision threshold. The method may be used to avoid changes to the preferred nominally synchronous SONET format, and is compatible with conventional desynchroniser designs. The method may be useful in general where a preferred stuff ratio is not achievable, or to widen the range of tributary offsets that a system can accommodate, or to permit wider-bandwidth desynchronisers in applications where acquisition speed is critical.

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DIRECT INTERFEROMETRIC MEASUREMENT OF NONLINEAR REFRACTIVE INDEX OF OPTICAL FIBRES BY CROSSPHASE MODULATION

Indexing terms: Optical measurement, Optical fibres

We have computed the nonlinear refractive index of optical fibres from the phase shift resulting from crossphase modulation between a probe signal and a pulsed pump. This phase shift is obtained with a Mach–Zehnder interferometer. Values of 0.92 x 10^{-13} esu for silica and 0.80 x 10^{-13} esu for fluorozirconate glasses have been measured.

Introduction: The nonlinear refractive index \( n_2 \) of a material is usually measured via the determination of the phase shift due to self-phase modulation (SPM) suffered by an optical wave after propagation through this material. The first reported experiments for bulk materials used time-resolved interferometry and picosecond pulses. Third-order frequency mixing and self-focusing were also reported. Using long interaction lengths is a suitable means to lower the power required to obtain measurable effects. SPM was observed and measured in single-mode fibres, and induced birefringence (Kerr effect) was measured using linearly birefringent fibres and cross-phase modulation (CPM), the interaction length being in the order of 100 m.

We report in this letter on a new method using a Mach–Zehnder interferometer. The principle of the method consists in increasing the index of refraction of the fibre core by sending a pump pulse in the fibre. The counterpropagating pulsed pump wave induces CPM in the fibre arm, leading to a phase shift detected by fringe shift reading.

Experimental set-up and theory: The experimental arrangement (shown in Fig. 1) consists of a Mach–Zehnder interferometer, the reference arm being an air path. The fibre is inserted in the other arm. The interference level at one output of the interferometer is continuously recorded. Light emitted from a Q-switched Nd-YAG laser is sent at the other output of the interferometer. Variable attenuators and a half-wave plate allow variation of the peak power and the direction of linear polarisation of the pump pulse. Filters in front of the detector block off the residual pump power originating from various reflections in the interferometer. The pump power is measured after propagation in the fibre. When a pump pulse is present in the fibre we observe a variation of the interference level, which is directly proportional to the nonlinear refractive index \( n_2 \) and the pump power. This phase shift is written as

\[
\Delta \phi = 2\pi \frac{\delta n L \lambda}{\lambda} = (2n_2)(|E|^2/2)
\]

where \( \delta n \) is the variation of the effective index of the fundamental mode at the probe wavelength. \( n_2 \) is the self-focusing nonlinear index of refraction. The factor of 2 multiplying \( n_2 \) accounts for CPM, which is twice the SPM effect. In CGS units we have

\[
|E|^2 = 8\pi \times 10^7 P / ncA_{eff} \quad A_{eff} = \pi(w_1^2 + w_2^2)/2
\]

where \( w_1 \) and \( w_2 \) are the probe and pump spot sizes. Measuring the phase shift \( \Delta \phi \) as a function of pump power \( P \) yields \( n_2 \):

\[
n_2 = nc\lambda A_{eff} \Delta \phi / (16\pi^2 \times 10^7 LP)
\]

Fig. 1 Experimental set-up

Fig. 3 Measured RMS jitter amplitude in asynchronous DS-1/SONET multiplexing against DS-1 offset frequency

- With conventional synchroniser (without threshold modulation)
- With threshold modulation

Fig. 3 Measured RMS jitter amplitude in asynchronous DS-1/SONET multiplexing against DS-1 offset frequency

1 UI = 360 deg

a. With conventional synchroniser (without threshold modulation)
b. With threshold modulation

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