"Primary Multiplexing"

Stage at which several analog signals are sampled, quantized, coded, and combined into one digital bit stream. Framing needed to define channel numbering.

"Loop timing" - master sampling clock can be derived from the outgoing transmission system clock so that all digital tributary streams are perfectly synchronized (and hence interleave naturally).

![Diagram of DS-1 signal timing and channel structure]

Basic DS-1 frame structure:

- **Channel 1 - Channel 24**: 8 bits/week
- **F-bit**: 1 bit
- **8,000 frames/sec** (125 μsec/frame)
- **Bit rate** = 24 x 8 + 1 = 193 bits • 8,000 frames = 1.544 Mb/s
Distributed (Added - digit) bit-frame alignment

- The basic (D1 format) DS-1 signal has one bit per frame for frame alignment. (1 bit in 193!)
- How can this possibly work?
  - Any pattern on the F-bit can be mimicked by any of the data bits too!

A.
- Yes, but not forever. The F-bit position will be like a digital "beacon". We search for it and only know we have found it because it always follows the frame pattern. Whereas data bits eventually give themselves away.

True F-bit framing pattern (D1) = 1010101010…

- Prob a data bit mimics this pattern for n successive tests in a row = \( \frac{1}{2^n} \) (n = #frame to frame comparisons)

\[ \begin{aligned}
\text{Expected number of frames until a false framing bit position reveals itself} &= \quad \text{(and the search moves on)} \\
&= \frac{1}{2} + 2 \left( \frac{1}{2} \right)^2 + 3 \left( \frac{1}{2} \right)^3 + \ldots \\
&= \sum_{n=1}^{\infty} n \left( \frac{1}{2} \right)^n = 2 \quad \text{[frames]} \\
&\approx \text{if the frame is } N \text{ bits long, the average number of false positions to be eliminated is } \frac{N}{2}.
\end{aligned} \]
And it takes one frame time to establish an initial "1" or "0" reference for the sequence being tested.

\[ \text{Average reframe time} = \left( \frac{N}{2} \right) \left( 2N + 1 \right) \text{ [bit time]} \]

Industry design specs are usually on the "maximum average reframe time" = expected time for a maximal length burst to find the true framing bit position.

More average reframe time = \( N \left( \frac{2N+1}{2} \right) \text{ [bit time]} \)

For DS-1, \( N = 193 \) bit rate = 1.544 Mbps

\( \text{Max avg reframe time} = 48.7 \text{ mSec} \)

Finite State Machine for (resiliant) frame finding/seqencing (Typical)

```
          0 -> in-frame
          1
          0
          1
          1

\[ \text{Declare in-frame} \]

\[ \text{Lost of frame declared} \]
```

\( 1 = \text{framing error} \)
\( 0 = \text{no error} \)

\( \text{slip} = \text{advance candidate bit position} \)
Typical framing system performance measures:

- Maximum average reframe time
- Out-of-frame detection time
- False-in-frame time (false declaration of in-frame condition)
- Mean time to false misframe (at specified BER)

How to make reframing faster?

- Lookahead or "skip compensation" in the search process

  - If skip occurs off of current candidate position(s),
    the recent history of bit(s) in the frame is
    already recorded to keep decisions process
    going at full speed. More important when
    the framing pattern is a long unique word.

    - e.g. 101010 - store one bit of history on
    next candidate
    - 10011001 - store 3 bits of history on
    next candidate position

- Parallel search

  - Define a block width $K$, $1 < K \leq N$ of
    frame bit positions which will all be evaluated
    in parallel for ongoing consistency with the
    known framing pattern.

  - A kind of "statistical siege"

  - $K = N$, parallel framing search on entire frame

  It information limited performance. (but core)
Parallel framing search concept:

- Full frame (or masterframe) length
- Search block, K bits
- Frame i

- Compare, $K/2$ survive
- Disqualified candidates
- Compare, $K/4$ survive
- Compare, $K/8$ survive
- Compare, 1 or 0 surviving

- Zero survivors, move block along & repeat
- 1 survivor, adapt new frame position

- Probability that a block of K (false) positions are all eliminated in n trials:

  $P_n = \left[1 - \left(\frac{1}{2}\right)^n\right]^K$
  
  for single framing bit error
Assume one search block is used, the full frame width. Then:

\[
\text{prob} \left( \text{frame found} \leq N \text{ trials} \right) = \left( 1 - \left( \frac{1}{2} \right)^N \right)^{N-1}
\]

50th percentile value \( \Rightarrow \eta = -\log_2 \left[ 1 - \left( \frac{1}{2} \right)^{N-1} \right] \)

**“Superframe” and “Extended Superframe” Formats**

- **SF Format** — define a 12-frame superframe to support “bit robbing” every 6th word of each channel, and to further structure that derived signalling channel into two subchannels “A” & “B”

<table>
<thead>
<tr>
<th>Frame</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Value: 001101100

**An SF Framing Procedure:**

- Search (as before) for 1/0
- Toggle on every second frame now.

- “Slide” from here into
  - Alignment on 001100 on the P-bits of intervening frames

Note:
- Only one unique alignment possible
- Define frame &
  - Superframe structure
  - Simultaneously
- Contains simple 10 toggle pattern (as before)
  - On every 2nd bit
  - To speed up framing
ESF format: Further extends the unique framing word distributed over the F-bit, so as to define a 24-Frame "Extended" Syncframe.

- Restructures A/B bit sequences (each at 4 kbps) into providing a 4 kbps general purpose data link and a 2 kbps Cyclic Redundancy Check channel
- Basic frame alignment sequence now becomes 0 0 1 0 1 1 defined on every 4th frame.

- Important: ESF format finally abandons the practice of "bit robbing".
- Key benefit: 8 bit clear channel transmission (Can use for data applications)
- But how is reframe speed retained?

SF format:

```
<table>
<thead>
<tr>
<th>D3/D4</th>
<th>Frame Number</th>
<th>Frame Number</th>
<th>ESF F/DL/CRC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
<td>2</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>3</td>
<td>3</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>4</td>
<td>4</td>
<td>O</td>
</tr>
<tr>
<td>1</td>
<td>5</td>
<td>5</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>6</td>
<td>6</td>
<td>C</td>
</tr>
<tr>
<td>1</td>
<td>7</td>
<td>7</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>8</td>
<td>8</td>
<td>O</td>
</tr>
<tr>
<td>1</td>
<td>9</td>
<td>9</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>10</td>
<td>10</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>11</td>
<td>11</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>12</td>
<td>12</td>
<td>1</td>
</tr>
</tbody>
</table>
```

* - robbed
16 kbps of
Prior sample
for A/B signalling
### E1 Frame Structure

**Frame Format:**

- **Frame Time:** 125 µs
- **Frames per Second:** 8000
- **Bits per Frame:** 32,768
- **Bits per Second:** 2.048 Mbps

#### E1 Frame Time

- **Start of Frame (SoF):** 10 bits
- **Frame Sync (FS):** 7 bits
- **Channel 1-32:** 32 x 8 bits
- **Continuing Time:** 102 µs
- **End of Frame (EOF):** 8 bits

#### E1 Frame Structure in Table Form

<table>
<thead>
<tr>
<th>Frame</th>
<th>Channel</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame 1</td>
<td>1-32</td>
<td>32 x 8 bits</td>
</tr>
<tr>
<td>Frame 2</td>
<td>1-32</td>
<td>32 x 8 bits</td>
</tr>
<tr>
<td>Frame 3</td>
<td>1-32</td>
<td>32 x 8 bits</td>
</tr>
</tbody>
</table>

#### E1 Frame Time in Table Form

<table>
<thead>
<tr>
<th>Frame</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>2</td>
<td>7</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
</tr>
</tbody>
</table>

#### E1 Frame Time in Graphical Form

- **Duration:** 125 µs (4096 bits)
Other framing concepts

- Put a unique "marking" attribute in the line code (e.g., reserve a certain level). In many signalling systems, all other levels represent a unique binary pattern. But one pattern of data is defined as having 2 line code symbols that can represent it.

- In a B(1,2) code, can make the following assignment of line-code-word space to payload bit word space:

- Choose \(2^n\) "good" line code words from here (3 x 2^n available)
- Reserve three \(2^n\) words to convey any n-bit data word plus transparently a "frame time" indication.
8. Digital Multiplexing

Multiplexing can be classified as primary or first level multiplexing and secondary, higher level multiplexing. In primary multiplexing, several analog signals are sampled, quantized and multiplexed into one digital bit stream. Secondary multiplexing combines several digital bit streams into one higher rate output bit stream.

8.1 Multiplexing Hierarchy

In North America and Japan, first level multiplexing combines 24 analog voice signals into digital signal one (DS1) output at 1.544 Mb/s. In North America, four DS1 signals at 1.544 Mb/s are digitally multiplexed to form one DS2 signal at 6.312 Mb/s and seven DS2 signals are combined with the M23 multiplexer to form one DS3 signal at 44.736 Mb/s. Finally, six DS3 signals are combined in the M34 multiplexer to form one DS4 signal at 274.176 Mb/s. Slight variations in the tributary bit rates are accommodated through the technique of pulse stuffing. A table (Freeman page 367) compares the standard multiplexer rates for North America, Japan and Europe.

<table>
<thead>
<tr>
<th>System Type</th>
<th>Level</th>
<th>Number of voice channels</th>
<th>Rate (Mb/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>North America</td>
<td>1</td>
<td>24</td>
<td>1,544</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>96</td>
<td>6,312</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>672</td>
<td>44,736</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>4032</td>
<td>274,176</td>
</tr>
<tr>
<td>Japan</td>
<td>1</td>
<td>24</td>
<td>1,544</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>96</td>
<td>6,312</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>480</td>
<td>32,064</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>1,440</td>
<td>97,728</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>5,760</td>
<td>400,352</td>
</tr>
<tr>
<td>Europe</td>
<td>1</td>
<td>30</td>
<td>8,448</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>120</td>
<td>34,368</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>480</td>
<td>139,264</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>1,920</td>
<td>565,148</td>
</tr>
</tbody>
</table>

Original North American plans called for wireline transmission of DS1 and DS2 signals and waveguide or coaxial cable transmission of DS4 signals. It was intended to use the DS3 rate only as an intermediate signal between multiplexers and not for transmission. The original hierarchy proposed in the early 1960's is illustrated in Fig. 8.1-1.

4:25 PM 10/19/96 8. Mux *9a 210
With the introduction of optical fiber and digital microwave systems, transmission at the DS3 rate became common place. On the other hand, transmission at the DS2 rate was rare since it required spans of specially manufactured low capacitance cable. The standard transmission rates throughout North America evolved toward DS1 and DS3. Improving technology in wire transmission and the use of screened cable allowed the use of the DS1-C rate which is twice that of DS1 but half that of DS2. An illustration of the resulting multiplexing hierarchy is shown in the figure below. Following sections will discuss DS1 transmission formats and the technique of asynchronous digital multiplexing using pulse stuffing.

![Image](image_url)
A new standard for a synchronous optical network (SONET) was set in 1988. The multiplexing format uses one framing structure at the STS1 rate of 51.840 Mb/s and all tributaries are referenced to it through pointers. This allows drop and insert of a low rate DS1 signal without several levels of demultiplexing and remultiplexing. The format accommodates the DS1, DS1C, DS2 and DS3 formats of the existing North American hierarchy as well as the first level European CEPT format at 2.048 Mb/s. Tributaries at 51.840 Mb/s can be grouped using synchronous multiplexing to form signals at rates up to 2488.320 Mb/s.

8.2 First Level Multiplexing Formats

Voice signals are converted to digital form by a channel bank which, for North American samples, codes and multiplexes 24 voice signals to produce a 1.544 Mb/s digital signal for transmission. Voice signals are each sampled at a 8 kHz rate and
8.4 NON-SYNCHRONOUS DIGITAL MULTIPLEXING

Transmission economy is improved if several digital signals are combined to form one higher rate digital bit stream. If the tributary bit streams originate from geographically separate locations, the clocking rates may differ slightly. If two bit streams are to be interleaved into a higher rate digital signal, a small number of dummy or empty time slots must be added to the lower rate tributary bit stream. This results in equal input bit rates to the interleaving process. This process is known as "justification".

Input tributary bits are placed in an "elastic" memory which is read more frequently than it is written. When the memory is nearing depletion, an empty time slot is transmitted which is then said to contain a "stuff" bit. In practice, the information transmission rate of the high speed channel slightly exceeds the total input bit rate and "stuffing" bits must be added to all tributary channels. As expected more stuff bits will be allocated to the lower speed channels. The average ratio of stuff bits to information bits is in the order of 0.2%.
At the demultiplexer, the empty or stuffing time slots must be identified and removed from the information stream. Another elastic memory is used to spread the data, fill in the gaps, and emit a bit stream with uniform time intervals. In addition to the information and stuff bits, control bits and framing bits are added to the high rate channel. The framing bits identify the location of the control bits and the time slot which may or may not be empty depending on the status of the control bits. Note that all bits of each input digital stream are treated equally including the lower rate framing bits.

If a stuffing bit is not removed or an information bit is deleted by the demultiplexer, a one bit displacement will occur in the lower rate channel. This is a severe disturbance since all output samples will be incorrect until the lower rate system can reframe. Control bits are therefore transmitted in triplicate to lessen the probability of a stuffing error caused by channel error.

The digital network in North America is becoming totally synchronized to improve the operation of digital switches. Requirements for multiplexing non-synchronous data streams is therefore decreasing. The pulse stuffing transmission systems, however, have become standard and will remain so long after the network becomes synchronous.

8.4.1 MCI Asynchronous Multiplexing for DS1-C Signals

The MCI multiplexer interleaves two DS1 bit streams (at nominal rate 1.544 Mb/s) into one DS1-C signal at 2.152 Mb/s. As illustrated by the “pipe” diagram below, stuffing bits are added to the data to bring both input rates up to 1546.6 kbps which permits synchronous multiplexing and demultiplexing. Also multiplexed with the data signals are a framing sequence and two stuff control channels which are used to remove the stuffing bits after demultiplexing.
The frame structure is organized with one overhead bit followed by 52 information bits (26 from each input DS-1 stream). A subframe contains 6 overhead bits and 6 x 52 information bits. One of the information bits in each subframe is designated as a stuff location and may contain DS1 information or it may contain a useless stuff bit. To allow stuffing in each of the two input streams, the frame must be defined with at least 2 subframes and to allow inclusion of the alarm bit X the frame has been defined with 4.
The stuffing process may be visualized using ring buffers where the multiplexing buffers are written at the input rates (i.e., 1545 and 1542 kbps) and read out at the "transport" rate of 1546.6 kbps. To avoid over-reading these buffers, the input write location is occasionally advanced an extra bit leaving a random stuff bit (a previously written bit) to be transported to the ring buffers in the demultiplexer. When this is about to occur, the multiplexer signals the remote demultiplexer using the stuff control bits. When at least 2 of the 3 bits are logic 1, the demultiplexer advances the read location by an extra bit and thus the stuff bit is not presented to the output.
8.4.2 M12 Multiplexing for DS2 Signals

In the M12 multiplexer, four DS1 digital signals at 1.544 Mb/s may be asynchronously multiplexed into one DS2 signal at 6.312 Mbps. The DS2 bits are grouped into 1176 bit masterframes each with four 294 bit subframes containing 3 framing bits, 3 control bits and 288 information bits. One of the information bits may be used or "stuffed" which allows some frequency inaccuracy in the DS1 signal.

8.4.3 M23 Multiplexing for DS3 Signals

![Diagram of M23 Multiplexing for DS3 Signals](image)

8.4.4 SYNTRAN

Synchronous transmission at the DS-3 level permits better management of the growing DS-3 race network and will permit direct termination to digital switches. SYNTRAN, which is synchronous to the 125 microsecond frame, permits access to the DS-0 and DS-1 signals directly from the synchronous DS-3 signal without the need for stuffing bit removal and demultiplexing through the DS-2 level. Removal of the stuffing bits and the intermediate framing bits allows for the insertion of cyclic redundancy check bits and other features for improved transmission system operation. (p670 NCF/36, G. Kichie)

8.5 SONET

In the mid 1980's, the working group T1X1 of the American National Standards Institute (ANSI), developed a standard informally called SONET for Synchronous
T1.105-1988, defines a base rate of 51.840 Mbit/s which is called the STS-1 signal. It also defines an equivalent 51.840 Mbit/s optical signal which is called OC-1 (Optical Carrier Level 1). Higher-level signals in the SONET hierarchy are obtained by byte-interleaving a number of STS-1 signals. Examples include STS-3 (and OC-3) which has 3 STS-1 signals and runs at 155.520 Mbit/s, and STS-48 (OC-48) which runs at 2.488320 Gbit/s.

The STS-1 frame is 125 μs long, so there are 8,000 frames per second. The STS-1 frame can be organized to accommodate DS1 (1.544 Mbit/s) DS2 and DS3 signals as well as the E1 30-channel (2.048 Mbit/s) signal. The basic format of the STS-1 frame is illustrated in Fig. 8.14. There are 9 rows of 90 bytes giving 810 bytes or 6480 bits in a 125 μs frame. The first 3 bytes in each row are transport overhead bytes while the remaining 783 bytes used to carry the synchronous payload envelope (SPE).

![Fig. 8.5-1 Organization of the SONET STS-1 Frame](image)

A "payload pointer" within the transport overhead is used to designate the beginning of the SPE which may begin in one frame and end in another. The payload pointer and SPE are illustrated in Fig. 10.15. The 9-byte path overhead is used to provide end-to-end communication between systems. A path is defined to end at the point at which the STS-1 signal is created or torn apart-demultiplexed-into its constituent lower-bit-rate signals.
DS3 signals are accommodated by the SONET structure by mapping 621 x 9 data bits into the STS-1 synchronous payload envelope to provide a bit rate of 44,712 Mbit/s. This is illustrated in Fig. 10.16. Stuffing bits are used to bring the bit rate up to the desired 44,736 Mbit/s. Each SPE row has in addition to the 621 data bits, 1 stuff opportunity bit and 5 C (stuff control) bits. The remaining bits of the SPE are ignored at the end of the path. The stuff opportunity bit in each subframe can be used as an additional data bit by setting each of the 5 C bits to zero. If the bit has been stuffed and is therefore unused, each of the C bits is set to 1. This adds up to 72 kbit/s to the 44,712 Mbit/s for a maximum possible data bit rate of 44,784 Mbit/s. The actual DS3
**Chapter 8: Digital Multiplexing**

![Figure 8.5-3 SPE Mapping to Accommodate DS-3 signals.](image)

### Problems

**8.3.** Consider an M12 multiplexer operating at the nominal DS2 rate of 6.312 Mbps.

i) What is the maximum and minimum DS1 input rate which can be accommodated by the asynchronous multiplexer?

ii) There is a “stuff” bit location associated with each DS1 input signal. If the input DS1 rate is exactly 1.544 Mbps, what fraction of the time will the “stuff” bit location carry useful DS1 information?

**8.4.** Suggest how DS2 signal format could be modified to increase the allowed rate variation in the input DS1 signals.

**8.5.** The DS-3 digital signal rate is 44.736 Mbps. This signal is formed by asynchronous multiplexing of 7 digital signals at the nominal DS-2 rate of 6.312 Mbps. Each DS-3 signal is partitioned into frames of 4760 bits which are divided into seven subframes each having 680 bits. There are five framing and alarm bits and three control bits in each subframe. Each subframe has one opportunity for bit stuffing in one of the DS-2 tributary signals.

a) What percentage of the transmission capacity is used for framing and control and what percentage can be used for the transmission of DS-2 signals?