3. Overview of Microfabrication Techniques
The Si revolution…

First Transistor
Bell Labs (1947)

Si integrated circuits
Texas Instruments (~1960)

Modern ICs

More ? Check out:
http://www.pbs.org/transistor/background1/events/miraclemo.html
http://www.ti.com/corp/docs/company/history/firstic.shtml
The need of micropatterning

The batch fabrication of microstructures requires a low-cost, high-throughput surface patterning technology
Microfabrication Processes

Complete processing sequence consist of:

Layering:
- Oxidation
- Deposition

Patterning:
- Lithography
- Etching

Doping:
- Ion Implantation
- Diffusion
Again and again....

Source: [http://www.cae.wisc.edu/~chauhan/nanolith2.shtml](http://www.cae.wisc.edu/~chauhan/nanolith2.shtml)
Bulk micromachining

Fabrication technologies for the machining of "bulk" microdevices in silicon
Example: Membrane Pressure Sensor
Example: MEMS Microturbines
3. Overview of Microfabrication...TOC

- Wafer-Level Processes
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding
3. Overview of Microfabrication…TOC

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization
3. Overview of Microfabrication...

- **Wafer-Level Processes**
  - **Substrates**
    - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding
Growth of Silicon (ctnd.)

- Quartzite or SiO₂ (sand) is reacted in a furnace with carbon (from coke and/or coal) to make *metallurgical grade silicon* (MGS) which is about 98% pure, via the reaction:
  \[ \text{SiO}_2 + 2\text{C} \rightarrow \text{Si} + 2\text{CO} \]

- The silicon is crushed and reacted with HCl (gas) to make trichlorosilane:
  \[ \text{Si} + 3\text{HCl(gas)} \rightarrow \text{SiHCl}_3 + \text{H}_2 \]

- Fractional distillation is then used to separate out the SiHCl₃ from most of the impurities. The (pure) trichlorosilane is then reacted with hydrogen gas to form pure electronic grade silicon (EGS):
  \[ \text{SiHCl}_3 + \text{H}_2 \rightarrow 2\text{Si} + 3\text{HCl} \]
The EGS is melted in a crucible, and then inserting a seed crystal on a rod called a puller which is then slowly removed from the melt.

If the temperature gradient of the melt is adjusted so that the melting/freezing temperature is just at the seed-melt interface, a continuous single crystal rod of silicon, called a boule, will grow as the puller is withdrawn.
The boule is grown down to a standard diameter. Flats are polished onto to boule to indicate crystalline orientation (above) before it is sliced into wafers.
3. Overview of Microfabrication...TOC

- Wafer-level Processes
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding
RCA cleaning of Si

The RCA cleaning procedure has three major steps used sequentially:


II. Oxide Strip: Removal of a thin silicon dioxide layer where metallic contaminants may accumulated as a result of (I), using a diluted 50:1 H₂O:HF solution.

III. Ionic Clean: Removal of ionic and heavy metal atomic contaminants using a solution of 6:1:1 H₂O:H₂O₂: HCl.
3. Overview of Microfabrication...TOC

- Wafer-level Processes
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding
Thermal Oxidation

Thermal oxidation of silicon accomplished at high temperatures by flowing oxygen sources such as $O_2$ or $H_2O$. 

- Wafers
- Quartz tube
- Quartz boat
- Flowmeter
- $O_2$
- Furnace
Thermal Oxidation (ctnd.)

Oxidation Reactions

Si (solid) + O₂ (gas) $\xrightarrow[900 - 1200^\circ C]{\;}$ SiO₂ (solid)

Si (solid) + 2H₂O (gas) $\xrightarrow[900 - 1200^\circ C]{\;}$ SiO₂ (solid) + 2H₂ (gas)

The growth of an oxide layer of thickness $x$ will consume $0.44x$ of silicon.
Thermal Oxidation (ctnd.)

Horizontal Tube Furnace

Most popular furnace used for oxidation, diffusion, and heat treatments

Check out: Plummer, Deal Griffin, Silicon VLSI Technology, Chap 6
Thermal Oxidation (ctnd.)

Growth kinetics dictated by transport and diffusion of precursors at the Si/SiO2 interface
3. Overview of Microfabrication...TOC

- Wafer-level Processes
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding
The Silicon Lattice

The silicon atoms share valence electron through covalent bonds
At $T = 0\, \text{K}$, all covalent electrons are localized to their covalent bond, and therefore no conduction can take place.

At $T > 0\, \text{K}$ (above left), thermal agitation can be sufficient for some electrons to break away from the covalent bonds, and can freely drift around the lattice. These conduction electrons leave behind a "hole" in the covalent bond, which can also "move" by having nearby covalent electrons hop into the empty state. When a field is applied (above right), the conduction electrons drift in one direction, while the holes drift in the opposite ones.
At $T > 0$ K, thermal agitation can be sufficient for some electrons to break away from the covalent bonds, and can freely drift around the lattice. This will populate the conduction band with electrons, and the valence band with empty orbitals ("holes"), in equal amount ($n = p$).
Doping of Semiconductors: n-type

An impurity with extra valence electron releases this electron in lattice, therefore creating a surplus of electrons over holes ($n > p$)
Doping of Semiconductors: p-type

An impurity with less valence electrons creates a vacant state in the valence band therefore creating a surplus of holes over electrons ($p > n$)
Summary: Intrinsic vs Doped Material

The n-doped material is rich in negatively charged conduction electrons.
The p-doped material is rich in positively charged valence band holes.
Introduction of Dopants

- **Local modification** of the material doping type and level

- Two methods are used:
  - Diffusion
  - Ion Implantation

- Advantage of implantation:
  - less under-diffusion
  - shallower junction
  - better control of depth (energy)
  - better control of concentration (dose)
Doping by Ion Implantation
Doping by Ion Implantation (ctnd.)
Doping by Ion Implantation (ctnd.)

Figure 8–2 Distribution of ions implanted into crystalline silicon at an energy of 200 keV. The light ions travel further and have a broader distribution than the heavy ions.
can be described statistically and is often modeled to first order by a symmetric Gaussian distribution given by

\[ C(x) = C_p \exp\left( -\frac{(x - R_p)^2}{2\Delta R_p^2} \right) \quad (8.1) \]

where \( R_p \) is the average projected range normal to the surface, \( \Delta R_p \) is the standard deviation or straggle about that range, and \( C_p \) is the peak concentration where the Gaussian is centered. Figure 8–3 plots the range and standard deviation for common dopants in silicon. Note that the profiles in Figure 8–2 are not perfectly symmetrical. We will return to these details later.

The total number of ions implanted is defined as the dose and is simply

\[ Q = \int_{-\infty}^{\infty} C(x)dx \quad (8.2) \]

Making use of the fact that the sum (or integral) of Gaussian functions is an error function (Chapter 7), and using the formula which defines the error function gives

\[ \int_{-\infty}^{\infty} \exp^{-u^2}du = \frac{\sqrt{\pi}}{2} [\text{erf}(\infty) - \text{erf}( - \infty)] \quad (8.3) \]

so that

\[ Q = \sqrt{2\pi \Delta R_p C_p} \quad (8.4) \]
Ion Implantation Process (ctnd.)
Ion Implantation Process (ctnd.)

(b) Projected and transverse straggle (µm) vs. Energy (keV)

- Si
- B
- P
- As

Energy (keV) vs. Projected and transverse straggle (µm)
Doping by Ion Implantation (example)

Q: Arsenic is implanted into a lightly doped p-type Si substrate at an energy of 75 keV. The dose is \(1 \times 10^{14}\) cm\(^{-2}\). The Si substrate is tilted 7° with respect to the ion beam to make it appear amorphous. The implanted region is assumed to be rapidly annealed so that complete electrical activation is achieved. What is the peak electron concentration produced?

A: From above graphs, the range and standard deviation for 75 keV arsenic are

\[
R_P = 0.05\mu m \quad \Delta R_P = 0.02\mu m
\]

The peak concentration is:

\[
C_P = \frac{Q}{\sqrt{2\pi} \Delta R_P} = \frac{1 \times 10^{14}}{\sqrt{2\pi} \left(0.02 \times 10^{-4}\right)} = 2 \times 10^{19} \text{ cm}^{-3}
\]

Assuming all the dose is active, then the peak electron concentration is equal to the peak dopant concentration.
Channeling Effects
Channeling Effects

Figure 8-10 Image of a silicon crystal looking down the 110 axial channels (top left), the 111 planar channels (top right), the 100 axial channels (lower left), and with a tilt and rotation to simulate a “random” direction (lower right).
Channeling Effects (ctnd.)

![Graph showing concentration vs. depth for different channeling effects.]

- 2 × 10^{13} \text{ cm}^{-2}
- 2 × 10^{15} \text{ cm}^{-2}
- 2 × 10^{13} \text{ cm}^{-2} \text{ scaled}

Concentration (cm^{-3})

Depth (\mu m)
Ion implantation for production of buried oxide

(a) Crystalline Si
(b) Stoichiometric SiO2
(c) Si with O2 implant
(d) Polysilicon

O2 Implant

Anneal
Cross-section of SIMOX wafers

(a) As implanted: 1.7E18/cm², 200keV, 520C
(b) Annealed: 1320C, 4hrs
Doping by Diffusion

**Figure 7-3** Two-step process for producing a junction at the desired depth. The predeposition step introduces a controlled number of impurity atoms, while the drive-in step thermally diffuses the dopant to the desired junction depth.
Diffusion Process

The diffusion process is ideally described in terms of Fick’s diffusion equation:

\[ \frac{\partial C}{\partial t} = D \frac{\partial^2 C}{\partial x^2} \]

where \( C \) is the dopant concentration, \( D \) is the diffusion coefficient, \( t \) is time, and \( x \) is measured from the water surface in a direction perpendicular to the surface.

The initial conditions of the concentration \( C(0, t) = 0 \) at time \( t = 0 \) and the boundary conditions are that surface concentration \( C(0, t) = C_s \) (the solubility of the dopant) at surface and that a semi-infinite medium has \( C(\infty, t) = 0 \). The solution that satisfies the initial and boundary conditions is given by:

\[ C(x, t) = C_s \text{erfc} \left( \frac{x}{2\sqrt{Dt}} \right) \]

where \( \text{erfc} \) is the complementary error function and the diffusion coefficient \( D \) is a function of temperature \( T \) expressed as:

\[ D = D_0 \exp \left( \frac{-E_A}{kT} \right) \]

The total dose being diffused into semiconductor is:

\[ Q = \int_0^\infty C(x, t) \, dx = \frac{2C_s}{\sqrt{\pi}} \sqrt{D} \sqrt{t} \]

where \( E_A \) is the activation energy of the thermally driven diffusion process, \( k \) is Boltzmann’s constant, and \( D \) is the diffusion constant.
Figure 2.16 Theoretical diffusion profile of dopant atoms within a silicon wafer
Figure 7-4 Solid solubility curves for various dopants in silicon. These values are the equilibrium solubilities at each temperature and may not be achieved in device doped regions. (After [7.3].)
Diffusion Process (ctnd.)

\[ D = D^0 \exp \left( -\frac{E_A}{kT} \right) \]

**Figure 7-15** Arrhenius plot of the intrinsic diffusivity of the common dopants in silicon.
Numerical Example

**Q:** A p-type (boron) diffusion is performed in silicon as follows for 30 min at 900°C. What is the deposited \( Q \)? Assume that the solid solubility is maintained at the surface (\( x=0 \))

**Solution:**
According to figures above, the boron diffusion coefficient is:

at 900°C: \( \text{D}^{900}_B = 1.0 \exp\left(-\frac{3.5}{k(900+273)}\right) = 9.27 \times 10^{-16} \text{cm}^2\text{s}^{-1} \)

The deposition is performed at 900°C where the boron solid solubility from Table 7.4 is: \( C_s = 1.2 \times 10^{20} \text{cm}^{-3} \)

The dose introduced is then:

\[
Q = \frac{2C_s}{\sqrt{\pi}} \sqrt{D \tau} = \frac{2(1.2 \times 10^{20})}{\sqrt{\pi}} \sqrt{9.27 \times 10^{-16}(30 \times 60)} = 1.75 \times 10^{14} \text{cm}^{-2}
\]
3. Overview of Microfabrication...

- Wafer-Level Processes
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding
Electronic Materials

- Typical IC materials include:
  - Thermal oxides (covered previously)
  - Other Dielectric Materials
  - Poly-crystalline silicon (Poly-Si)
  - Metals
Typical IC materials include:

- Thermal oxides (covered previously)
- Other Dielectric Materials
- Poly-crystalline silicon (Poly-Si)
- Metals
Chemical Vapor Deposition

- **SiO₂**
  - Field Oxide
  - Interlevel Insulator
  - Passivation (overcoat layer)
- **Si₃N₄**
  - Local Oxidation Mask
  - Protective Overcoat Layer
  - Gate Dielectric
- **Poly-Si**
  - Gate Material in MOSFET
- **Metallization**
  - Interconnects
- **Epitaxial Layers**
  - Si
  - Ge
  - GaAs
  - GaP

**Purpose:** low temperature deposition of insulators and conductors
Chemical Vapor Deposition (CVD)

A: Gaseous transport and adsorption of precursor
B: Surface transport and reaction
C: Desorption of by-products
Chemical Vapor Deposition (ctnd...)

For SiO₂:
- \( \text{SiH}_4 + \text{O}_2 \xrightarrow{500 \, ^\circ\text{C}} \text{SiO}_2 + 2 \, \text{H}_2 \)
- \( \text{SiCl}_2\text{H}_2 + 2 \, \text{H}_2\text{O} \xrightarrow{900 \, ^\circ\text{C}} \text{SiO}_2 + 2 \, \text{H}_2 + 2 \, \text{HCl} \)

For Si₃N₄:
- \( 3\text{SiCl}_2\text{H}_2 + 4 \, \text{NH}_3 \xrightarrow{800 \, ^\circ\text{C}} \text{Si}_3\text{N}_4 + 6 \, \text{HCl} + 6 \, \text{H}_2 \)

For Poly-Si:
- \( \text{SiH}_4 \xrightarrow{600 \, ^\circ\text{C}} \text{Si} + 2 \, \text{H}_2 \)
Low Pressure CVD (LPCVD)

1. Pressure between 0.2 and 2.0 torr
2. Gas flow between 1 to 10 cm$^3$/s
3. Temperatures between 300 and 900 °C
Plasma-enhanced CVD (PECVD)

Deposition of material physically assisted by RF plasma

Allows lower deposition temperatures
### Properties of Oxide Films

<table>
<thead>
<tr>
<th>Property</th>
<th>Composition</th>
<th>Step coverage</th>
<th>Density $\rho$ (g/cm$^3$)</th>
<th>Refractive index $n_r$</th>
<th>Dielectric strength (V/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermally grown at 1000°C</td>
<td>SiO$_2$</td>
<td>–</td>
<td>2.2</td>
<td>1.46</td>
<td>$&gt;10^{-5}$</td>
</tr>
<tr>
<td>Deposited by SiH$_4$ + O$_2$ at 450°C</td>
<td>SiO$_2$(H)</td>
<td>Nonconformal</td>
<td>2.1</td>
<td>1.44</td>
<td>$8 \times 10^{-6}$</td>
</tr>
<tr>
<td>Deposited by TEOS at 700°C</td>
<td>SiO$_2$</td>
<td>Conformal</td>
<td>2.2</td>
<td>1.46</td>
<td>$10^{-5}$</td>
</tr>
<tr>
<td>Deposited by SiCl$_2$H$_2$ + N$_2$O at 900°C</td>
<td>SiO$_2$</td>
<td>Conformal</td>
<td>2.2</td>
<td>1.46</td>
<td>$10^{-5}$</td>
</tr>
</tbody>
</table>
Ar atoms are ionized at low pressure by an electric field.

The positive ions are accelerated towards the negatively charged target:

Sputtered material condenses on the ambient surfaces
Electronic Materials

Typical IC materials include:

- Thermal oxides (covered previously)
- Other Dielectric Materials
- Poly-crystalline silicon (Poly-Si)
- Metals
Metallization

- **Purpose:** interconnecting the devices to form a circuit
- **Use low resistance metal layers:**
  - Aluminum alloys
  - Silicides
  - Copper
- **Important issues:**
  - Resistivity
  - Electromigration
  - Planarity

Nine levels of metallization (with low-k dielectric and SiC-based barriers)

- Copper introduced in 2001 by IBM
- Lower resistance than Aluminum
- Less interconnection delays on chip
- Higher clock frequencies possible

(Source: AMD)
Metallization by evaporation
3. Overview of Microfabrication…TOC

Wafer-Level Processes

- Substrates
- Wafer Cleaning
- Oxidation
- Doping
- Thin-Film Deposition
- Wafer Bonding
Wafer bonding

- Used to permanently join two wafers together
- Allows the design and fabrication of multi-level devices assembled from the machining of separate wafers
- Fundamentals of process not fully understood, but does rely on formation of Si-O-Si bonds between wafers.
MEMS microturbines
Wafer bonding by fusion (ctnd.)

Diagram showing the process of wafer bonding by fusion. The diagram illustrates the bonding of two layers of silicon with a layer of 

\( \text{SiO}_2 \) in between. The layers are heated to over 700°C to achieve the bonding. The bonding process includes the formation of silanol (Si-OH) bonds and siloxane (Si-O-Si) bonds. The reaction involves the dehydration of silanol groups to form siloxane networks.
Fusion bonding procedures

1. Surface treatment to make hydrophilic surfaces **by soaking wafers in Piranha, diluted sulfuric acid, or boiling nitric acid, or hydrophobic surfaces in HF.** Hydrophilic top layer consisting of O-H bonds (hydroxyl) is formed on the oxide surface.

2. Contacting the wafers in **clean air at room temperature after rinsing and drying them.** Self-bonding (**hydrogen bonding**) is formed throughout the wafer surfaces without external pressure with considerable forces.

3. Annealing (> 800°C) in oxidizing or nonoxidizing ambient. Water molecules come out and the voids (intrinsic) are observed beyond 200°C. **The voids tend to disappear and bonding strength is increased at more than 300°C forming siloxane (Si-O) bonds.** At high temperatures (>800°C), Oxygen at the interface may diffuse into the silicon bulk to form Si-Si bonds like single crystal silicon at above 1000°C.
## Wafer bonding by fusion

### Table 5.4

<table>
<thead>
<tr>
<th>Structure</th>
<th>Annealing temperature (°C)</th>
<th>Bond strength (Jm$^{-2}$)</th>
<th>Voids (% nonbonding)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si/Si</td>
<td>450</td>
<td>0.5</td>
<td>-</td>
</tr>
<tr>
<td>Si/Si</td>
<td>800</td>
<td>0.6</td>
<td>0.3</td>
</tr>
<tr>
<td>Si/Si</td>
<td>1000</td>
<td>2.6</td>
<td>0.3</td>
</tr>
<tr>
<td>Si/Si$_3$N$_4$(140 nm)</td>
<td>800</td>
<td>0.9</td>
<td>0.2</td>
</tr>
<tr>
<td>Si/Si$_3$N$_4$(140 nm)</td>
<td>1000</td>
<td>Cleavage</td>
<td>0.2</td>
</tr>
<tr>
<td>Si/Si$_3$N$_4$(300 nm)</td>
<td>1000</td>
<td>Cleavage</td>
<td>25</td>
</tr>
</tbody>
</table>
Thermal considerations in fusion bonding

1. Temperature less than 450°C for postmetallisation wafers.

2. Temperature less than 800°C for wafers with diffusion dopant layers (e.g. $p^+$ etch-stop layers).

3. Temperature greater than 1000°C for wafer bonding before processing. According to the reaction mechanism, annealing at temperatures above 1000°C for several hours should result in an almost complete reaction of the interface. A 1000°C anneal for about two hours gives sufficiently high bond strength for all subsequent treatments (Harendt et al. 1991); it is not possible to separate the two bonded Si wafers without breaking the silicon.
Anodic bonding: principle
Anodic bonding: principle (ctnd.)

(c) Diagram showing the bonding process involving sodium ions ($Na^+$) and oxygen ions ($O^-$) with a depleted zone and Si-O bond.

(d) Graph showing current density ($mA/cm^2$) against bonding time [sec].

States described in the corresponding subfigures.
**Anodic bonding: principle (ctnd.)**

- **General Principles:** *Due to the elevated temperature, the Na⁺ ions are mobile enough for the Pyrex to behave like a conductor. Hence, in the very first moment, most of the voltage applied to the silicon-Pyrex sandwich drops across a small gap of a few microns between the two surfaces.*

- The high electric field in this area creates a strong electrostatic force, pulling the two surfaces together and thus forming an intimate contact.

- In addition Na⁺ ions start drifting to the negative electrode, which is connected with glass, creating depletion zone adjacent to the silicon, positive electrode.

- During this charging process, the electric field is high enough to allow a drift of oxygen to the positive electrode (Si) reacting with silicon and creating Si-O bond.
Anodic bonding setup

Glass sputtered onto one of the silicon surfaces

Bonding take place at $T \sim 300-400 \, ^\circ\text{C}$, at $V = 50 - 1200 \, \text{V}$ (greatly varies depending on glass used for bonding)
Anodic bonding: procedure

- Typical Variables: temperature, applied voltage, bonding load, voltage-applying time, bonding area, glass thickness. 300 – 400 °C, 700-1200V. (FYI: Temperature limit for IC processed Si substrates is about 450 °C)

- General conditions: Silicon + Pyrex 7740, 400 °C, and 1000V.

- Requirements:
  - Microroughness (Ra) < 1μm. Warp/bow < 5μm
  - The native or thermal oxide layer on the Si must be thinner than 2000Å.

- Benefits:
  - Lower temperature process and popular and reliable process
  - Less stringent requirement for the surface quality of the wafers.
Alternate bonding technique: eutectic bonding

One wafer coated with Au prior to bonding
Temperature is raised until the Eutectic point is reached
Above eutectic temperature, Au will diffuse into Si (and not other way around)
An Au-Si eutectic alloy is then formed between the two wafers
Other Si-metal alloys eutectic bonding also possible
IR monitoring of bonded wafers

Quality of bonds is usually monitored using infrared absorption imaging.
Worked Example: floating element shear sensor

(a) Angled view and (b) cross section of a floating sensor based on a rectangular plate with four tethers
Worked Example: floating element shear sensor

Figure 2: Schematic plan view and cross-section of a typical floating-element sensor.

A better view of geometry of such device
Worked example: floating element shear sensor

(a) Silicon epi (5 μm thick)

(b)
Worked example: floating element shear sensor
3. Overview of Microfabrication

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization
3. Overview of Microfabrication…TOC

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization
Elements of photolithography
Lithography consists of patterning substrate by employing the interaction of beams of photons or particles with materials.

Photolithography is widely used in the integrated circuits (ICs) manufacturing.

The process of IC manufacturing consists of a series of 10-20 steps or more, called mask layers where layers of materials coated with resists are patterned then transferred onto the material layer.
Elements of photolithography (ctnd.)

- A photolithography system consists of a light source, a mask, and a optical projection system.

- **Photoresists** are radiation sensitive materials that usually consist of a photo-sensitive compound, a polymeric backbone, and a solvent.

- Resists can be classified upon their solubility after exposure into: *positive resists* (solubility of exposed area increases) and *negative resists* (solubility of exposed area decreases).
Positive vs. negative photoresists

Exposing
Radiation

Polymer Resist
Thin Film
Substrate

Positive
Developing
Resist

Negative

Etching and Stripping

Resist
Types of photolithography

1:1 Exposure Systems

- **Contact Printing**
  - Light Source
  - Optical System
  - Mask Photoresist
  - Si Wafer

- **Proximity Printing**
  - Light Source
  - Optical System
  - Gap

- **Projection Printing**
  - Light Source
  - Optical System
  - Usually 4X or 5X Reduction

Contact Printing  Proximity Printing  Projection Printing
Types of photolithography (ctnd.)

Contact lithography limited by Fresnel diffraction:

\[ W_{\text{min}} = \sqrt{\lambda g} \]

where \( \lambda \) is wavelength employed and \( g \) is mask-resist gap.
Types of photolithography (ctnd.)

Projection lithography limited by Rayleigh's criterion:

\[ R = \frac{k_1 \lambda}{NA} \]

where \( \lambda \) is wavelength employed, NA is numerical aperture of lense (\( NA = \sin \alpha \)), and \( k_1 \) is a constant (typically \( k_1 = 0.6 - 0.8 \))
Question:
An x-ray contact lithography system uses photons of energy of 1 keV. If the separation between the mask and the wafer is 20 μm, estimate the diffraction-limited resolution that is achievable by this system.

Answer:
The energy $E_p$ of photons is related to their wavelength $\lambda$ through:

$$E_p = \frac{hc}{\lambda}$$

where $h = 6.626 \times 10^{-34}$ m$^2$ kg/s is Planck’s constant, and $c = 3 \times 10^8$ m/s is the speed of light.

Thus, the wavelength of the photons employed is:

$$\lambda = \frac{6.626 \times 10^{-34} \cdot 3 \times 10^8}{1000 \cdot 1.6 \times 10^{-19}}$$

$$\lambda = 1.24 \text{ nm}$$

The minimum feature size that can be resolved is:

$$W_{\text{min}} = \sqrt{\lambda g}$$

$$W_{\text{min}} = \sqrt{1.24 \times 10^{-9} \cdot 20 \times 10^{-6}}$$

$$W_{\text{min}} = 157 \text{ nm}$$
Resolution of photolithography (ctnd.)
Resol. enhancement: phase shift masks (ctnd)

120 nm wide gates produced using $\lambda = 248$ nm radiation and PSM masks
Resolution enhancement: immersion lithography

- In immersion lithography, the medium through which the exposure light passes is purified water, with a refractive index of 1.44, rather than air.

- Therefore, the NA can be increased by a factor of up to 1.44, which will enable to surpass the barrier of the 65nm line width, which is considered the limit for ArF steppers.

- Theoretically, the technology is expected to be capable of extending micro processing down to the 45nm line width.

http://www.nikon.co.jp/main/eng/portfolio/about/technology/nikon_technology/immersion_e/index.htm
EUV lithography system (ctnd.)

One in every home...
Alternate Nanolithography Techniques

- Micro-contact Printing
- Nanoimprint Lithography
- Scanned Probe Lithography
- Dip-pen Lithography
Micro-contact printing

1) Application of ink to stamp
2) Application of stamp to surface
3) Removal of stamp
4) Residues rinsed off

Source: IBM Zurich
Biological interactions that underlie neuron cell attachment and growth are being employed to produce defined networks of neurons.

Microcontact printing has been used to place chemical, biochemical, and/or topographical cues at designated locations.

Important potential for the interfacing of solid state electronics with nerve cell biology, and for the fundamental electrical studies of single nerve cells.

Source: [Craighhead Group, Cornell](https://www.craighedgroup.com)
Alternate Nanolithography Techniques

- Micro-contact Printing
- Nanoimprint Lithography
- Scanned Probe Lithography
- Dip-pen Lithography
Nanoimprint Lithography

Consists of pressing a mold onto the resist above its glass transition temperature $T_g$

More? Check out S. Y. Chou, Princeton
SiO₂ pillars with 10 nm diameter, 40 nm spacing, and 60 nm height fabricated by e-beam lithography.

This master can be used tens of times for the imprinting of holes in PMMA without degradation.
NIL pattern in PMMA

- Mask is pressed into 80 nm thick layer of PMMA on Si substrate at 175° C ($T_g=105$ °C), $P=4.4$ MPa.

- PMMA conforms to master pattern, resulting in ~10 nm range holes
Reactive ion etching is used to cut down resist thickness until shallow regions are completely removed.

Ti/Au is deposited onto resist.

Resist and metal-coating is removed by solvent leaving behind metal dots where resist had been removed.
Alternate Nanolithography Techniques

- Micro-contact Printing
- Nanoimprint Lithography
- Scanned Probe Lithography
- Dip-pen Lithography
Scanned Probe Lithography

Source: Quate Group, Stanford
Fabrication of CMOS gate using SPM lithography

Source: Quate Group, Stanford
Alternate Nanolithography Techniques

- Micro-contact Printing
- Nanoimprint Lithography
- Scanned Probe Lithography
- Dip-pen Lithography
Dip-pen lithography

Source: Mirkin Group, NWU
A) Ultra-high resolution pattern of mercaptohexadecanoic acid on atomically-flat gold surface. B) DPN generated multi-component nanostructure with two aligned alkanethiol patterns. C) Richard Feynmann's historic speech written using the DPN nanoplotter.

Source: [Mirkin Group, NWU](#)
3. Overview of Microfabrication…TOC

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making (read)
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization
3. Overview of Microfabrication...TOC

- **Pattern Transfer**
  - Optical Lithography
  - Design Rules
  - Mask Making (read)
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization
Need for Wet Etching....

Selective removal of material as defined by photolithography

Etch

Remove photoresist
Wet Etching....

(a) Isotropic  (b) Anisotropic  (c) Completely Anisotropic

More Directional Etching
Isotropic vs anisotropic etching: etching bias

- Bias = \( d_f - d_m \)
- Complete isotropic etching \( B = 2h_f \)
- Complete anisotropic etching \( B = 0 \)
Degree of anisotropy

\[ A_f \equiv 1 - \frac{|B|}{2h_f} \]

\[ 0 \leq A_f \leq 1 \]

- \( A_f = 0 \): isotropic \quad \left| B = 2h_f \right|

- \( A_f = 1 \): anisotropic \quad \left| B = 0 \right|
Anisotropic etchants in silicon

\[ w = w_0 - 2h \cot(55^\circ) \]

**Figure 5.1** Anisotropic etching of (100) crystal silicon

\[ w = w_0 - 2h \cot(55^\circ) \]
Anisotropic etchants in silicon (ctnd.)

Table 5.1  Anisotropic etching characteristics of different wet etchants for single-crystalline silicon

<table>
<thead>
<tr>
<th>Etchant</th>
<th>Temperature (°C)</th>
<th>Etch-rate (μm/hour) of Si(100)</th>
<th>Si(110)</th>
<th>Si(111)</th>
</tr>
</thead>
<tbody>
<tr>
<td>KOH:H₂O</td>
<td>80</td>
<td>84</td>
<td>126</td>
<td>0.21</td>
</tr>
<tr>
<td>KOH</td>
<td>75</td>
<td>25–42</td>
<td>39–66</td>
<td>0.5</td>
</tr>
<tr>
<td>EDP</td>
<td>110</td>
<td>51</td>
<td>57</td>
<td>1.25</td>
</tr>
<tr>
<td>N₂H₄H₂O</td>
<td>118</td>
<td>176</td>
<td>99</td>
<td>11</td>
</tr>
<tr>
<td>NH₄OH</td>
<td>75</td>
<td>24</td>
<td>8</td>
<td>1</td>
</tr>
</tbody>
</table>
KOH etch of Si

- KOH etches silicon substrate
  - V-grooves, trenches
  - Concave stop, convex undercut
  - (100) to (111) $\rightarrow$ 100 to 1 etch rate
- Masks:
  - SiO$_2$: for short period
  - Si$_x$N$_y$: Excellent
  - heavily doped P$^{++}$ silicon: etch stop
Example MEMS Velcro

Post length, from head to base, 220μm

Head diameter 48μm

Distance between head centers, 78μm

Closest distance between heads, 38μm

240μm

Fig 2
Example: MEMS Velcro (ctnd.)

Figure 5.3  Process flow for the fabrication of silicon microvelcro
Need for etch-stopping layers
Need for etch-stopping layers (ctnd.)
Doping-selective etching

- KOH Concentration:
  - 10%
  - 24%
  - 42%
  - 57%

- <100> Silicon

- 60 °C

- Boron Concentration (cm^3)

- 10^17, 10^14, 10^11, 10^8, 10^5, 10^2

- EDP type S

- 110 °C, C_b = 2.8 x 10^16 cm^3
- 81 °C, C_b = 2.9 x 10^16 cm^3
- 66 °C, C_b = 3.0 x 10^15 cm^3
Doping-selective etching (ctnd.)

Disadvantage: requires high-dopant concentration to achieve good selectivity

<table>
<thead>
<tr>
<th>Etchant (Diluent)</th>
<th>Temperature (°C)</th>
<th>(100) Etch rate (μm/min) for boron doping ≪ 10^{19} \text{ cm}^{-3}</th>
<th>Etch rate (μm/min) for boron-doping \sim 10^{20}\text{ cm}^{-3}</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDP (H_2O)</td>
<td>115</td>
<td>0.75</td>
<td>0.015</td>
</tr>
<tr>
<td>KOH (H_2O)</td>
<td>85</td>
<td>1.4</td>
<td>0.07</td>
</tr>
<tr>
<td>NaOH (H_2O)</td>
<td>65</td>
<td>0.25–1.0</td>
<td>0.025–0.1</td>
</tr>
</tbody>
</table>
Electrochemical etching

Steps
1. Injection of holes into the semiconductor to raise it to a higher oxidation state Si⁺
2. Attachment of negatively charged hydroxyl groups, OH⁻, to the positively charged Si
3. Reaction of the hydrated silicon with the complexing agent in the solution
4. Dissolution of the reaction products into the etchant solution
Plot of electrochemical current density against voltage for silicon doped to different resistivities.
Electrochemical etch stop (ctnd.)

Current-voltage characteristics of n-Si and p-Si in KOH. No current flows at the OCP and the current stops above the passivating potential.
Example #1: fabrication of membranes

- Method to fabricate an array of thin membranes: (a) design of an oxide mask and (b) the electrochemical cell providing a back etch
Example #2: fabrication of cantilevers

Figure 5.15 Process flow of diffused pattern technique
Example #2: fabrication of cantilevers (ctnd.)

Figure 5.16  Process flow of etched-pattern technique
3. Overview of Microfabrication…TOC

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making (read)
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization
Plasma Etching

Figure 10-7 Schematic diagram of an RF-powered plasma etch system.
Plasma Induced Etching Process

Dissociation:
\[ \text{CF}_4 + \text{e}^- \rightarrow \text{CF}_3 + \text{F} + \text{e}^- \]

Dissociative ionization:
\[ \text{CF}_4 + \text{e}^- \rightarrow \text{CF}_3^+ + \text{F} + 2\text{e}^- \]

Ionization:
\[ \text{CF}_3 + \text{e}^- \rightarrow \text{CF}_3^+ + 2\text{e}^- \]

Excitation:
\[ \text{CF}_4 + \text{e}^- \rightarrow \text{CF}_4^* + \text{e}^- \]

Recombination:
\[ \text{CF}_3^+ + \text{F} + \text{e}^- \rightarrow \text{CF}_4 \]
\[ \text{F} + \text{F} \rightarrow \text{F}_2 \]
Plasma Induced Etching Process (ctnd.)

Etchant (Free Radical) Creation

e^- + OO → O

Etchant Transfer

Byproduct Removal

Film

Etchant Adsorption

Etchant/Film Reaction

Mask
Etched Structures

Advantages

- Good directional etching
- Good Selectivity of SiO2 to Si
SCREAM process overview

(a) Si substrate

(b) Si substrate

(c) Si substrate

(d) Si substrate
SCREAM process overview (ctnd.)

(e) Si substrate

(f) Aluminum

(g) Thermal SiO₂

(h) Si substrate

Aluminum

Thermal SiO₂

Photoresist

Aluminum

Silicon

Thermal SiO₂
Example of structures produced by SCREAM
3. Overview of Microfabrication...TOC

- **Pattern Transfer**
  - Optical Lithography
  - Design Rules
  - Mask Making (read)
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization
3. Overview of Microfabrication...TOC

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making (read)
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization (read)