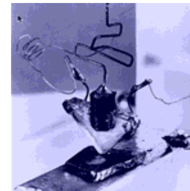
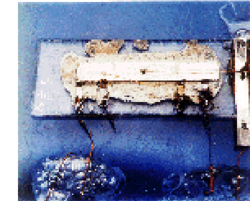
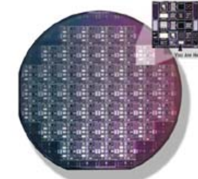
3. Overview of Microfabrication Techniques

The Si Revolution…

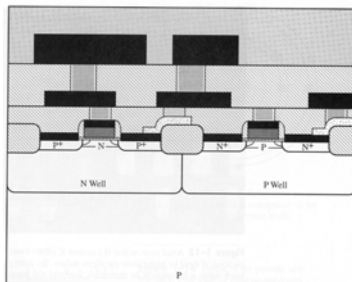

First Transistor
Bell Labs (1947)

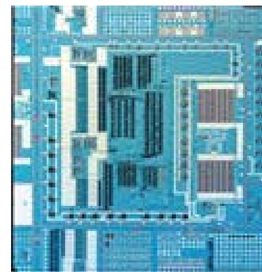

Si integrated circuits
Texas Instruments (~1960)


Modern ICs

More ? Check out:
http://www.pbs.org/transistor/background1/events/miraclemo.html
http://www.ti.com/corp/docs/company/history/firstic.shtml

The Need of Micropatterning



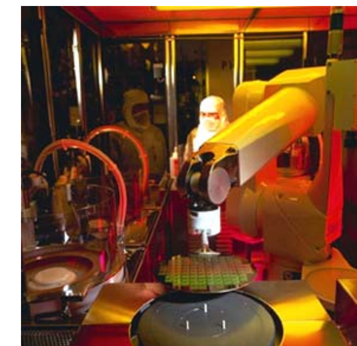


The batch fabrication of microstructures requires a low-cost, high throughput surface patterning technology

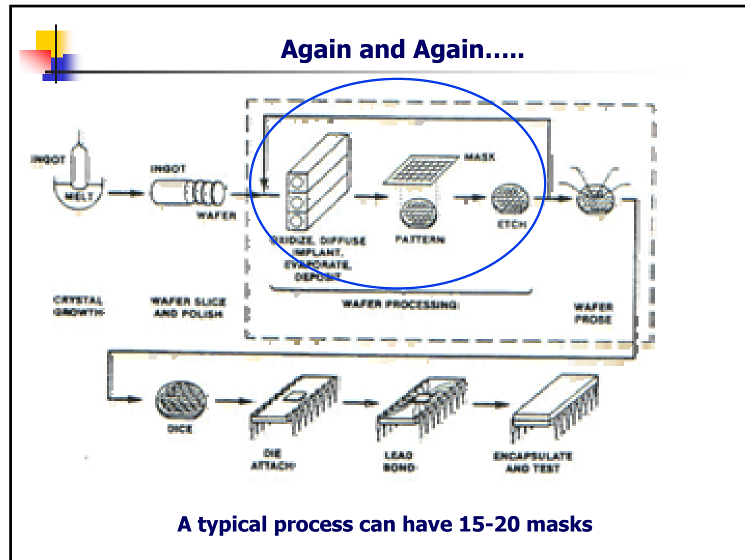
Microfabrication Process

Complete processing sequence consist of:

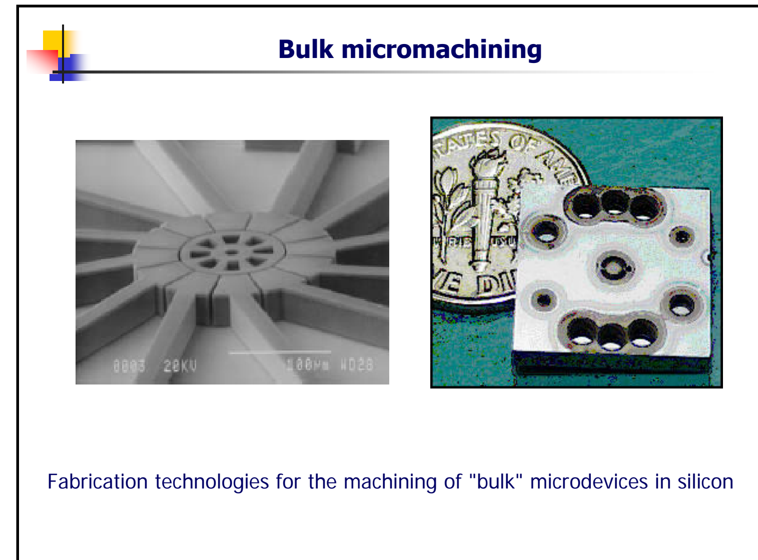
- **Layering:**
  - **Oxidation**
  - **Deposition**
- **Patterning:**
  - **Lithography**
  - **Etching**
- **Doping :**
  - **Ion Implantation**
  - **Diffusion**


Robotics arm is used to transfer wafers

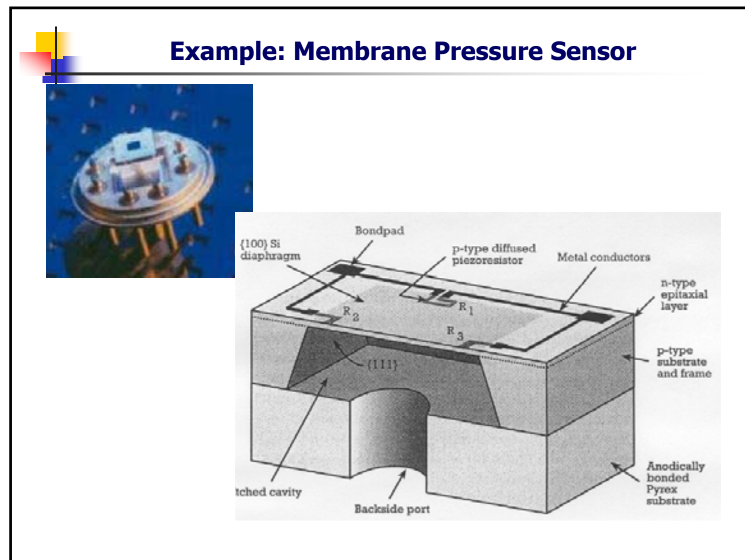
Check out: B. Van Zeghbroeck, "*Principles of Semiconductor Devices*"
W. Maly, "Atlas of IC Tech"



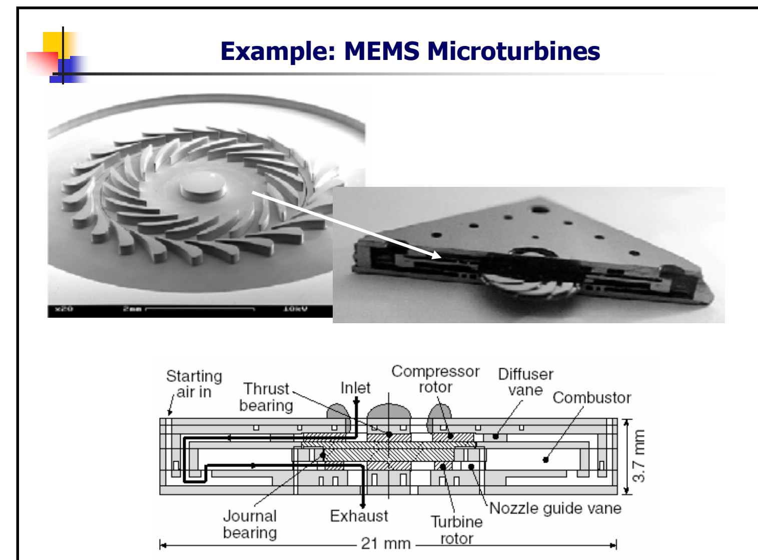
Again and Again.....
INGOT
MELT
INGOT
WAFER
CRYSTAL GROWTH
WAFER SLICE AND POLISH
MASK
PATTERN
ETCH
WAFER PROCESSING
WAFER PROBE
DICE
DIE ATTACH
LEAD BOND
ENCAPSULATE AND TEST
A typical process can have 15-20 masks



Bulk micromachining
Fabrication technologies for the machining of "bulk" microdevices in silicon



Example: Membrane Pressure Sensor
(100) Si diaphragm
Bondpad
p-type diffused piezoresistor
Metal conductors
n-type epitaxial layer
p-type substrate and frame
Anodically bonded Pyrex substrate
Backside port
(111)



Example: MEMS Microturbines
Starting air in
Thrust bearing
Inlet
Compressor rotor
Diffuser vane
Combustor
3.7 mm
Journal bearing
Exhaust
Turbine rotor
Nozzle guide vane
21 mm

3. Overview of Microfabrication...TOC

- Wafer-level Processes
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding

3. Overview of Microfabrication...TOC

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization

3. Overview of Microfabrication...TOC

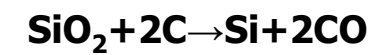
- Wafer-level Processes
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding

3. Overview of Microfabrication...TOC

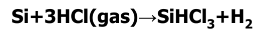
- Wafer-level Processes
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding

Growth of Silicon (ctnd.)

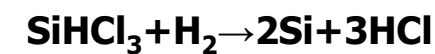
- Quartzite or SiO_2 (sand) is reacted in a furnace with carbon (from coke and/or coal) to make *metallurgical grade silicon* (MGS) which is about 98% pure, via the reaction:



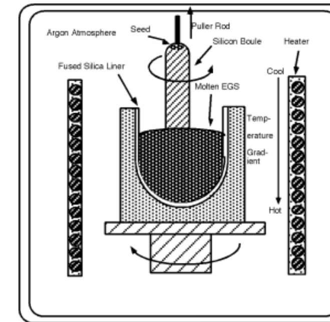
- The silicon is crushed and reacted with HCl (gas) to make trichlorosilane:



- Fractional distillation is then used to separate out the $SiHCl_3$ from most of the impurities. The (pure) trichlorosilane is then reacted with hydrogen gas to form pure electronic grade silicon (EGS):

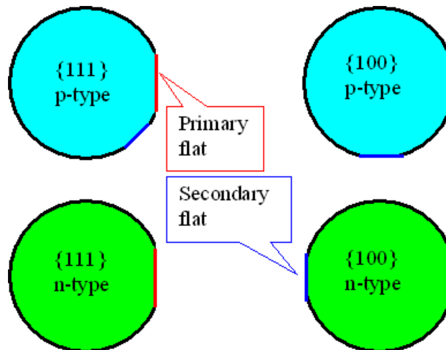


Growth of Silicon (ctnd.)



- The EGS is melted in a crucible, and then inserting a seed crystal on a rod called a puller which is then slowly removed from the melt.
- If the temperature gradient of the melt is adjusted so that the melting/freezing temperature is just at the seed-melt interface, a continuous single crystal rod of silicon, called a boule, will grow as the puller is withdrawn.

Growth of Silicon (ctnd.)



- The boule is grown down to a standard diameter. Flats are polished onto to boule to indicate crystalline orientation (above) before it is sliced into wafers

3. Overview of Microfabrication…TOC

- **Wafer-level Processes**
  - Substrates
  - **Wafer Cleaning**
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding

RCA cleaning of Si

The RCA cleaning procedure has three major steps used sequentially:

I. Organic Clean: Removal of insoluble organic contaminants with a 5:1:1 H_2O:H_2O_2:NH_4OH solution.

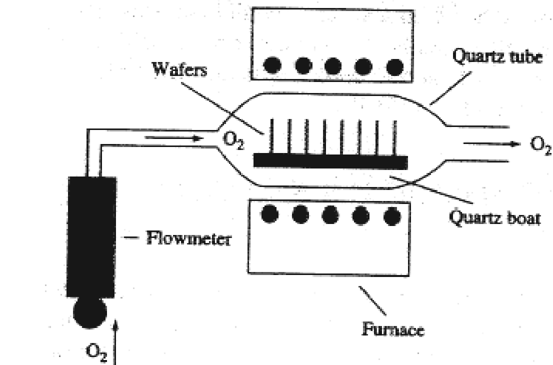
II. Oxide Strip: Removal of a thin silicon dioxide layer where metallic contaminants may accumulated as a result of (I), using a diluted 50:1 H_2O:HF solution.

III. Ionic Clean: Removal of ionic and heavy metal atomic contaminants using a solution of 6:1:1 H_2O:H_2O_2: HCl.

3. Overview of Microfabrication…TOC

- **Wafer-level Processes**
  - Substrates
  - Wafer Cleaning
  - **Oxidation**
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding

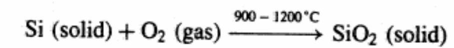
Thermal Oxidation



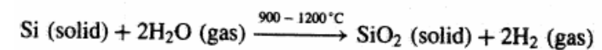
Thermal oxidation of silicon accomplished at high temperatures by flowing oxygen sources such as O_2 or H_2O

Thermal Oxidation (ctnd.)

Oxidation Reactions

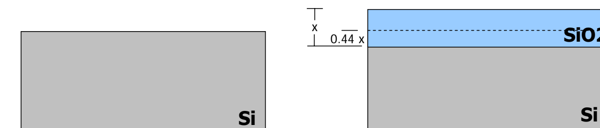


$$\text{Si (solid)} + \text{O}_2 \text{ (gas)} \xrightarrow{900-1200^\circ\text{C}} \text{SiO}_2 \text{ (solid)}$$



$$\text{Si (solid)} + 2\text{H}_2\text{O (gas)} \xrightarrow{900-1200^\circ\text{C}} \text{SiO}_2 \text{ (solid)} + 2\text{H}_2 \text{ (gas)}$$

The growth of an oxide layer of thickness x will consume 0.44 x of silicon



Thermal Oxidation (ctnd.)

Source Zone | Center Zone | Load Zone | Muffle | Oxidation Tube | Proportional Band Controller | Temp | Flat Zone | Distance

Horizontal Tube Furnace

Most popular furnace used for oxidation, diffusion, and heat treatments

Check out: Plummer, Deal Griffin, Silicon VLSI Technology, Chap 6

Thermal Oxidation (ctnd.)

Oxide Thickness – microns | Time – hours | 1200°C | 1100°C | 1000°C | 900°C | 800°C | 700 °C

Growth kinetics dictated by transport and diffusion of precursors at the Si/SiO2 interface

3. Overview of Microfabrication…TOC

- **Wafer-level Processes**
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - **Doping**
  - Thin-Film Deposition
  - Wafer Bonding

The Silicon Lattice

Si | Shared electrons of a covalent bond

The silicon atoms share valence electron through covalent bonds

Conduction in Intrinsic Silicon

Si Si Si Si Si
Hole
Free electron

electron conduction
hole conduction
Conventional current

At T = 0 K, all covalent electrons are localized to their co-valent bond, and therefore no conduction can take place.

At T > 0 K (above left), thermal agitation can be sufficient for some electrons to break away from the covalent bonds, and can freely drift around the lattice

These conduction electrons leave behind a "hole" in the covalent bond, which can also "move" by having nearby covalent electrons hop into the empty state

When a field is applied (above right), the conduction electrons drift in one direction, while the holes drift in the opposite ones

Band Structure : Intrinsic Material at T > O K

Hole
Free electron
E(k)
E_f

At T > 0 K, thermal agitation can be sufficient for some electrons to break away from the covalent bonds, and can freely drift around the lattice.

This will populate the conduction band with electrons, and the valence band with empty orbitals ("holes"), in equal amount (n = p)

intrinsic (T > 0 K)

Doping of Semiconductors: n-type

Si
Sb
Donor impurity contributes free electrons
E(k)
E_f

An impurity with extra valence electron releases this electron in lattice, therefore creating a surplus of electrons over holes (n > p)

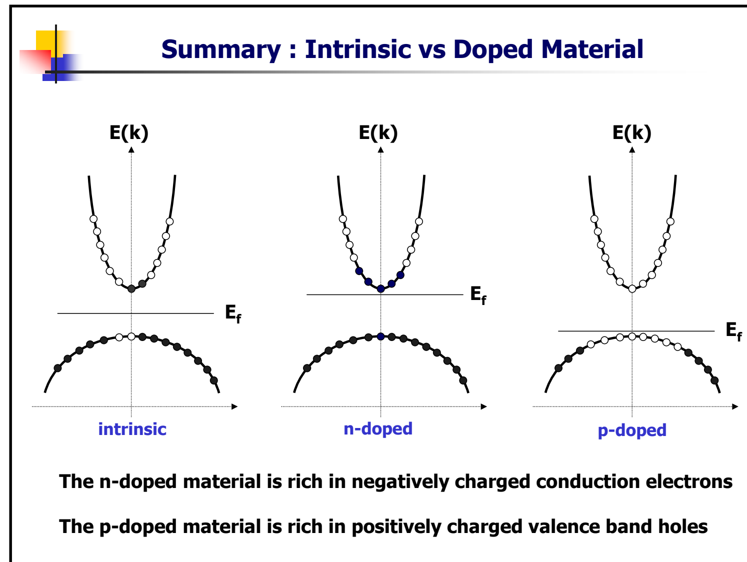
n-doped

Doping of Semiconductors: p-type

Si
B
Acceptor impurity creates a hole
E(k)
E_f

An impurity with less valence electrons creates a vacant state in the valence band therefore creating a surplus of holes over electrons (p > n)

p-doped



Introduction of Dopants

- **Local modification of the material doping type and level**
- **Two methods are used:**
  - **Diffusion**
  - **Ion Implantation**
- **Advantage of implantation:**
  - **less under-diffusion**
  - **shallower junction**
  - **better control of depth (energy)**
  - **better control of concentration (dose)**

oxide

p-Si

P

oxide

n⁺-Si

p-Si

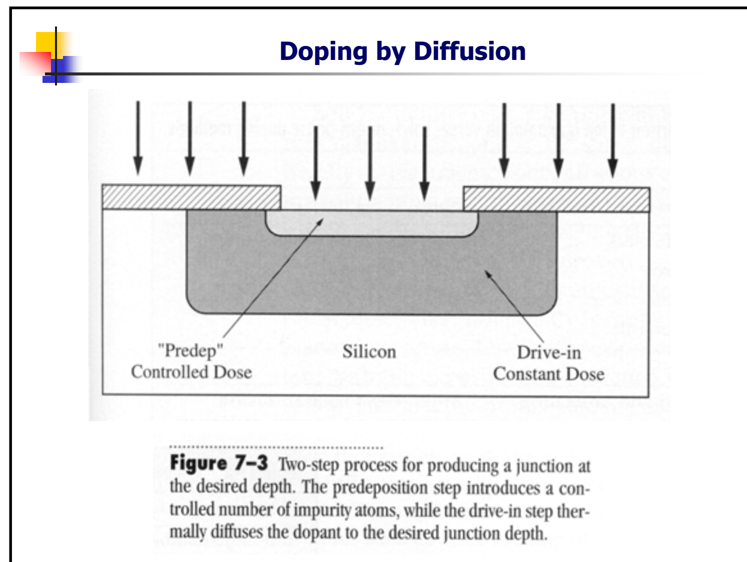


Figure 7–3 Two-step process for producing a junction at the desired depth. The predeposition step introduces a controlled number of impurity atoms, while the drive-in step thermally diffuses the dopant to the desired junction depth.

Diffusion Process

The diffusion process is ideally described in terms of Fick's diffusion equation:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2}$$

where *C* is the dopant concentration, *D* is the diffusion coefficient, *t* is time, and *x* is measured from the water surface in a direction perpendicular to the surface.

The initial conditions of the concentration $C(0,t) = 0$ at time $t = 0$ and the boundary conditions are that surface concentration $C(0,t) = C_s$ (the solubility of the dopant) at surface and that a semi-infinite medium has $C(\infty,t) = 0$. The solution that satisfies the initial and boundary conditions is given by:

$$C(x,t) = C_S erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$

where erfc is the complementary error function and the diffusion coefficient *D* is a function of temperature *T* expressed as:

$$D = D_0 \exp\left(\frac{-E_A}{kT}\right)$$

The total dose being diffused into semiconductor is:

$$Q = \int_0^\infty C(x,t)\partial x = \frac{2C_s}{\sqrt{\pi}}\sqrt{Dt}$$

where E_a is the activation energy of the thermally driven diffusion process, *k* is Boltzmann's constant, and *D* is the diffusion constant.

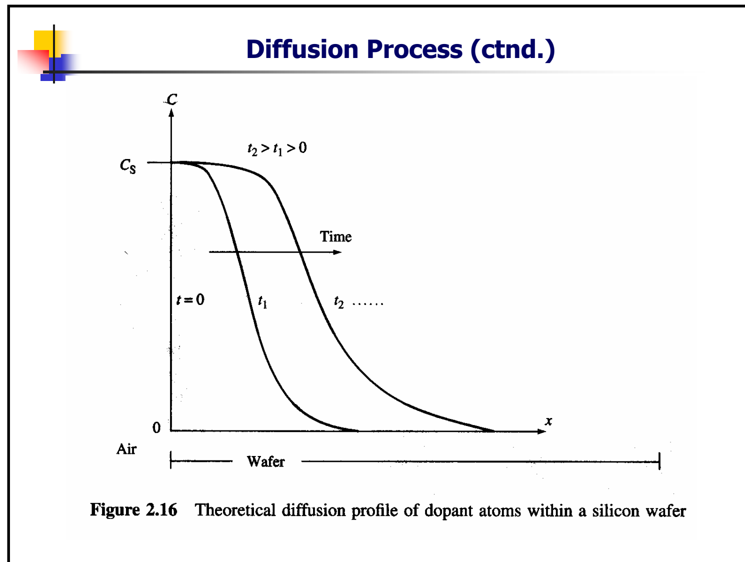


Figure 2.16 Theoretical diffusion profile of dopant atoms within a silicon wafer

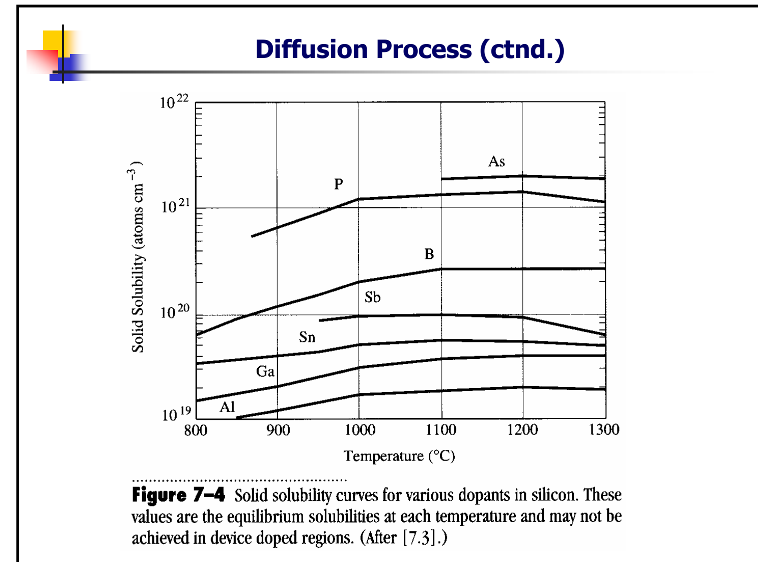


Figure 7–4 Solid solubility curves for various dopants in silicon. These values are the equilibrium solubilities at each temperature and may not be achieved in device doped regions. (After [7.3].)

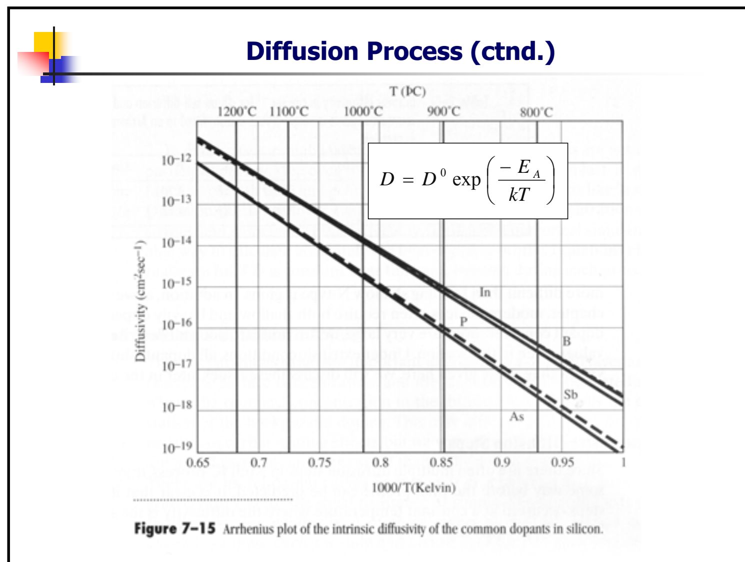


Figure 7–15 Arrhenius plot of the intrinsic diffusivity of the common dopants in silicon.

Numerical Example

Q: A p-type (boron) diffusion is performed in silicon as follows for 30 min at 900°C. What is the deposited Q? Assume that the solid solubility is maintained at the surface (x=0)

Solution:

According to figures above, the boron diffusion coefficient is:

at 900°C: $D_B^{900} = 1.0 \exp\left(-\frac{3.5}{k(900+273)}\right) = 9.27 \times 10^{-16} cm^2 s^{-1}$

The deposition is performed at 900°C where the boron solid solubility from Table 7.4 is: $C_S = 1.2 \times 10^{20} cm^{-3}$

The dose introduced is then:

$$Q = \frac{2C_S}{\sqrt{\pi}}\sqrt{Dt} = \frac{2(1.2 \times 10^{20})}{\sqrt{\pi}}\sqrt{(9.27 \times 10^{-16})(30 \times 60)} = 1.75 \times 10^{14} cm^{-2}$$

Doping by Ion Implantation

Ga+ Ga+ Ga+ Ga+ Ga+

Si

VACUUM SEMICONDUCTOR (a)

ION BEAM R X

R_p

LOG ION CONCENTRATION (b)

$n(R_p)$ GAUSSIAN

$0.6n(R_p)$ σ_p

ION BEAM O R_p X

Y

Allows precise control over dose and depth of doping layer

Doping by Ion Implantation (ctnd.)

Doping profile controlled by implantation energy

Check out: Ion Implantation : A General Overview, National University of Singapore

Doping by Ion Implantation (ctnd.)

Mass Analyzing Slit

Ion Acceleration Column

Electronic Scanning

Magnet

Magnetic Quadrupole Lenses

End Station

Ion Extraction/ Pre-Acceleration

Magnet

Filament (Cathode)

Ion Source

Elemental Source

Chamber

Plasma

Ion Implantation Process

The distribution is approximated at first order by a symmetric Gaussian distribution:

$$C(x) = C_p \exp\left(-\frac{(x-R_p)^2}{2\Delta R_p^2}\right)$$

where R_p is the average projected range normal to the surface, ΔR_p is the standard deviation or straggle about that range, and C_p is the peak concentration where the Gaussian is centered. Range and standard deviation for common dopants in silicon are shown in next two slides. The total number of ions implanted is defined as the dose and is simply:

$$Q = \int_{-\infty}^{\infty} C(x)dx$$

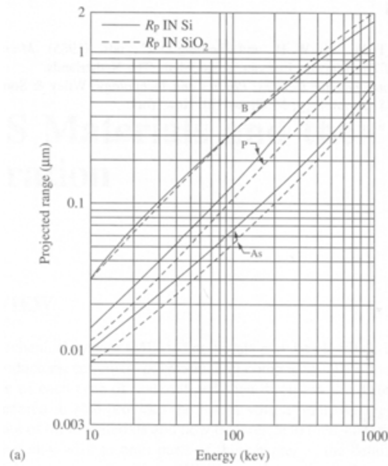
Making use of the fact that the sum (or integral) of Gaussian functions is an error function, and using the formula which defines the error function gives

$$\int_{-\infty}^{\infty} \exp^{-u^2} du = \frac{\sqrt{\pi}}{2}[erf(\infty) - erf(-\infty)]$$

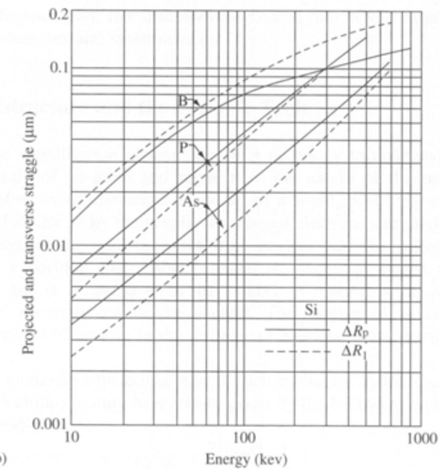
so that

$$Q = \sqrt{2\pi}\Delta R_p C_p$$

Ion Implantation Process (ctnd.)



Ion Implantation Process (ctnd.)



Ion Implantation Process (ctnd.)

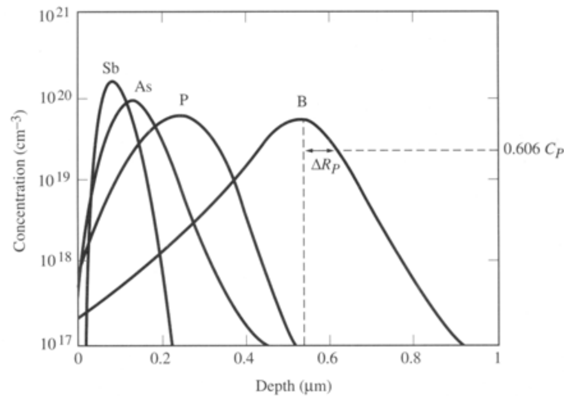


Figure 8–2 Distribution of ions implanted into crystalline silicon at an energy of 200 keV. The light ions travel further and have a broader distribution than the heavy ions.

Numerical Example

Q: Arsenic is implanted into a lightly doped p-type Si substrate at an energy of 75 keV. The dose is 1×10^{14} cm^{-2}. The Si substrate is tilted 7° with respect to the ion beam to make it appear amorphous. The implanted region is assumed to be rapidly annealed so that complete electrical activation is achieved. What is the peak electron concentration produced?

A: From above graphs, the range and standard deviation for 75 keV arsenic are

$$R_P = 0.05\mu m \qquad \Delta R_P = 0.02\mu m$$

The peak concentration is:

$$C_P = \frac{Q}{\sqrt{2\pi}\,\Delta R_P} = \frac{1 \times 10^{14}}{\sqrt{2\pi}\left(0.02 \times 10^{-4}\right)} = 2 \times 10^{19}\ cm^{-3}$$

Assuming all the dose is active, then the peak electron concentration is equal to the peak dopant concentration.

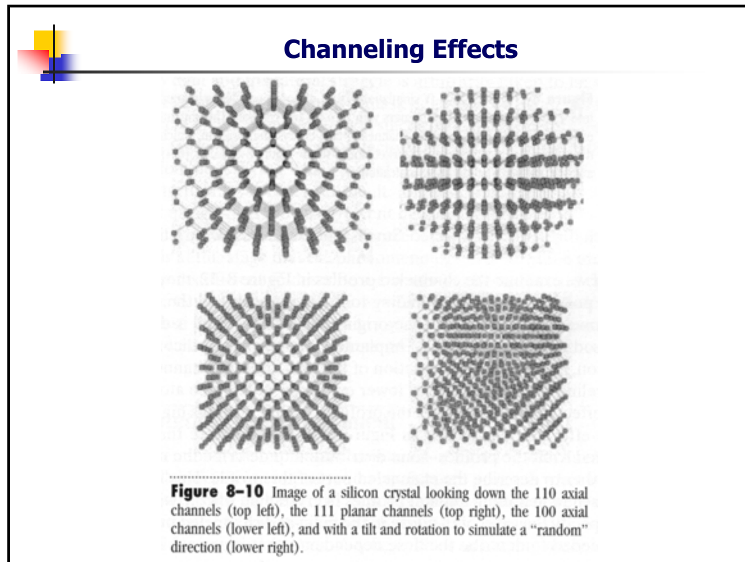


Figure 8–10 Image of a silicon crystal looking down the 110 axial channels (top left), the 111 planar channels (top right), the 100 axial channels (lower left), and with a tilt and rotation to simulate a "random" direction (lower right).

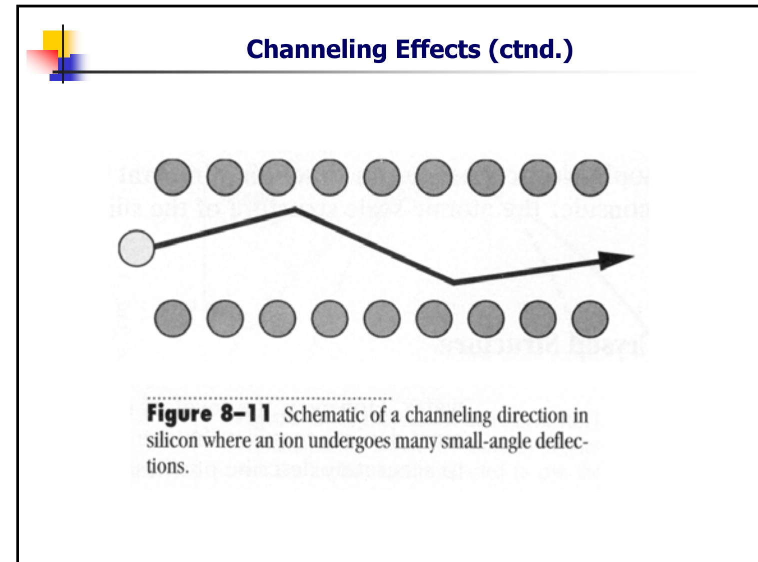


Figure 8–11 Schematic of a channeling direction in silicon where an ion undergoes many small-angle deflections.

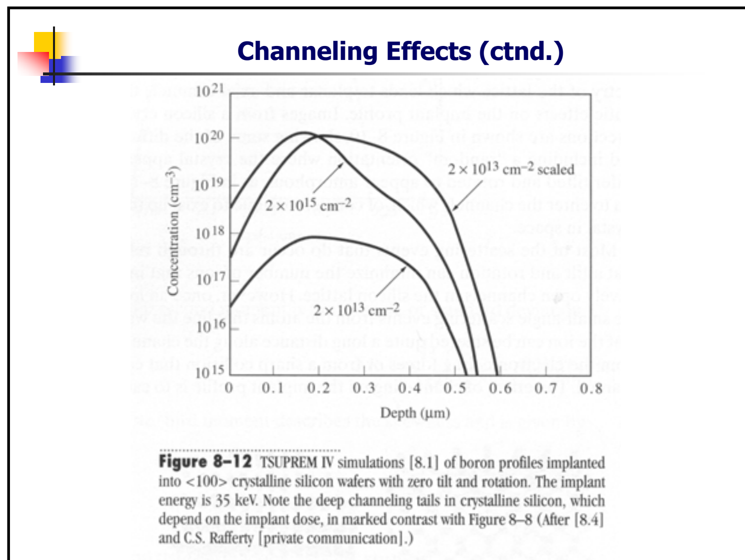
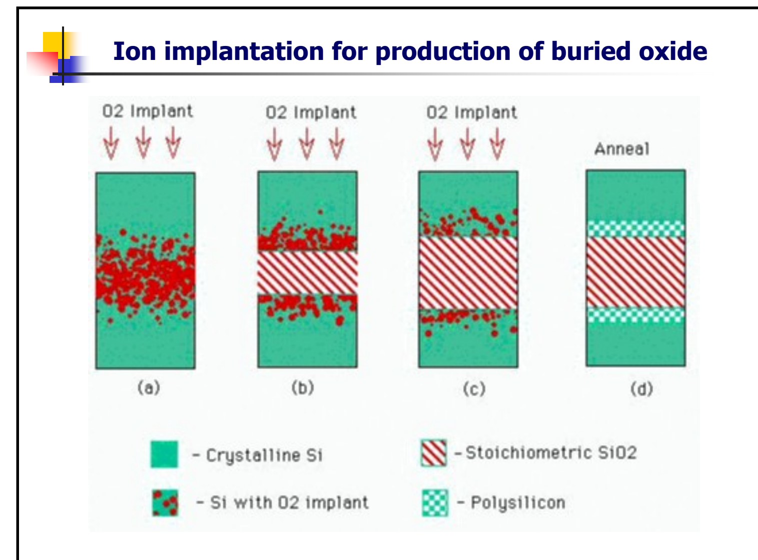
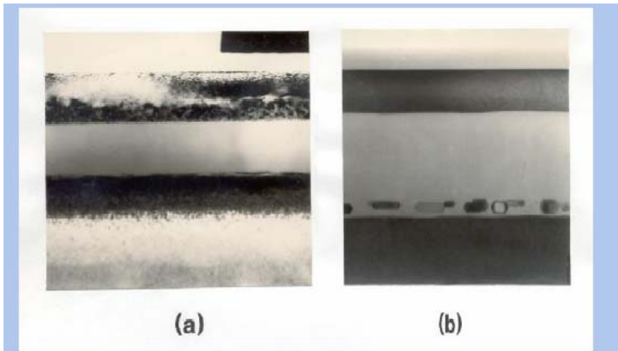


Figure 8–12 TSUPREM IV simulations [8.1] of boron profiles implanted into <100> crystalline silicon wafers with zero tilt and rotation. The implant energy is 35 keV. Note the deep channeling tails in crystalline silicon, which depend on the implant dose, in marked contrast with Figure 8–8 (After [8.4] and C.S. Rafferty [private communication].)

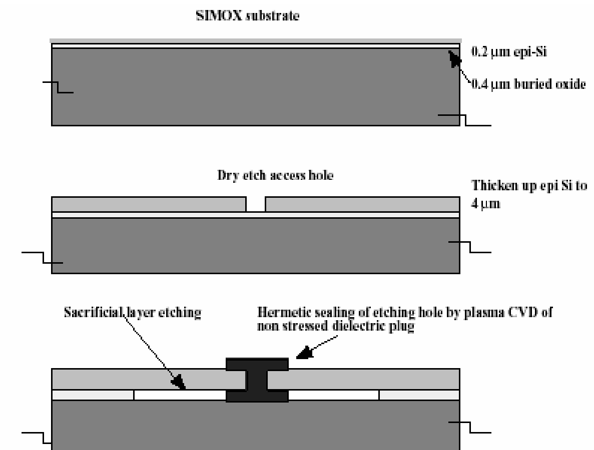


Cross-section of SIMOX wafers



(a) As implanted : 1.7E18/cm2, 200keV, 520C
(b) Annealed : 1320C, 4hrs

SIMOX wafers for MEMS devices



3. Overview of Microfabrication…TOC

- **Wafer-level Processes**
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - **Thin-Film Deposition**
  - Wafer Bonding

Electronics Materials

Typical IC materials include:

Thermal Oxides (covered previously)

Other Dielectric Materials

Polycrystalline silicon (Poly-Si)

Metals

Electronics Materials

Typical IC materials include:

Thermal Oxides (covered previously)

Other Dielectric Materials

Polycrystalline silicon (Poly-Si)

Metals

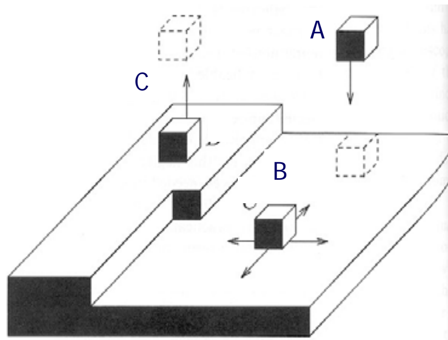
Chemical Vapor Deposition

- SiO_2
  - Field oxide
  - interlevel insulator
  - passivation (overcoat layer)
- Si_3N_4
  - Local oxidation mask
  - protective overcoat layer
  - gate dielectric
- Poly-Si
  - gate material in MOSFET
- Metallization
  - interconnections
- Epitaxial layers
  - Si
  - Ge
  - GaAs
  - GaP

Purpose: Low temperature deposition of insulators & conductors

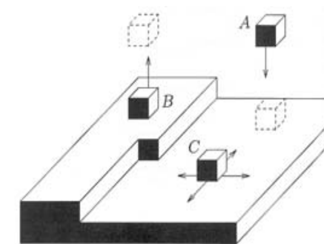
Check out: Plummer, Deal Griffin, Silicon VLSI Technology, Chap 9

Chemical Vapor Deposition (ctnd...)

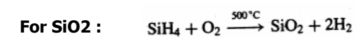


A : Gaseous transport and adsorption of precursor
B: Surface transport and reaction
C: Desorption of by-products

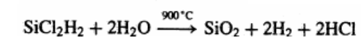
Chemical Vapor Deposition (ctnd...)



For SiO2 :

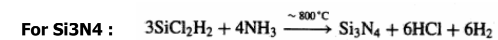


$$SiH_4 + O_2 \xrightarrow{500^\circ C} SiO_2 + 2H_2$$



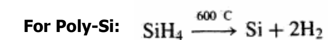
$$SiCl_2H_2 + 2H_2O \xrightarrow{900^\circ C} SiO_2 + 2H_2 + 2HCl$$

For Si3N4 :



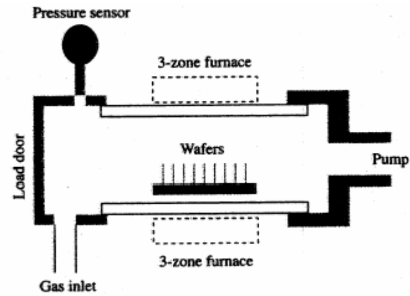
$$3SiCl_2H_2 + 4NH_3 \xrightarrow{\sim 800^\circ C} Si_3N_4 + 6HCl + 6H_2$$

For Poly-Si:



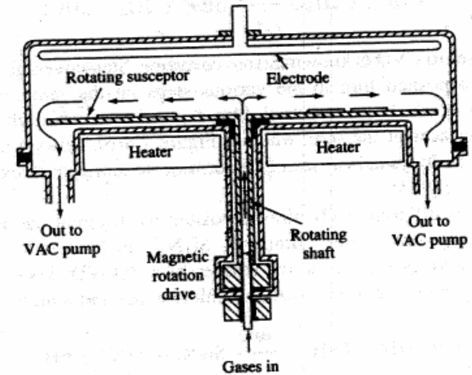
$$SiH_4 \xrightarrow{600\ C} Si + 2H_2$$

Low-Pressure CVD (LPCVD)



1. Pressure between 0.2 and 2.0 torr
2. Gas flow between 1 to 10 cm^3/s
3. Temperatures between 300 and 900 °C

Plasma-Enhanced CVD (PECVD)



Deposition of material physically assisted by RF plasma

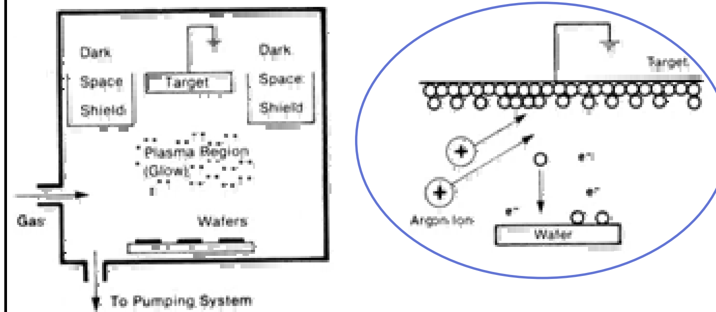
Allows lower deposition temperatures

Properties of Oxide Films

Table 2.1 Properties of deposited and thermally grown oxide films (Sze 1985)

Property	Composition	Step coverage	Density ρ (g/cm^3)	Refractive index n_r	Dielectric strength (V/cm)
Thermally grown at 1000 °C	SiO_2	–	2.2	1.46	$>10^{-5}$
Deposited by $SiH_4 + O_2$ at 450 °C	$SiO_2(H)$	Nonconformal	2.1	1.44	8×10^{-6}
Deposited by TEOS at 700 °C	SiO_2	Conformal	2.2	1.46	10^{-5}
Deposited by $SiCl_2H_2 + N_2O$ at 900 °C	SiO_2	Conformal	2.2	1.46	10^{-5}

Sputtering



Ar atoms are ionized at low pressure by an electric field.

The positive ions are accelerated towards the negatively charged target:

Sputtered material condenses on the ambient surfaces

Electronics Materials

Typical IC materials include:

Thermal Oxides

Dielectric Materials

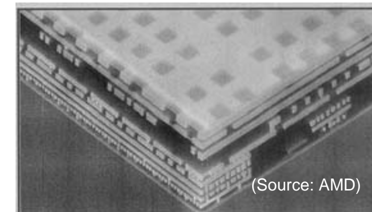
Polycrystalline silicon (Poly-Si)

Metals

Metallization

- Purpose: interconnecting the devices to form a circuit
- Use low resistance metal layers:
  - Aluminum alloys
  - Silicides
  - Copper
- Important issues:
  - resistivity
  - electromigration
  - planarity

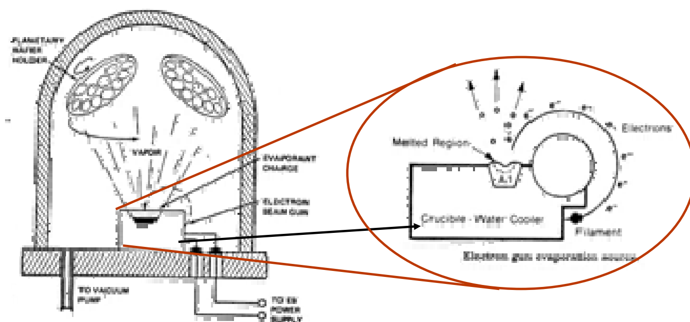
Nine levels of metallization
(with low-k dielectric and SiC-based barriers)


(Source: AMD)

- Copper introduced in 2001 by IBM
- Lower resistance than Aluminum
- Less interconnection delays on chip
- Higher clock frequencies possible

Check out: Plummer, Deal, Griffin, Silicon VLSI Technology, Chap 11

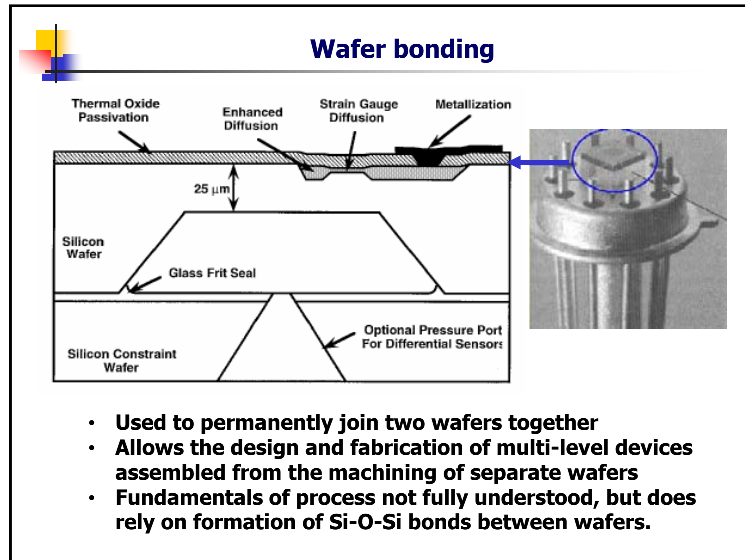
Metallization by Evaporation



3. Overview of Microfabrication...TOC

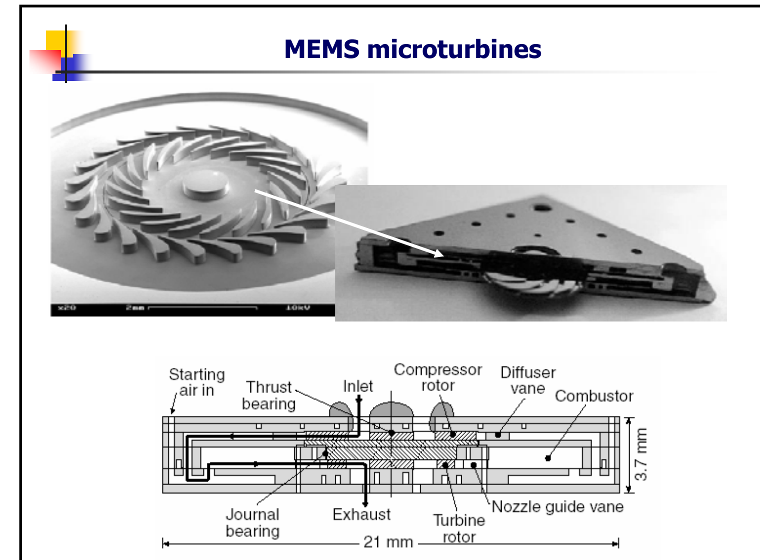
- **Wafer-level Processes**
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - **Wafer Bonding**

Wafer bonding

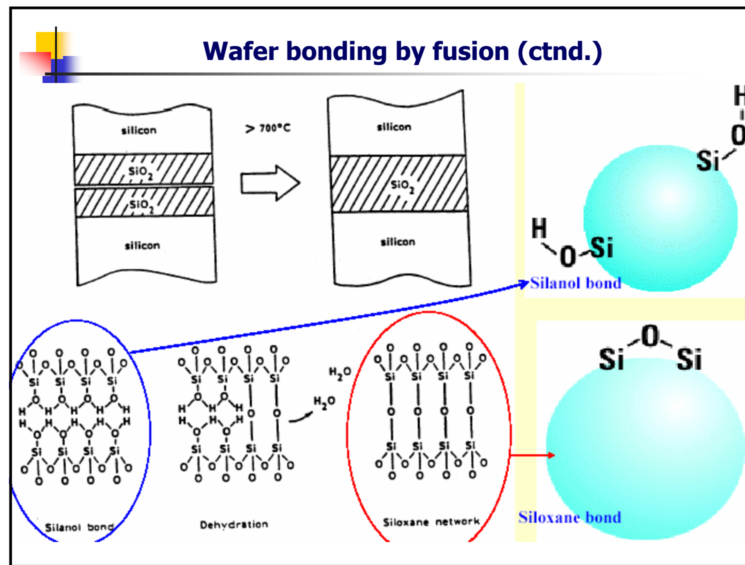


- **Used to permanently join two wafers together**
- **Allows the design and fabrication of multi-level devices assembled from the machining of separate wafers**
- **Fundamentals of process not fully understood, but does rely on formation of Si-O-Si bonds between wafers.**

MEMS microturbines



Wafer bonding by fusion (ctnd.)



Fusion bonding procedures

- **1.** Surface treatment to make hydrophilic surfaces **by soaking wafers in Piranha, diluted sulfuric acid, or boiling nitric acid, or hydrophobic surfaces in HF. Hydrophilic top layer consisting of O-H bonds (hydroxyl) is formed on the oxide surface.**
- **2.** Contacting the wafers **in clean air at room temperature after rinsing and drying them. Self-bonding (hydrogen bonding) is formed throughout the wafer surfaces without external pressure with considerable forces.**
- **3.** Annealing (> 800°C) **in oxidizing or nonoxidizing ambient. Water molecules come out and the voids (intrinsic) are observed beyond 200°C. The voids tend to disappear and bonding strength is increased at more than 300°C forming siloxane (Si-O) bonds. At high temperatures (>800 °C), Oxygen at the interface may diffuse into the silicon bulk to form Si-Si bonds like single crystal silicon at above 1000°C.**

Wafer Bonding by Fusion

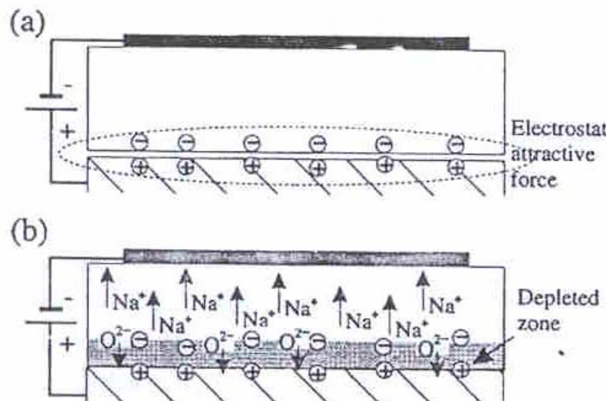
Table 5.4 Bond quality data taken from Harendt *et al.* (1991)

Structure	Annealing temperature (°C)	Bond strength (Jm^{-2})	Voids (% nonbonding)
Si/Si	450	0.5	–
Si/Si	800	0.6	0.3
Si/Si	1000	2.6	0.3
Si/Si_3N_4(140 nm)	800	0.9	0.2
Si/Si_3N_4(140 nm)	1000	Cleavage	0.2
Si/Si_3N_4(300 nm)	1000	Cleavage	25

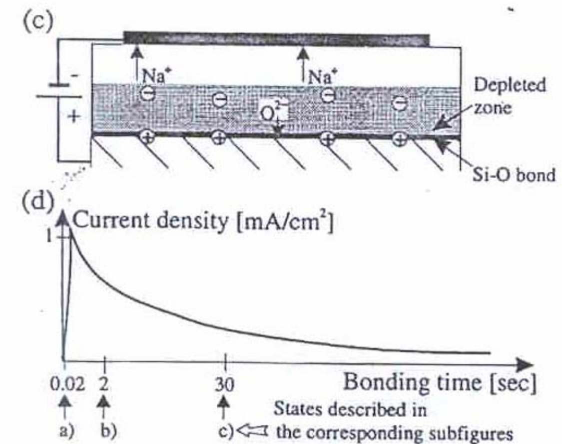
Thermal Considerations in Fusion Bonding

1. **Temperature less than 450°C for postmetallisation wafers.**
2. **Temperature less than 800°C for wafers with diffusion dopant layers (e.g. p^+ etch-stop layers).**
3. **Temperature greater than 1000°C for wafer bonding before processing. According to the reaction mechanism, annealing at temperatures above 1000°C for several hours should result in an almost complete reaction of the interface. A 1000°C anneal for about two hours gives sufficiently high bond strength for all subsequent treatments (Harendt *et al.* 1991); it is not possible to separate the two bonded Si wafers without breaking the silicon.**

Anodic Bonding : Principle



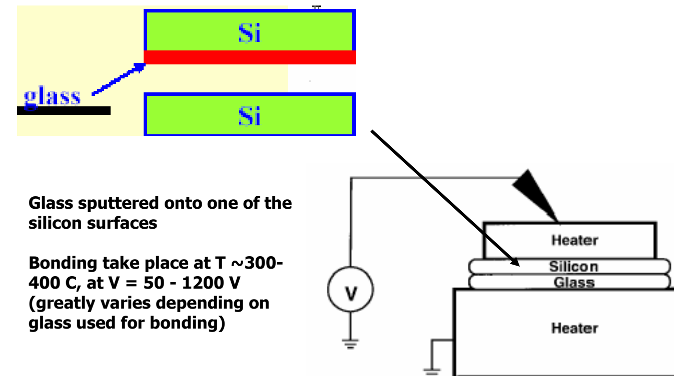
Anodic Bonding : Principle (ctnd.)



Anodic Bonding : Principle (ctnd.)

- General Principles**: Due to the elevated temperature, the Na+ ions are mobile enough for the Pyrex to behave like a conductor. Hence, in the very first moment, most of the voltage applied to the silicon-Pyrex sandwich drops across a small gap of a few microns between the two surfaces.**
- **The high electric field in this area creates a strong electrostatic force, pulling the two surfaces together and thus forming an intimate contact.**
- **In addition Na+ ions start drifting to the negative electrode, which is connected with glass, creating depletion zone adjacent to the silicon, positive electrode.**
- **During this charging process, the electric field is high enough to allow a drift of oxygen to the positive electrode (Si) reacting with silicon and creating Si-O bond.**

Anodic Bonding Setup



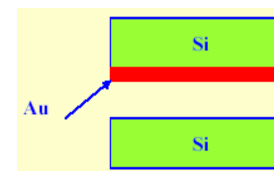
Glass sputtered onto one of the silicon surfaces

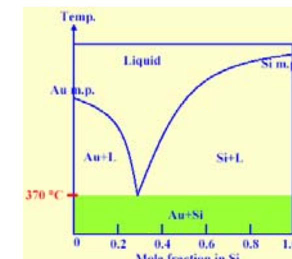
Bonding take place at T ~300-400 C, at V = 50 - 1200 V (greatly varies depending on glass used for bonding)

Anodic Bonding : Procedure

- **Typical Variables: temperature, applied voltage, bonding load, voltage-applying time, bonding area, glass thickness. 300 – 400 °C, 700-1200V. (FYI: Temperature limit for IC processed Si substrates is about 450 °C)**
- **General conditions: Silicon + Pyrex 7740, 400 °C, and 1000V.**
- **Requirements:**
  - **Microroughness (Ra) < 1μm. Warp/bow < 5μm**
  - **The native or thermal oxide layer on the Si must be thinner than 2000Å.**
- **Benefits:**
  - **Lower temperature process and popular and reliable process**
  - **Less stringent requirement for the surface quality of the wafers.**

Alternate Bonding Technique : Eutectic Bonding





One wafer coated with Au prior to bonding
Temperature is raised until the Eutectic point is reached
Above eutectic temperature, Au will diffuse into Si (and not other way around
An Au-Si eutectic alloy is then formed between the two wafers
Other Si-metal alloys eutecic bonding also possible

IR Monitoring of Bonded Wafers

Quality of bonds is usually monitored using infrared absorption imaging

Worked Example : Floating Element Shear Sensor

- **(a) Angled view and (b) cross section of a floating sensor based on a rectangular plate with four tethers**

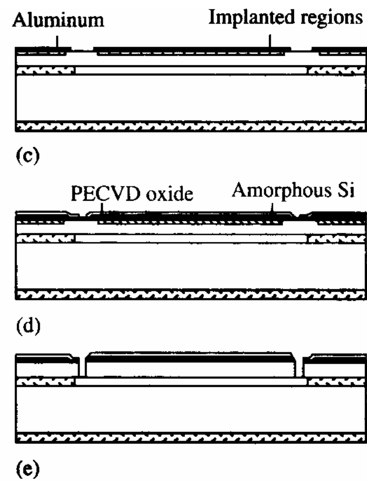
Worked Example : Floating Element Shear Sensor

Figure 2: Schematic plan view and cross-section of a typical floating-element sensor.

A better view of geometry of such device

Worked example : Floating Element Shear Sensor

Worked example : Floating Element Shear Sensor



3. Overview of Microfabrication…TOC

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization

3. Overview of Microfabrication…TOC

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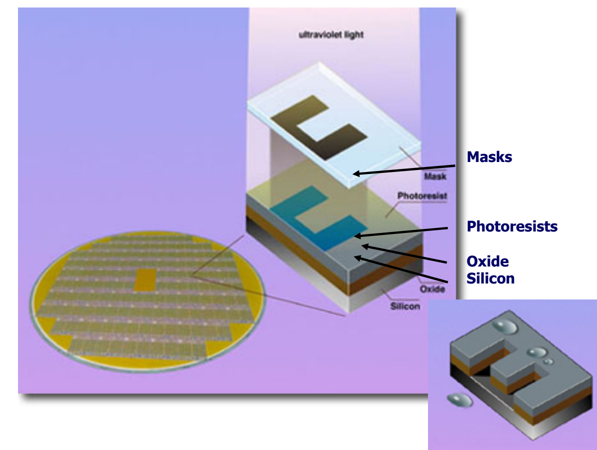
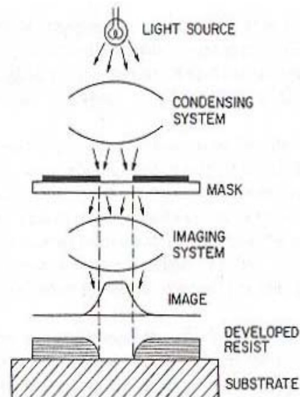
Lithography



Elements of Photolithography



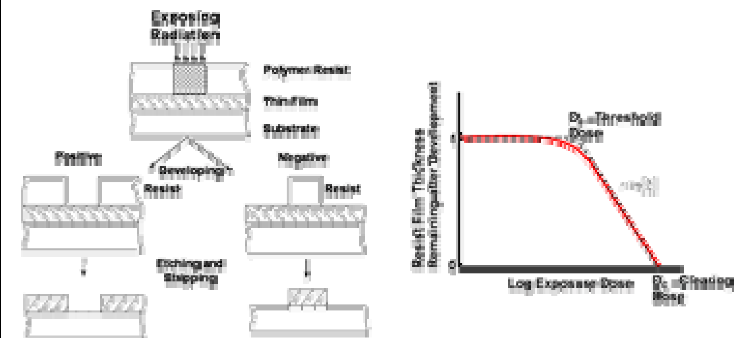
Elements of Photolithography (ctnd.)

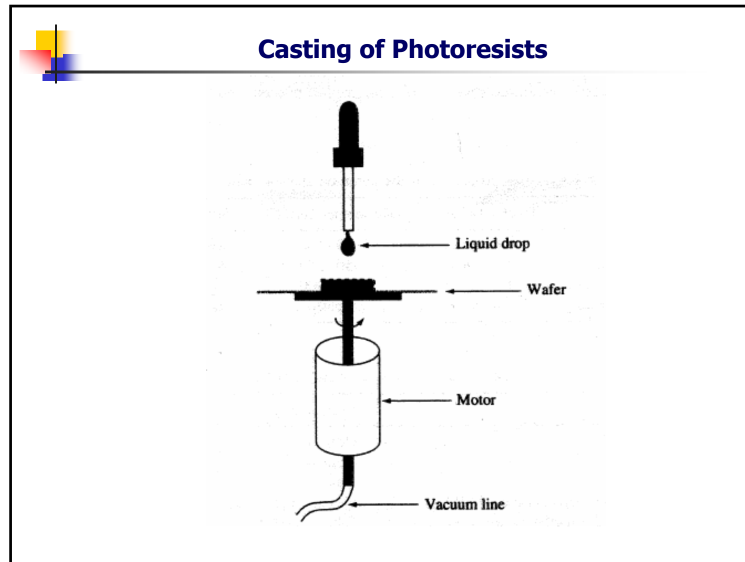
- ***Lithography*** **consists of patterning substrate by employing the interaction of beams of photons or particles with materials.**
- ***Photolithography*** **is widely used in the integrated circuits (ICs) manufacturing.**
- **The process of IC manufacturing consists of a series of 10-20 steps or more, called *mask layers* where layers of materials coated with resists are patterned then transferred onto the material layer.**

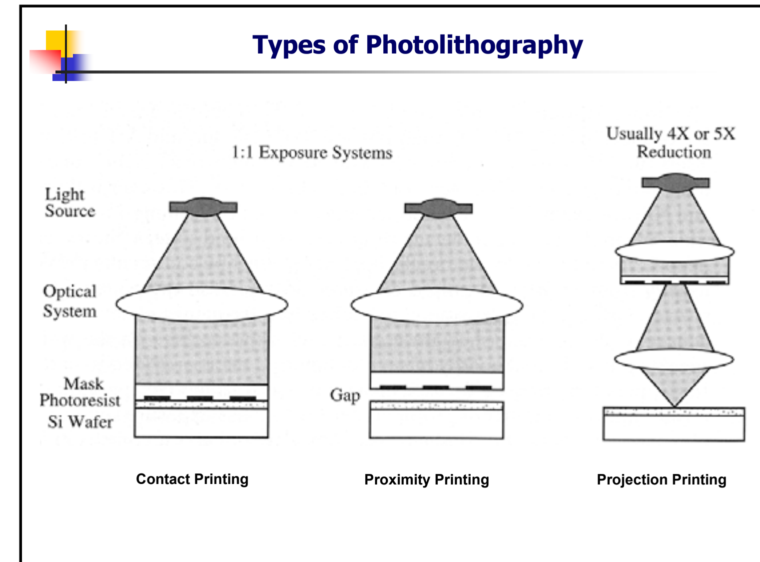
Elements of photolithography (ctnd.)

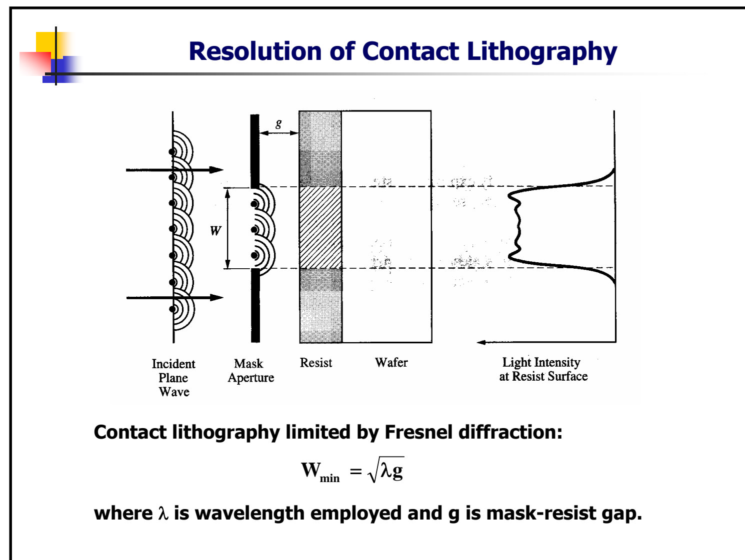
- **A photolithography system consists of a light source, a mask, and a optical projection system.**
- ***Photoresists*** **are radiation sensitive materials that usually consist of a photo-sensitive compound, a polymeric backbone, and a solvent.**
- **Resists can be classified upon their solubility after exposure into: *positive resists* (solubility of exposed area increases) and *negative resists* (solubility of exposed area decreases).**

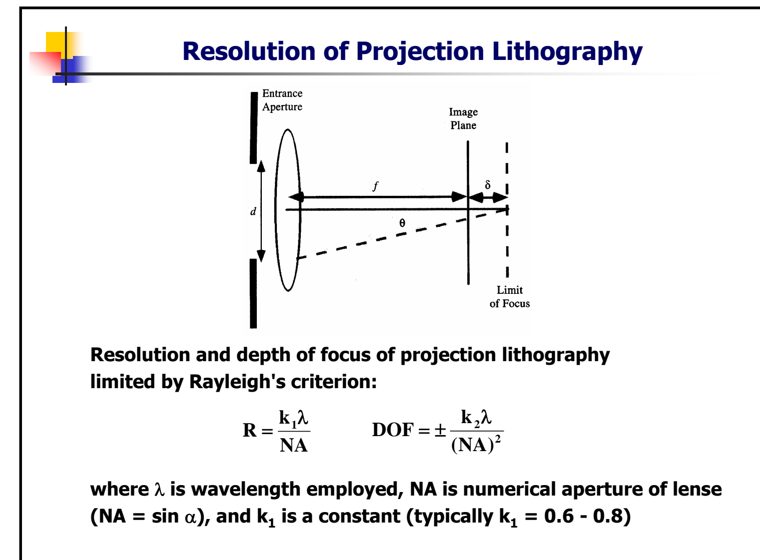
Positive vs. Negative Photoresists




Casting of Photoresists
Liquid drop
Wafer
Motor
Vacuum line


Types of Photolithography
1:1 Exposure Systems
Usually 4X or 5X Reduction
Light Source
Optical System
Mask
Photoresist
Si Wafer
Gap
Contact Printing
Proximity Printing
Projection Printing


Resolution of Contact Lithography
g
W
Incident Plane Wave
Mask Aperture
Resist
Wafer
Light Intensity at Resist Surface
Contact lithography limited by Fresnel diffraction:
$W_{min} = \sqrt{\lambda g}$
where λ is wavelength employed and g is mask-resist gap.


Resolution of Projection Lithography
Entrance Aperture
Image Plane
f
δ
d
θ
Limit of Focus
Resolution and depth of focus of projection lithography limited by Rayleigh's criterion:
$R = \frac{k_1\lambda}{NA}$ $DOF = \pm\frac{k_2\lambda}{(NA)^2}$
where λ is wavelength employed, NA is numerical aperture of lense (NA = sin α), and k_1 is a constant (typically k_1 = 0.6 - 0.8)

Numerical Example

Q: Estimate the resolution and depth of focus of a state-of-the-art excimer laser stepper using a KrF light source (λ = 248 nm) with a NA= 0.6. Assume k_1 = 0.75 and k_2= 0.5.

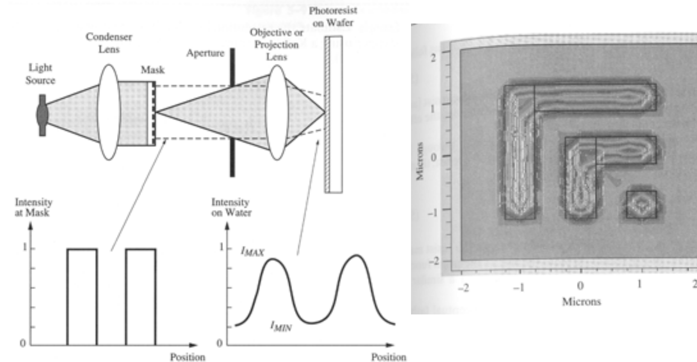
Answer

$$R = k_1 \frac{\lambda}{NA} = 0.75\left(\frac{0.248\ \mu\text{m}}{0.6}\right) = 0.31\ \mu\text{m}$$

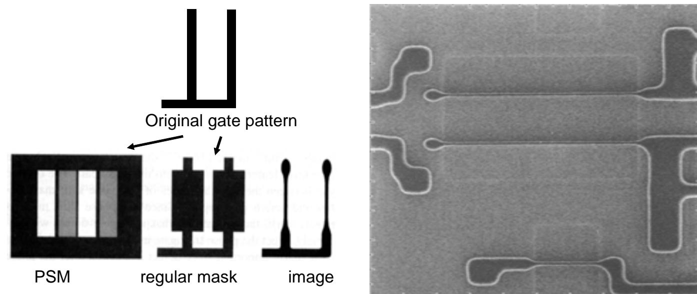
$$\text{DOF} = \pm\, k_2 \frac{\lambda}{(NA)^2} = \pm 0.5\left[\frac{0.248\mu m}{(0.6)^2}\right] = \pm 0.34\mu m$$

- Using additional technical "tricks" like off- axis illumination, the resolution can be pushed below 0.25 μm, suitable for the SIA NTRS 0.25 μm generation.
- Further improvements can be obtained through more sophisticated mask designs using concepts like optical proximity correction and phase shift masks.
- The depth of focus is on the same order as the resist layer thickness itself and therefore requires very flat topography and careful attention in the stepper to keep the image plane focused by adjusting the height of the wafer with respect to the lens.

Resolution of Photolithography (ctnd.)

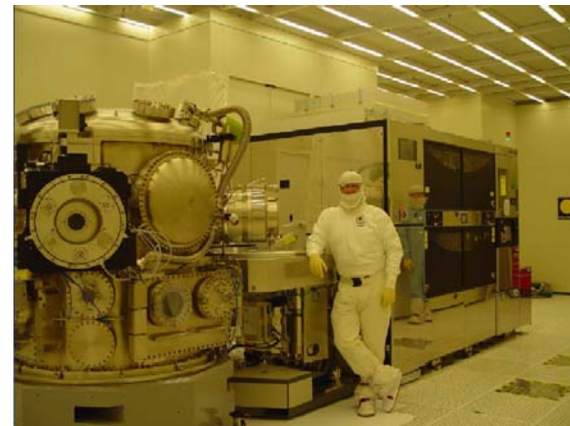


Resolution Enhancement : Phase Shift Masks



120 nm wide gates produced using λ = 248 nm radiation and PSM masks

EUV Lithography System...

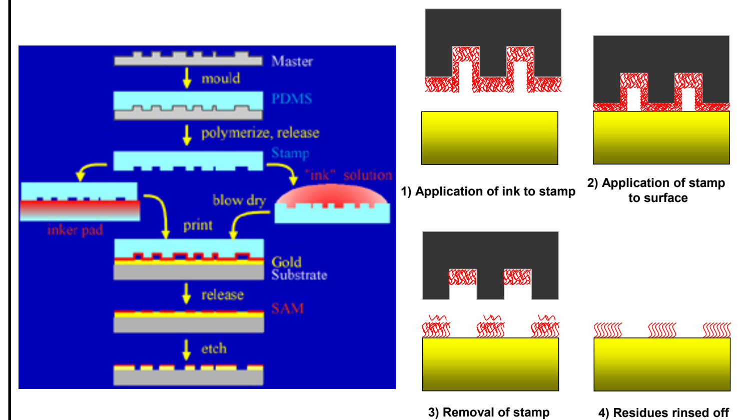


One in every home...

Alternate Nanolithography Techniques

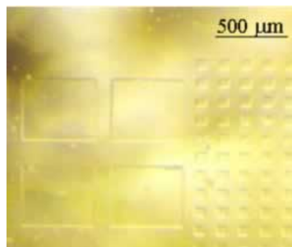
- **Micro-contact Printing**
- **Nanoimprint Lithography**
- **Scanned Probe Lithography**
- **Dip-pen Lithography**

Micro-Contact Printing



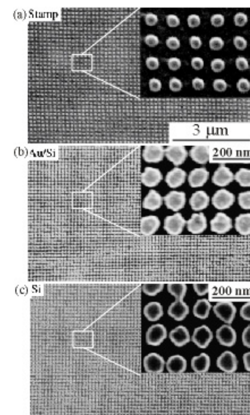
Source: IBM Zurich

Micro-Contact Printing (ctnd.)



Printing of PDMS

Source: Winograd Group, Penn State



High resolution μCP of 60 nm dots

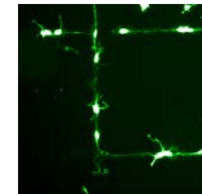
Source: IBM Zurich

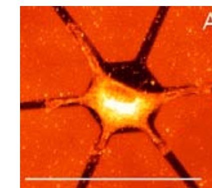
Selective Growth of Neurons on Printed Surfaces

Biological interactions that underlie neuron cell attachment and growth are being employed to produce defined networks of neurons.

Microcontact printing has been used to place chemical, biochemical, and/or topographical cues at designated locations.

Important potential for the interfacing of solid state electronics with nerve cell biology, and for the fundamental electrical studies of single nerve cells.





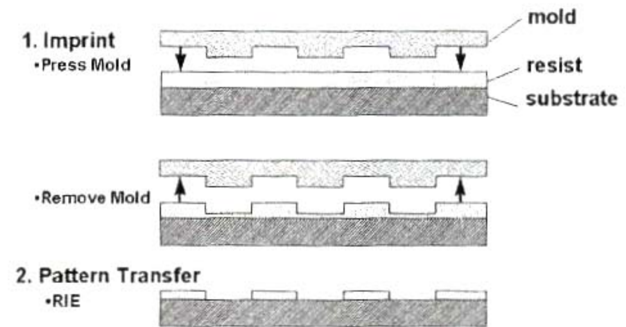
Selective growth of neurons on chemically patterned Si (C. D. James *et al.)*

Source: Craighead Group, Cornell

Alternate Nanolithography Techniques

- Micro-contact Printing
- **Nanoimprint Lithography**
- Scanned Probe Lithography
- Dip-pen Lithography

Nanoimprint Lithography

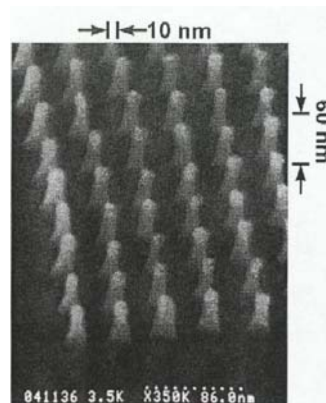


Consists of pressing a mold onto the resist above its glass transition temperature T_g

More ? Check out S. Y. Chou, Princeton

NIL Master

- **SiO_2 pillars with 10 nm diameter, 40 nm spacing, and 60 nm height fabricated by e-beam lithography.**
- **Master can be used tens of times without degradation**



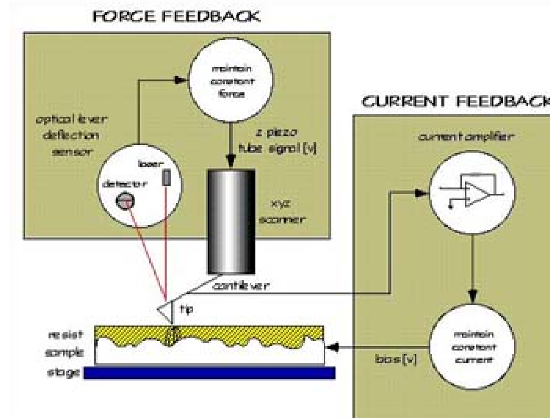
NIL Pattern in PMMA

- **Mask is pressed into 80 nm thick layer of PMMA on Si substrate at 175° C (T_g=105 ° C), P= 4.4 MPa.**
- **PMMA conforms to master patterng, resulting in ~10 nm range holes**

Alternate Nanolithography Techniques

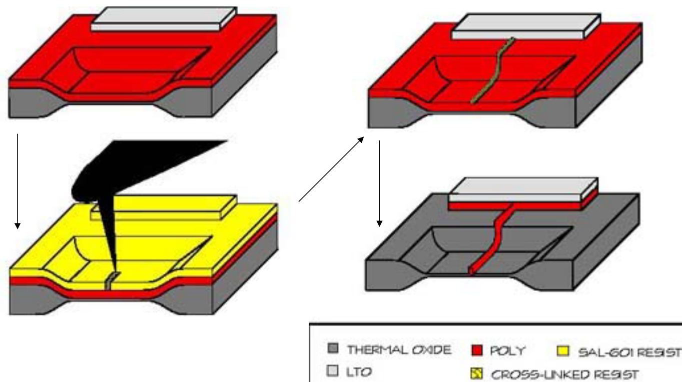
- Micro-contact Printing
- Nanoimprint Lithography
- **Scanned Probe Lithography**
- Dip-pen Lithography

Scanned Probe Lithography



Source: Quate Group, Stanford

Fabrication of CMOS Gate Using SPM Lithography



Source: Quate Group, Stanford

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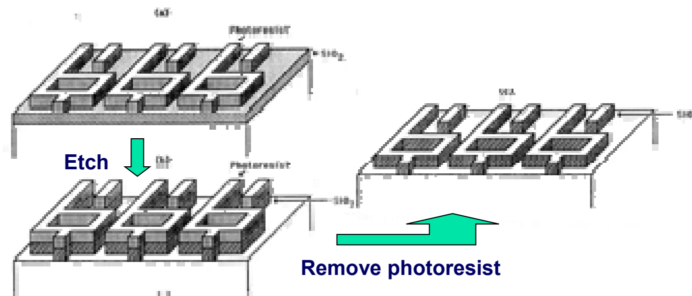
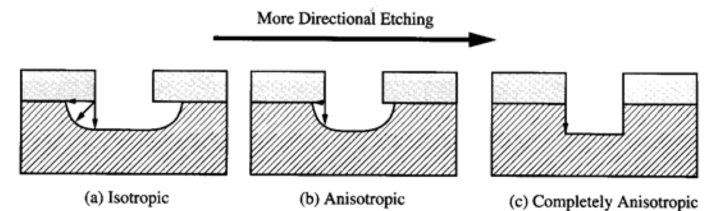
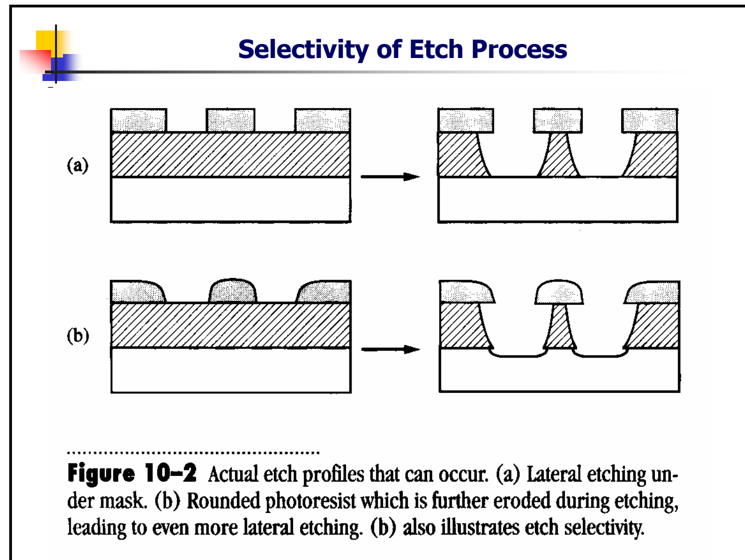
Need for Etching Processes

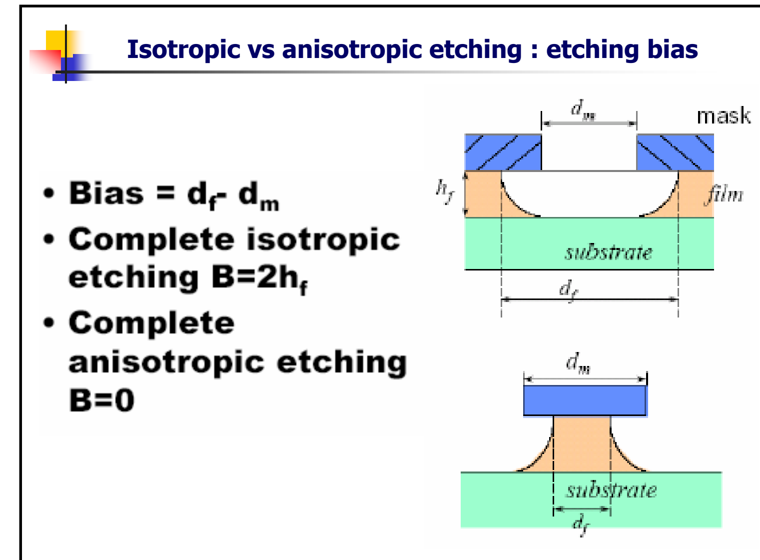
- **Selective removal of material as defined by photolithography**

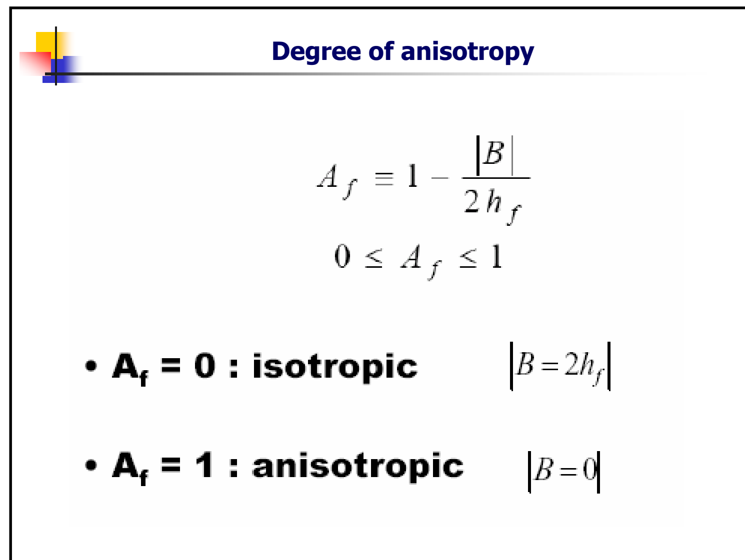


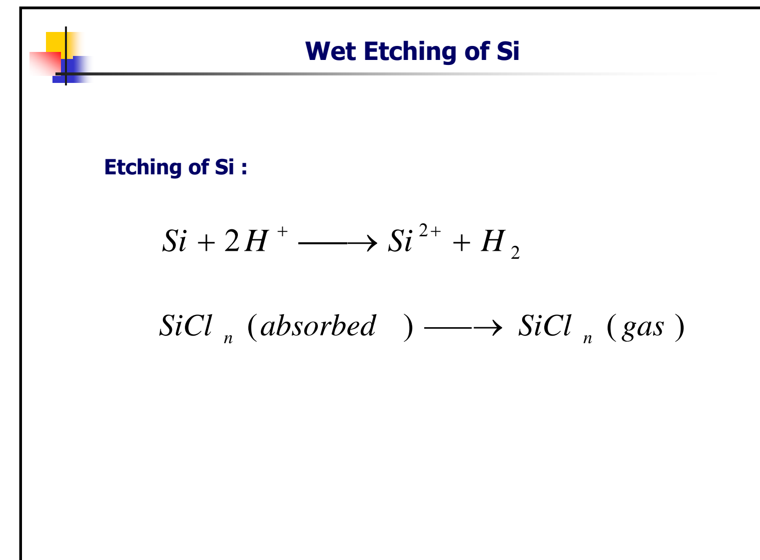
Isotropic vs. Anisotropic Etching

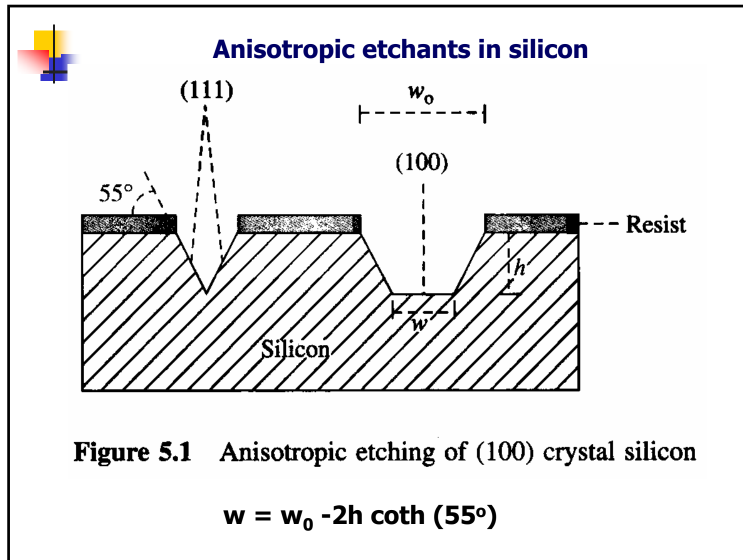



Selectivity of Etch Process
(a)
(b)
Figure 10–2 Actual etch profiles that can occur. (a) Lateral etching under mask. (b) Rounded photoresist which is further eroded during etching, leading to even more lateral etching. (b) also illustrates etch selectivity.


Isotropic vs anisotropic etching : etching bias
• Bias = d_f- d_m
• Complete isotropic etching $B=2h_f$
• Complete anisotropic etching B=0
d_m
mask
h_f
film
substrate
d_f
d_m
substrate
d_f


Degree of anisotropy
$A_f \equiv 1 - \frac{|B|}{2h_f}$
$0 \le A_f \le 1$
• A_f = 0 : isotropic $|B = 2h_f|$
• A_f = 1 : anisotropic $|B = 0|$

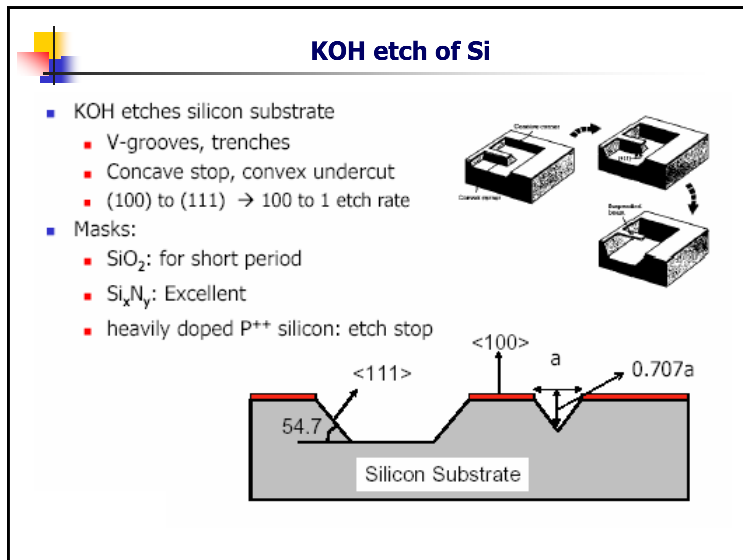

Wet Etching of Si
Etching of Si :
$Si + 2H^+ \longrightarrow Si^{2+} + H_2$
$SiCl_n\ (absorbed) \longrightarrow SiCl_n\ (gas)$

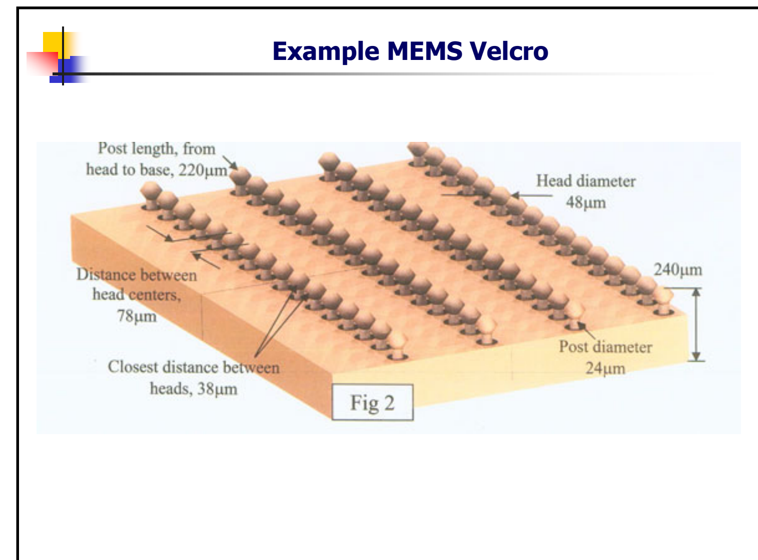


Anisotropic etchants in silicon (ctnd.)

Table 5.1 Anisotropic etching characteristics of different wet etchants for single-crystalline silicon

Etchant	Temperature (°C)	Etch-rate (μm/hour) of Si(100)	Si(110)	Si(111)
KOH:H_2O	80	84	126	0.21
KOH	75	25–42	39–66	0.5
EDP	110	51	57	1.25
$N_2H_4H_2O$	118	176	99	11
NH_4OH	75	24	8	1





Example : MEMS Velcro (ctnd.)

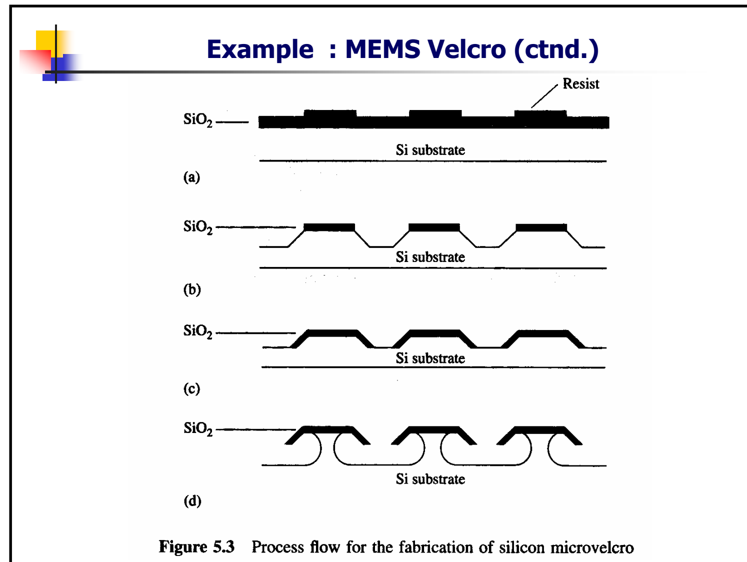


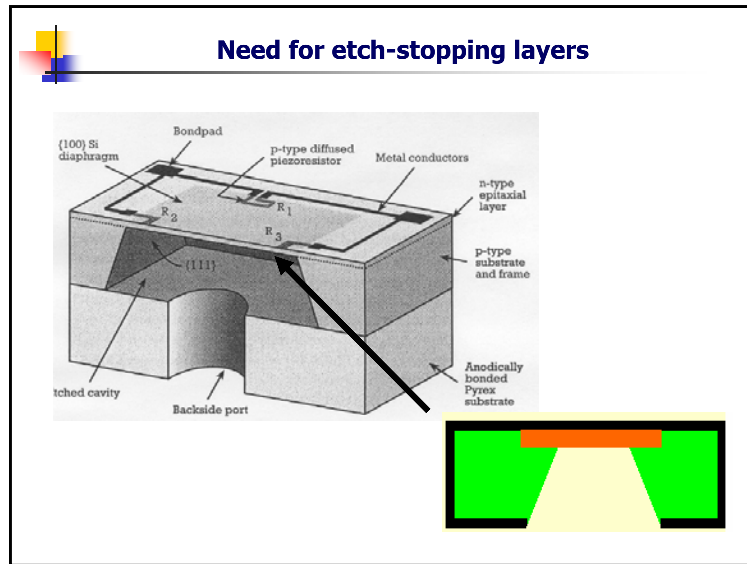
Figure 5.3 Process flow for the fabrication of silicon microvelcro

Wet Etching of Other Materials

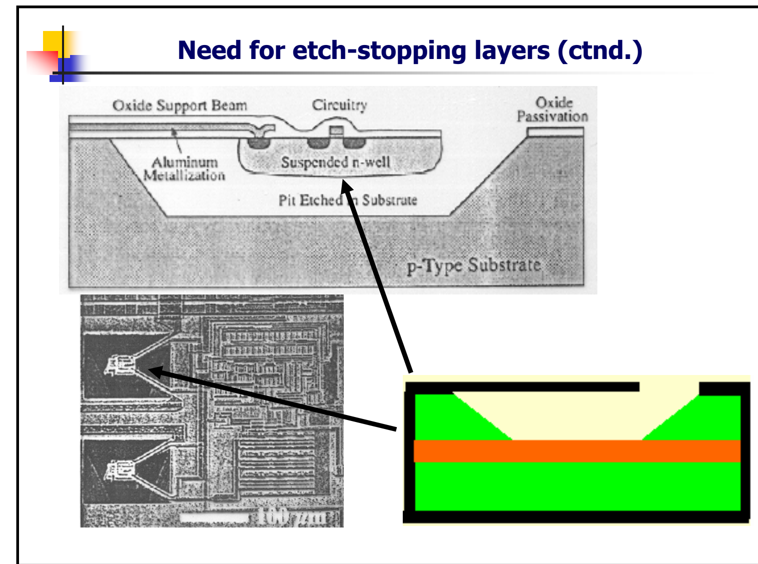
Table 10–1 Common wet chemical etchants for various thin films used in IC fabrication

Material	Etchant	Comments
SiO_2	HF (49% in water) "straight HF"	Selective over Si (i.e., will etch Si very slowly in comparison). Etch rate depends on film density, doping.
	NH_4F:HF (6:1) "Buffered HF" or "BOE"	About $^1/_{20}$ th the etch rate of straight HF. Etch rate depends on film density, doping. Will not lift up photoresist like straight HF.
Si_3N_4	HF (49%)	Etch rate depends strongly on film density, O, H in film.
	H_3PO_4:H_2O (boiling @ 130–150°C)	Selective over SiO_2. Requires oxide mask.
Al	H_3PO_4:H_2O:HNO_3:CH_3COOH (16:2:1:1)	Selective over Si, SiO_2, and photoresist.
Polysilicon	HNO_3:H_2O:HF (+ CH_3COOH) (50:20:1)	Etch rate depends on etchant composition.
Single crystal Si	HNO_3:H_2O:HF (+ CH_3COOH) (50:20:1)	Etch rate depends on etchant composition.
	KOH:H_2O:IPA (23 wt. % KOH, 13 wt. % IPA)	Crystallographically selective; relative etch rates: (100): 100 (111): 1
Ti	NH_4OH:H_2O_2:H_2O (1:1:5)	Selective over $TiSi_2$.
TiN	NH_4OH:H_2O_2:H_2O (1:1:5)	Selective over $TiSi_2$.
$TiSi_2$	NH_4F:HF (6:1)	
Photoresist	H_2SO_4:H_2O_2 (125°C)	For wafers without metal.
	Organic strippers	For wafers with metal.

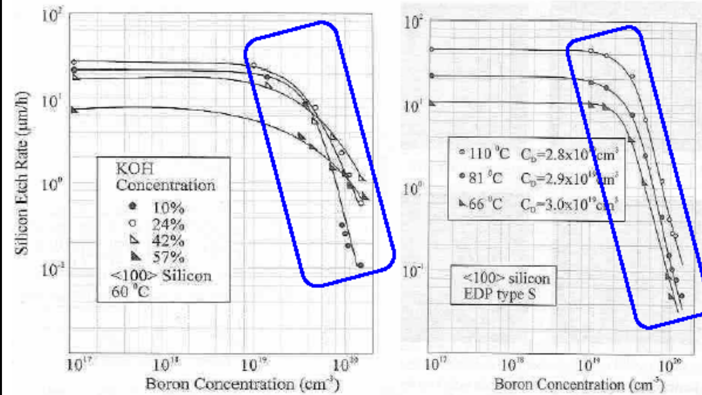
Need for etch-stopping layers



Need for etch-stopping layers (ctnd.)



Doping-selective etching



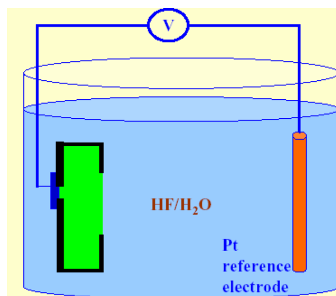
Doping-selective etching (ctnd.)

Table 5.2 Dopant-dependent etch rates of selected silicon wet etchants

Etchant (Diluent)	Temperature (°C)	(100) Etch rate (μm/min) for boron doping $\ll 10^{19}$ cm^{-3}	Etch rate (μm/min) for boron-doping $\sim 10^{20}$cm^{-3}
EDP (H_2O)	115	0.75	0.015
KOH (H_2O)	85	1.4	0.07
NaOH (H_2O)	65	0.25–1.0	0.025–0.1

- **Disadvantage: requires high-dopant concentration to achieve good selectivity**

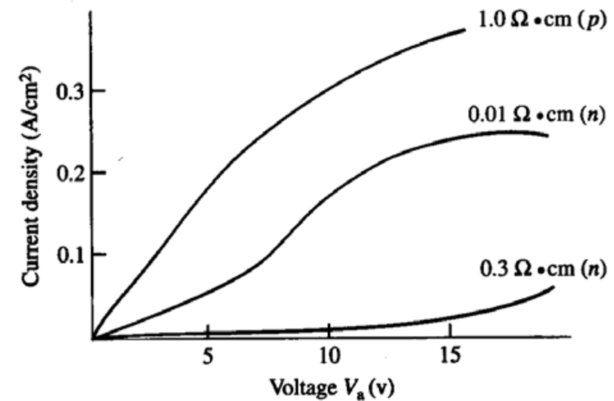
Electrochemical etching



Steps

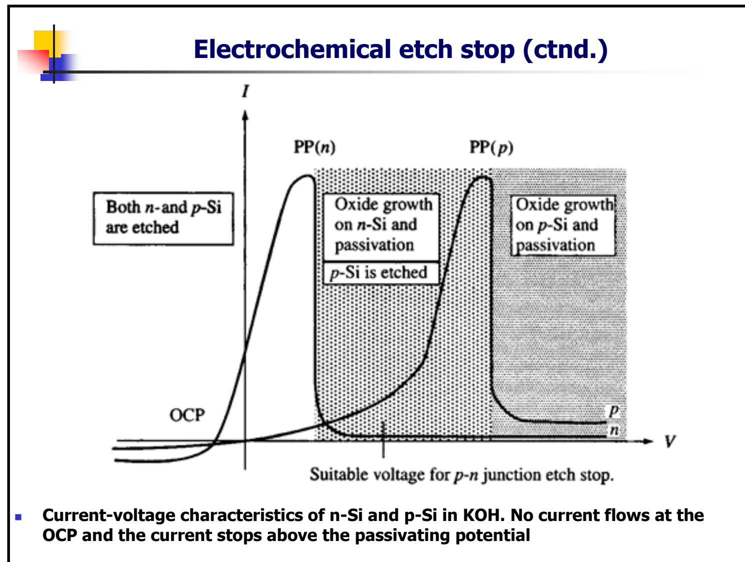
1. **Injection of holes into the semiconductor to raise it to a higher oxidation state Si^{+}**
2. **Attachment of negatively charged hydroxyl groups, OH^{-}, to the positively charged Si**
3. **Reaction of the hydrated silicon with the complexing agent in the solution**
4. **Dissolution of the reaction products into the etchant solution**

Electrochemical etching ctnd.)



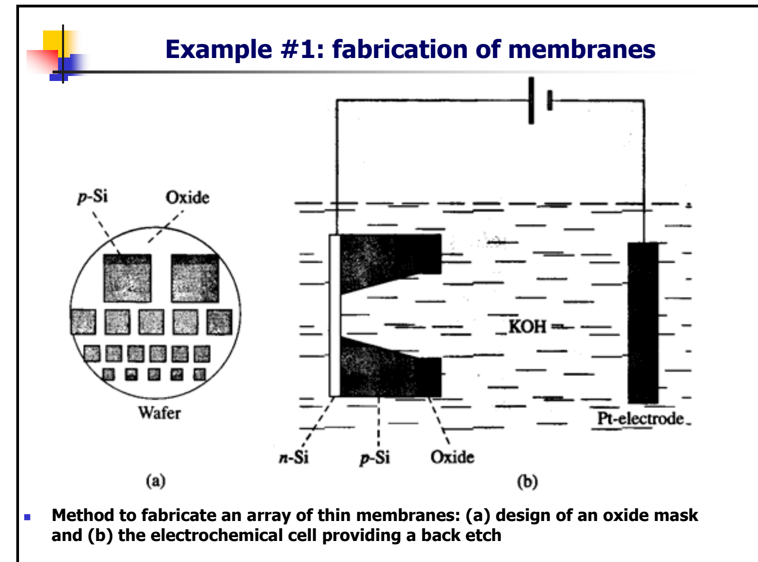
- **Plot of electrochemical current density against voltage for silicon doped to different resistivities**

Electrochemical etch stop (ctnd.)



- **Current-voltage characteristics of n-Si and p-Si in KOH. No current flows at the OCP and the current stops above the passivating potential**

Example #1: fabrication of membranes



- **Method to fabricate an array of thin membranes: (a) design of an oxide mask and (b) the electrochemical cell providing a back etch**

Example #2 : fabrication of cantilevers

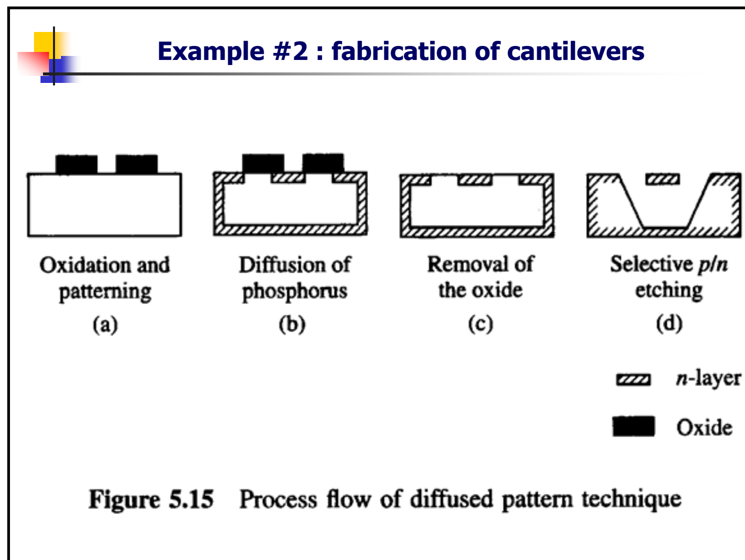


Figure 5.15 Process flow of diffused pattern technique

Example #2 : fabrication of cantilevers (ctnd.)

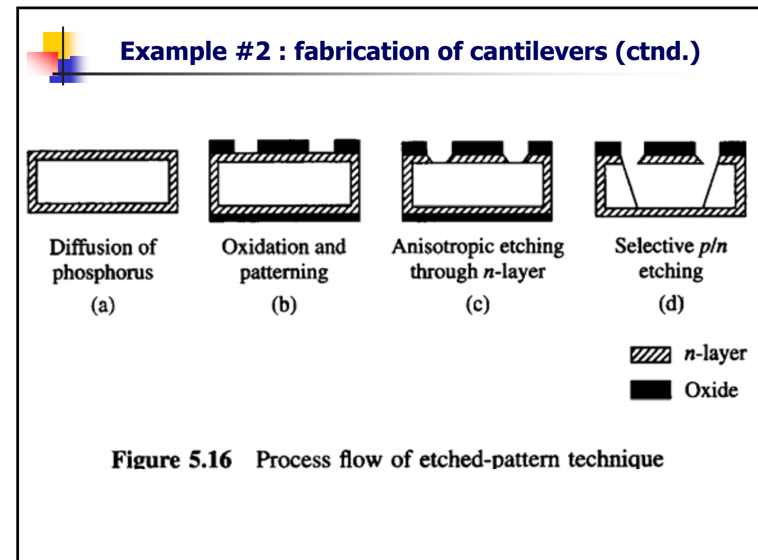


Figure 5.16 Process flow of etched-pattern technique

3. Overview of Microfabrication...TOC

- **Pattern Transfer**
  - Optical Lithography
  - Design Rules
  - Mask Making
  - Wet Etching
  - **Dry-Etching**
  - Lift-Off
  - Planarization

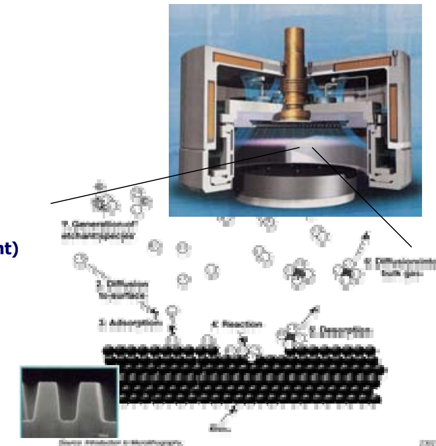
Dry Etching Methods

Dry etching required for small feature size:

- Anisotropic
- High aspect ratios

Types:

- Reactive Ion etching (right)
- Sputtering
- Ion beam milling



Check out: Plummer, Deal Griffin, Silicon VLSI Technology, Chap 10

Plasma Etching

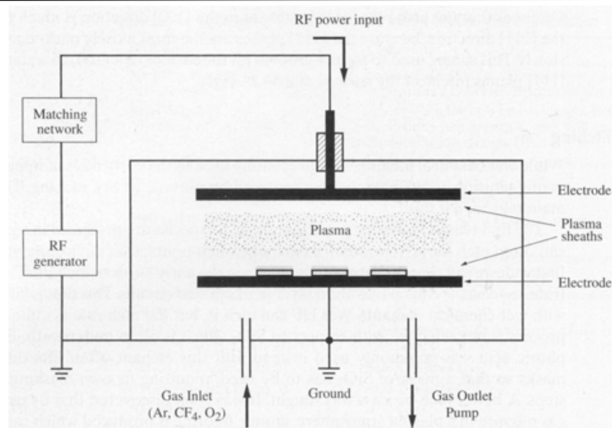
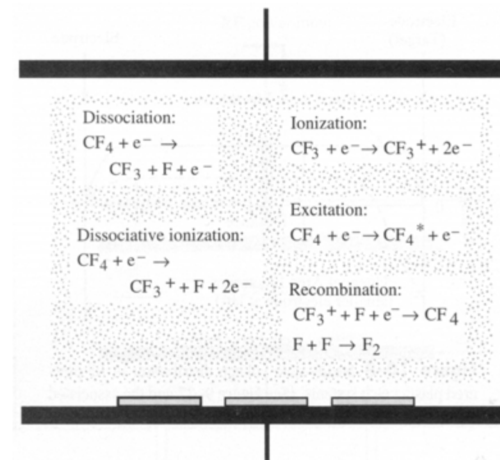
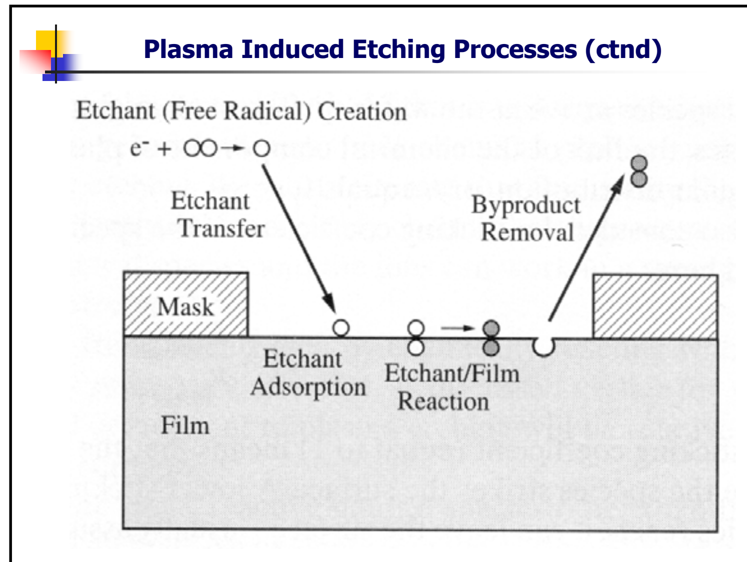


Figure 10-7 Schematic diagram of an RF-powered plasma etch system.

Plasma Induced Etching Processes

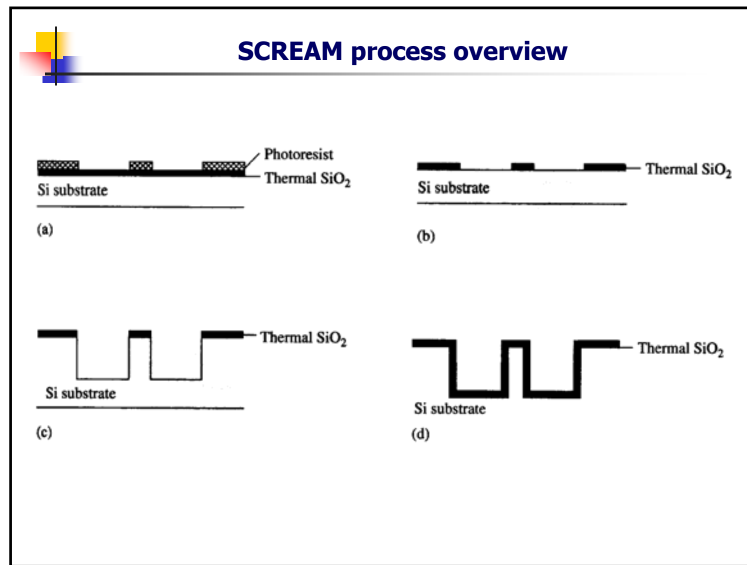


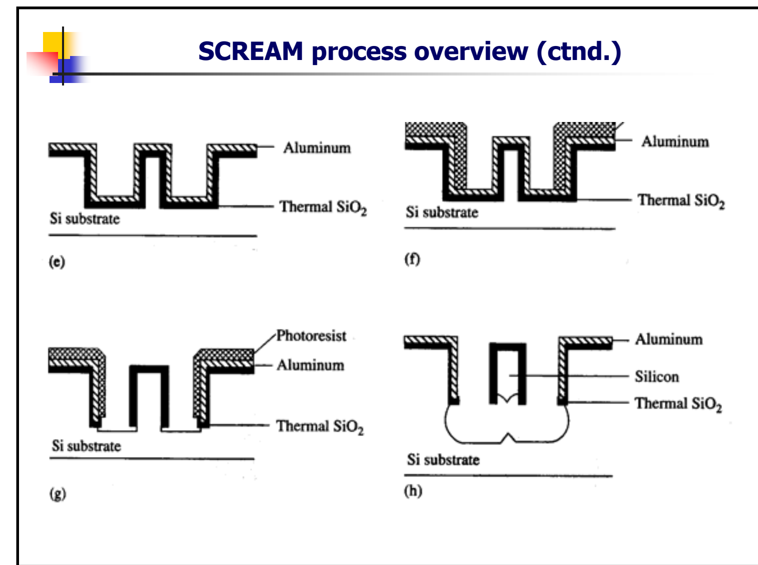


Etched Structures

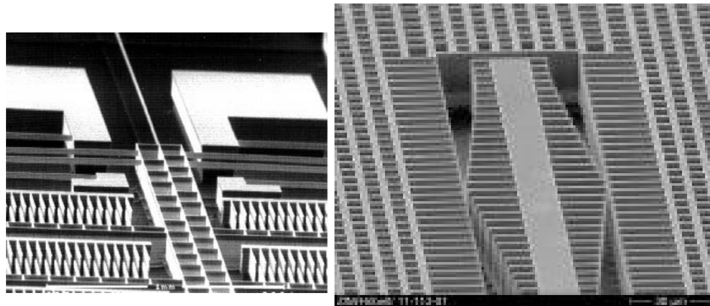
SiO2
SiC
Si-O-C
SiC
100 nm
3.0 um

- **Advantages:**
  - **good directional etching**
  - **good selectivity : SiO_2 to Si (35:1)**





Example of structures produced by SCREAM



3. Overview of Microfabrication…TOC

- **Pattern Transfer**
  - Optical Lithography
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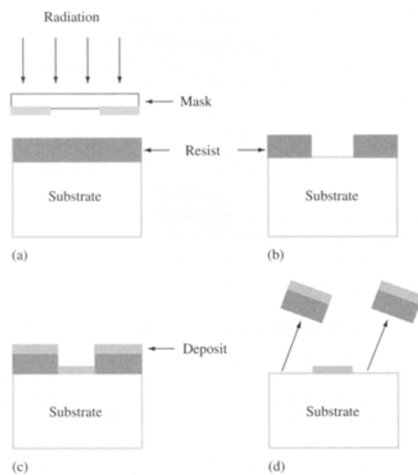
  - Mask Making
  - Wet Etching
  - Dry-Etching
  - **Lift-Off**
  - Planarization

Transfer by lift-off process



3. Overview of Microfabrication…TOC

- **Pattern Transfer**
  - Optical Lithography
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  - Dry-Etching
  - Lift-Off
  - **Planarization (read)**