A Comparative Simulation Study of Four Multilevel DRAMs

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Outline

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- Motivation
- MLDRAM storage and basic circuit techniques
- Brief Descriptions of MLDRAM designs
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    - Gillingham's (MOSAID, 1996)
    - Okuda's (NEC, 1997)
    - A proposed MLDRAM (1999)
- Simulation Setup
- Results
- Discussion
- Conclusions
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Introduction to Multilevel DRAM

The Basic Idea

- Store *n* bits in one DRAM cell by using $N=2^n$ voltage levels
- Sensing is analogous to *N*-level A/D conversion

The main advantage of MLDRAM

- Density potentially increased by a factor of 2^{n-1} without any change in the process and the optimized cell array
    - E.g. A factor of 2 for 4-level MLDRAM

The main disadvantage of MLDRAM

- Noise margins reduced by a factor of *N*-1 compared to conventional DRAM
    - E.g. A factor of 3 reduction for 4-level MLDRAM

Scenarios for Using MLDRAM

- Can increase storage density of embedded DRAM
  - 1.5 to 1.7 times the original number of bits
  - shrink DRAM area by 30 to 40 percent
- Use relaxed line widths for the same die size
  - 25 to 30 percent thicker line width
  - e.g. use 0.21 μm instead of 0.17 μm
- Maintain the pace of DRAM density increases
  - Avoid the need for 128 Mb or 512 Mb generations

Motivation and Goal

Motivation

- We want to find a manufacturable MLDRAM design
- Several MLDRAM schemes have been proposed, but it is difficult to compare the schemes because
    - Each was presented assuming a different process
    - Each had different array parameters
- A fair comparison would
    - Help identify strengths and weaknesses of each

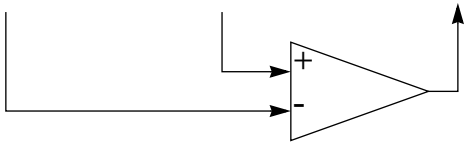
Goal

To “fairly” compare MLDRAM schemes in terms of access time, cycle time, and cycle energy, and to evaluate area overhead, robustness and complexity

MLDRAM Storage

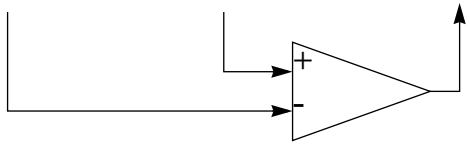
Conventional

Reference Voltage	Cell Voltage	Binary
	V_{DD}	1
$\frac{1}{2}V_{DD}$		
	V_{SS}	0



Multilevel

Reference Voltage	Cell Voltage	Binary
	V_{DD}	11
$\frac{5}{6}V_{DD}$		
	$\frac{2}{3}V_{DD}$	10
$\frac{1}{2}V_{DD}$		
	$\frac{1}{3}V_{DD}$	01
$\frac{1}{6}V_{DD}$		
	V_{SS}	00



Basic MLDRAM Techniques

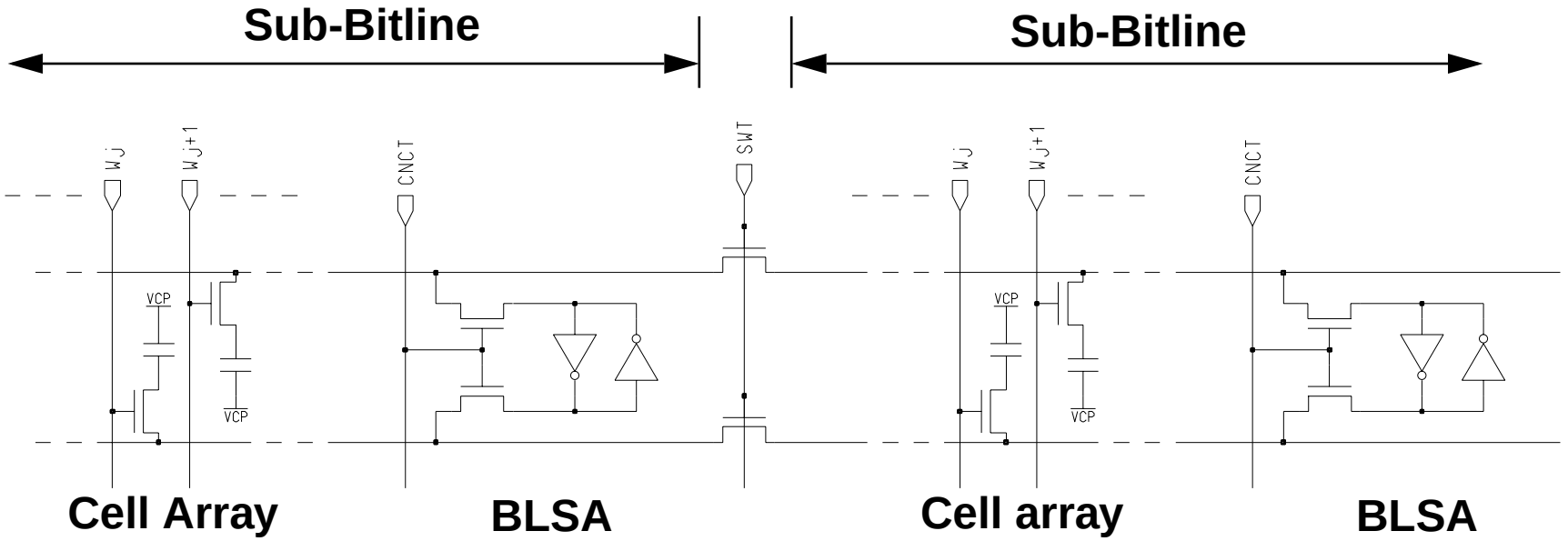
What types of circuits can be used?

- Want to re-use proven pitch-matched circuitry

  ➔ *Use bitline sense amplifiers (BLSA)*

- Need to have multiple “copies” of the cell signal, one for each sense amplifier comparison

  ➔ *Divide up the bitline into sub-bitlines*



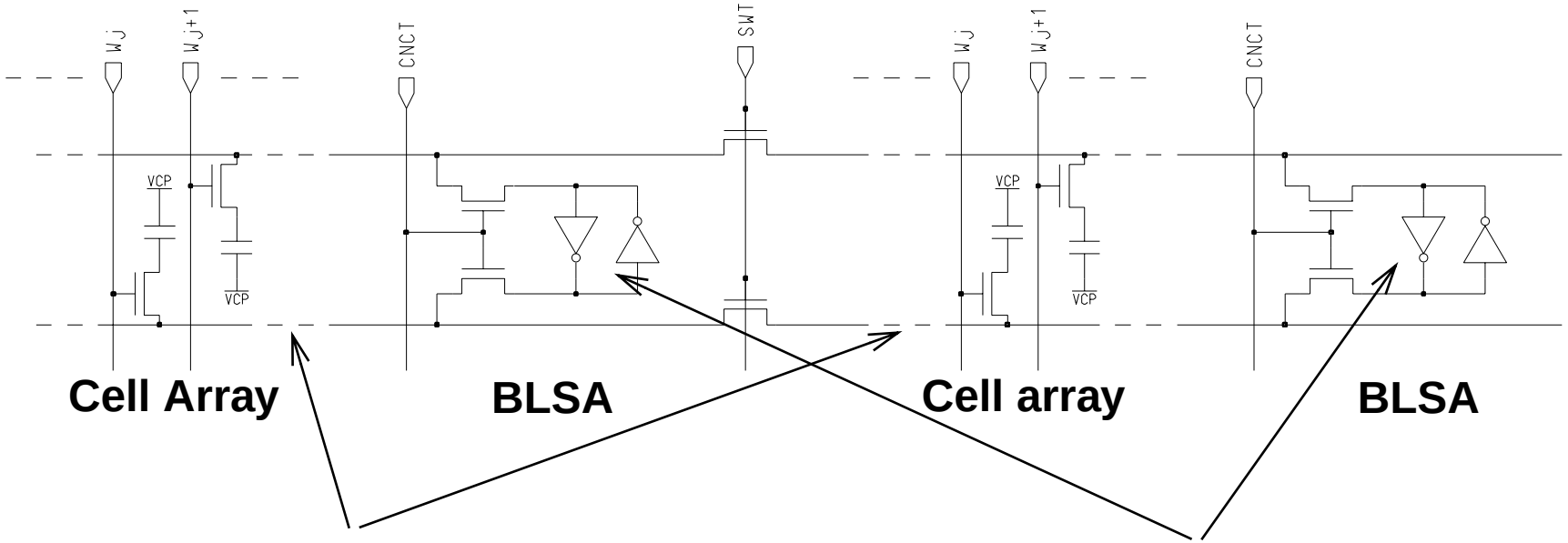
Basic MLDRAM Techniques (continued)

How is sensing performed?

1. Activate a wordline

2. Share cell charge with all sub-bitlines

3. Connect the sense amplifiers



4. Somehow, the reference voltages are in place

?

5. Activate the sense amplifiers

Basic MLDRAM Techniques (continued)

What about the reference voltages?

- Two approaches:
    1. Globally generate and distribute reference voltages
    2. Locally generate reference voltages using capacitor charge-sharing techniques or coupling capacitors

How are the four voltages restored to the cell?

- Charge two sub-bitline capacitances to the voltage of the first bit, charge another to the voltage of the second bit and short the three together.

MLDRAM Taxonomy

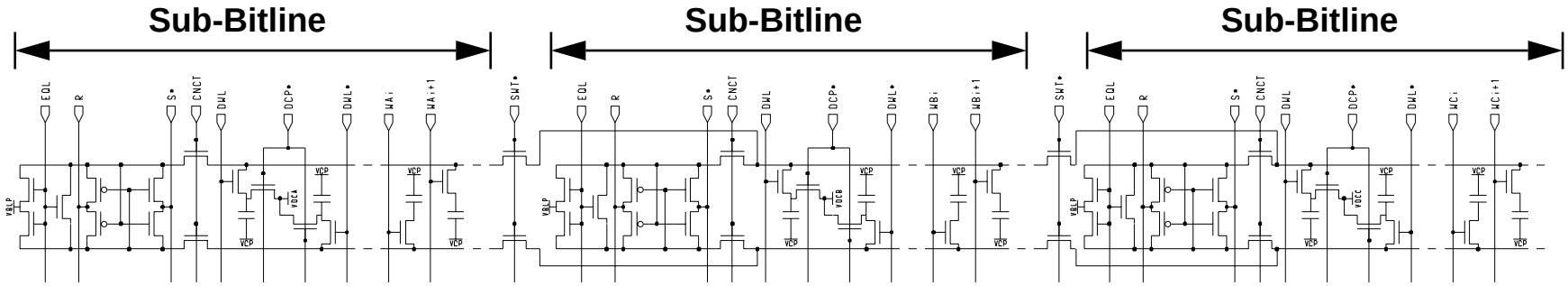
Circuits can be classified by

1. Reference voltage generation
    - Global generation and distribution or local generation
2. Sensing method
    - Analogies to A/D conversion can describe the approach taken

Reference Method	***Sensing Method Analogies***	
	Flash Conversion	**Successive Approximation**
Globally Distributed	Furuyama	
Locally Generated	Birk	Gillingham, Okuda

MLDRAM Designs

Furuyama et al. (Toshiba Corp., 1989)



- Bitline is split into three identical sub-bitlines
- Reference cells in each sub-bitline supply three references
- Global voltage lines provide reference cell signals

Data in the sense amplifiers is represented by a "thermometer code"

Sense amplifier results	000	001	011	111
Binary Data	00	01	10	11

MLDRAM Designs (continued)

Gillingham (MOSAID Technologies Inc., 1996)

- Uses two identical sub-bitlines
- The first bit sensed and then used to create the reference voltage for the second bit

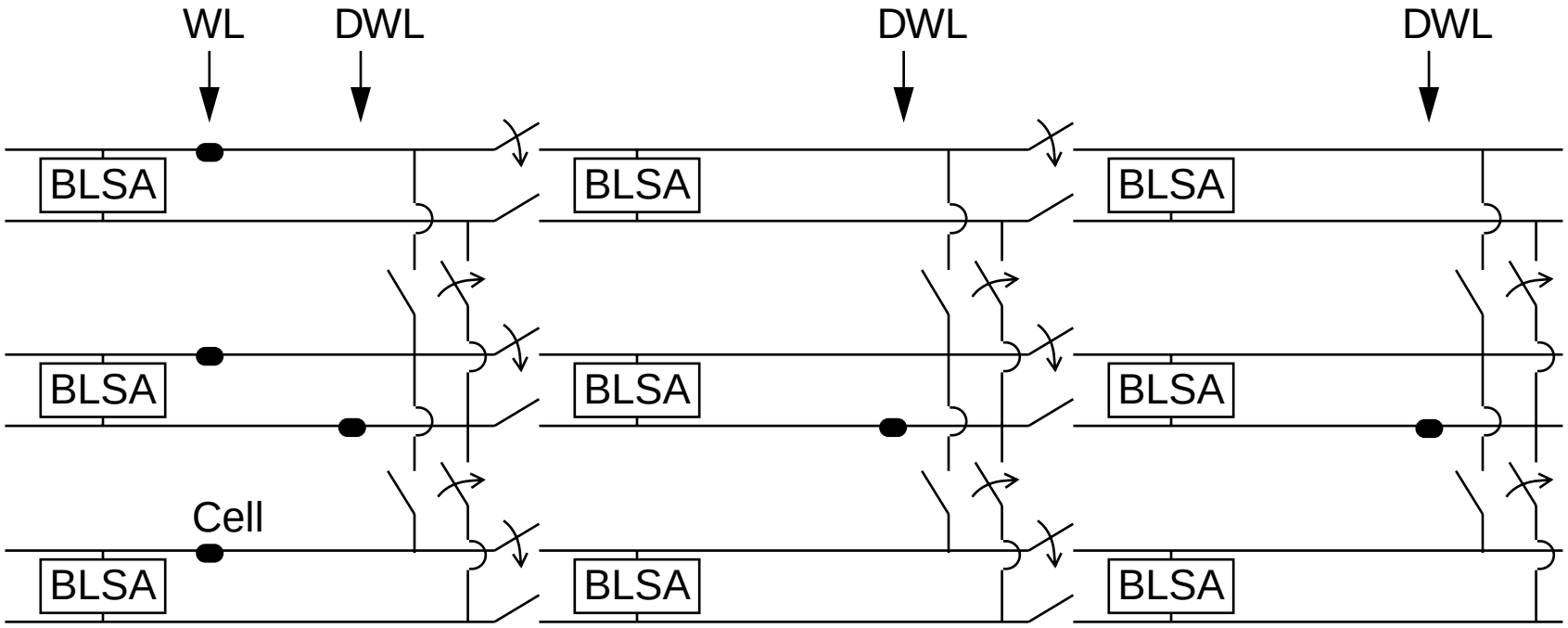
Okuda et al. (NEC Corp., 1997)

- Uses two uneven sub-bitlines, one having twice the parasitic capacitance as the other
- When the larger sub-bitline is sensed, the smaller sub-bitline is bumped to the correct reference value via the coupling capacitors

MLDRAM Designs (continued)

Birk et al. (University of Alberta, 1999)

- Combines the speed of Furuyama's design and the robustness of Gillingham's design
- Uses three identical sub-bitlines



Simulation Setup

- Device models are based on a 250 nm process
- Bitlines must have at least 256 wordlines
- Capacitances and wire models are the same throughout
- Common sense amplifiers
- Common timing parameters used
- Uniform criteria were used for timing optimization
- Uniform power supply models
- A conventional DRAM control case was simulated

Results

Attribute	DRAM	Furuyama	Gillingham	Okuda	Birk
SA activation, 1st bit (ns)	8.00	14.06	18.33	15.27	14.25
BL, 0.5V split, 1st bit (ns)	9.08	16.73	20.16	17.00	17.03
SA activation, 2nd bit (ns)	N/A	14.06	70.25	34.04	14.25
BL, 0.5V Split, 2nd bit (ns)	N/A	16.73	72.50	35.40	17.03
Cycle time (ns)	37.87	57.75	152.48	82.09	77.74
Energy per bit (fJ/bit)	809	1101	1490	767	1605

MLDRAM Compared to DRAM:

- Access is generally slower
- Cycle time is longer
- Energy per bit is usually greater

Discussion

Attribute	DRAM	Furuyama	Gllingham	Okuda	Birk
Access time	1	2	5	4	3
Cycle time	1	2	5	4	3
Cycle energy per bit	2	3	4	1	5
Overall robustness	1	4	3	5	2
Area per bit	5	3	2	1	4
Control logic simplicity	1	3	5	2	4

- Furuyama's: Fast, but not robust
- Gillingham's: Low area and robust, but slow and complex
- Okuda's: Low energy and area, but not robust
- Birk's: Fast and robust, but high area and greatest energy per bit

Conclusions

- Performed a fair comparison of MLDRAM schemes
- Clarified their real advantages and disadvantages
- We proposed a new MLDRAM scheme
    - About as fast as Furuyama's
    - More robust than previous schemes
    - Offers significant density improvement over DRAM
- MLDRAM is a promising and practical technology but important challenges remain
    - Reduced noise margins (retention time)

Future Work

- Robustness: Can it be quantified?
- Area overhead: A layout analysis to quantify area overhead
- Complexity: What burden does complexity place on the chip periphery in terms of area and power?
- Does the proposed scheme work?
    - A test chip is being designed
    - A fault model is needed
    - Once made, the chip must be tested

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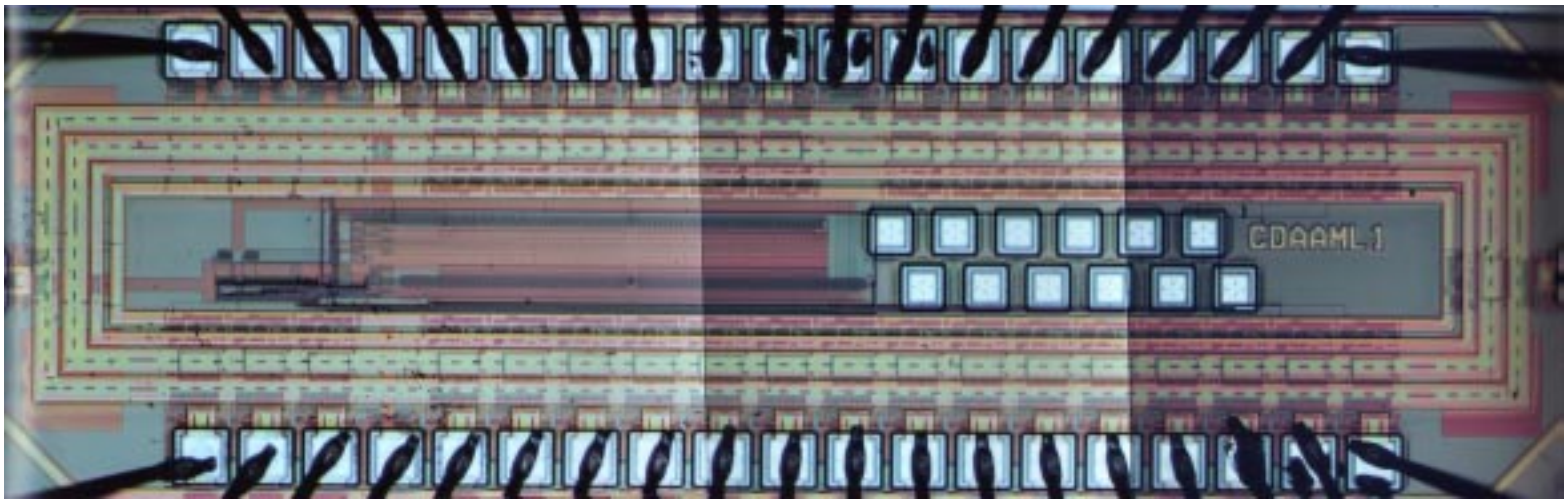
Ongoing Research at U of A

Gillingham's Design in Silicon



- Preliminary results show proper MLDRAM functionality
- Detailed characterization is underway