Clocks on General Purpose I/O Pins

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This document discusses inputting clock signals on general purpose input pins. It is directed at students using the Xilinx Spartan FPGA.

The Xilinx Spartan FPGA has dedicated clock pins for inputting global clock signals. These clock pins are connected to global clock buffers (BUFGP) which distribute the clock signal throughout the chip. These global clock buffers are optimized for high fan-out and low skew.

A problem arises when you need to deliver a signal that is used heavily throughout your design and you only have access to one of the general purpose input pins (i.e. generating a reset signal with a pushbutton). Such is the case when you are using a student prototype board. The ISE tools will give an error indicating that the signal should be allocated to a global clock buffer. However, a general purpose pin cannot be connected to a global clock buffer.

The solution to the problem is as follows. You need to manually instantiate an input buffer (IBUF) and connect it to a global buffer (BUFG). The global buffer is similar to the global clock buffer (BUFGP) in that it distributes signals throughout the design, optimized for high fanout and low skew.

For example, to instantiate the components:

Include the following library

```
library unisim;
use unisim.vcomponents;
```

Include the following component declarations in the architecture before the begin statement.

```
architecture

  component IBUF
    port (
      I : in  std_logic;
```

```
      O : out std_logic);
  end component;

  component BUFG
    port (
      I : in  std_logic;
      O : out std_logic);
  end component;
```

Instantiate the components in the architecture body.

```
begin

  ...

  iobuf: IBUF
    port map (
      I => rst_in,
      O => rst_mid);

  clkbuf: BUFG
    port map (
      I => rst_mid,
      O => rst_global);

  ...

end architecture;
```

Note that *rst_in* is the input signal and *rst_global* is the signal distributed by the global buffer. The ISE tools should now stop complaining at you.