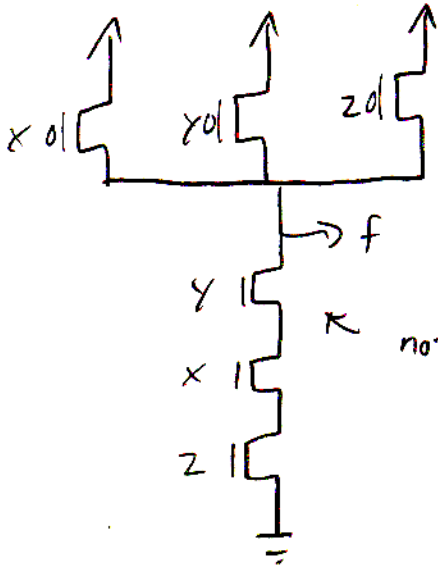
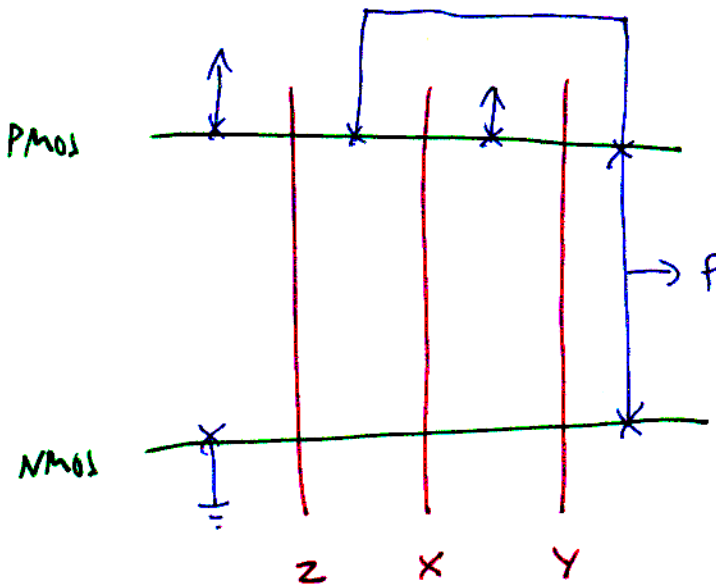


1a

$$f = \overline{xyz}$$



note y here for min delay



or

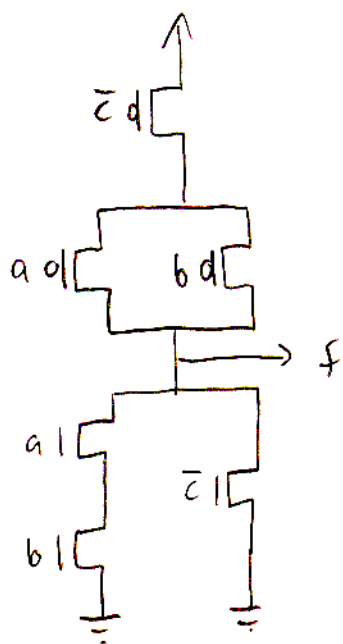
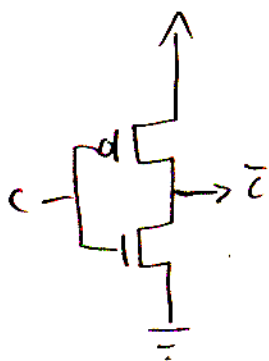
x z

16

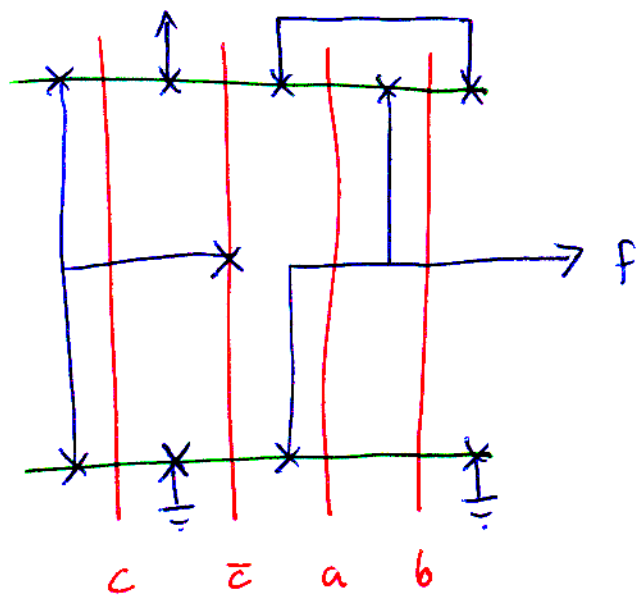
$$f = \overline{(a \cdot b)} \cdot c$$

$$= \overline{\overline{(a \cdot b)} + \bar{c}}$$

$$= \overline{a \cdot b + \bar{c}}$$



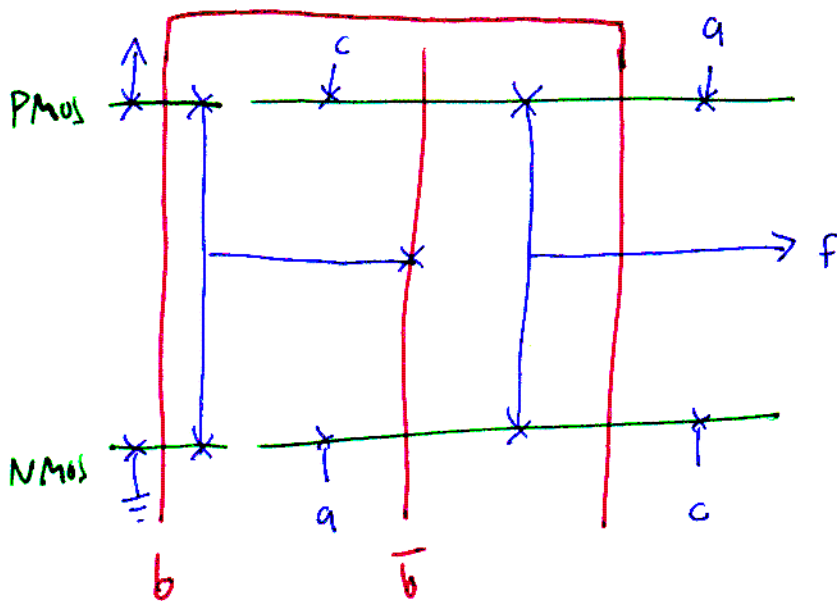
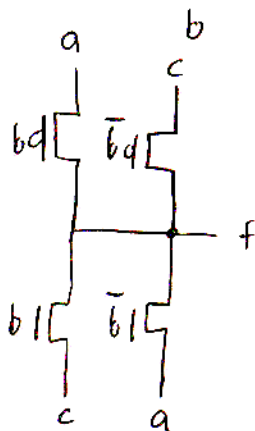
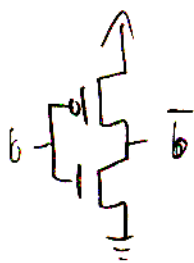
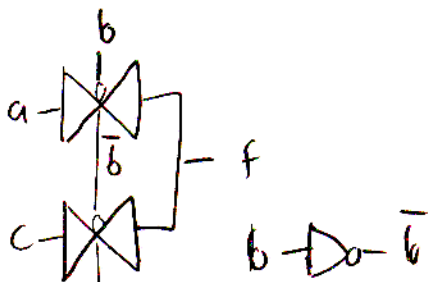
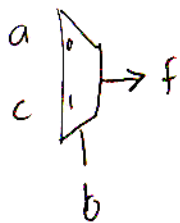
PMOS



NMOS

1c

$$f = a \cdot b + c \cdot \bar{b}$$



Question 2

4 input NAND

complimentary logic CMOS (static)	8 T
pseudo NMOS	5 T
dynamic logic	6 T

Consume significant static power:
pseudo NMOS

Question 3

Cascaded Inverter Question

First $\frac{W_p = 1.2 \mu m}{W_n = 1 \mu m} \approx \frac{W_p = 484 \mu m}{W_n = 403 \mu m}$

The inverters maintain the same ratio
 \therefore only one scaling factor needs to be calculated.

Equation $S^{(j-1)} = \frac{C_j}{C_1}$

Assume ratio of widths (gate capacitance)

$$S^{(j-1)} = \frac{W_n = 403 \mu m}{W_n = 1 \mu m}$$

where,

S = scaling factor

j = number of stages

$$\ln(S^{(j-1)}) = \ln\left(\frac{403 \mu m}{1 \mu m}\right)$$

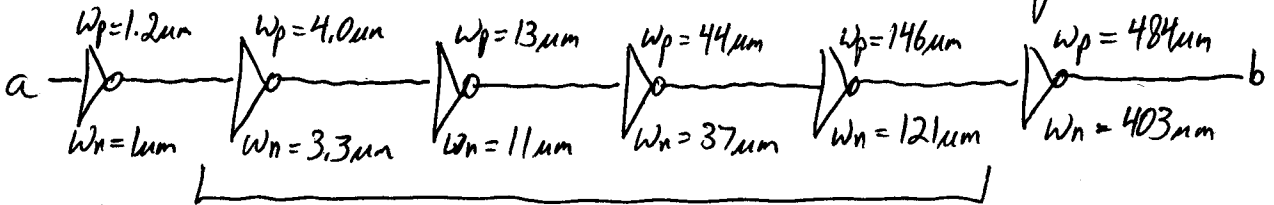
$$(j-1) \ln(S) = \ln(403)$$

To maintain functionality we require an even number of inverters

Try, $j=4 \Rightarrow S = 7.39$ (4 stages, including first + last)

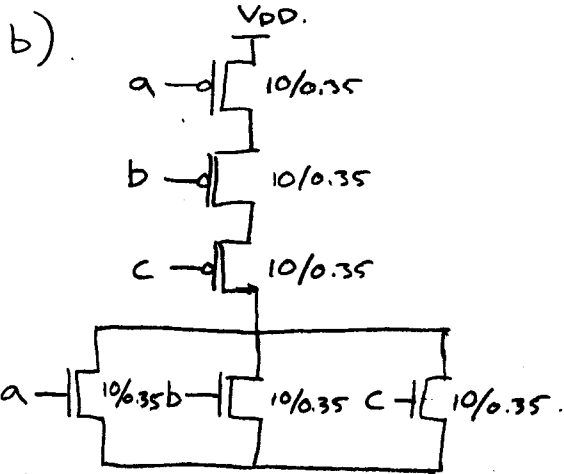
$j=6 \Rightarrow S = 3.32$ (6 stages, including first + last)

OR $j=8 \Rightarrow S = 2.36$ (8 stages, including first + last)



Theoretically, to minimize propagation delay, we should choose the number of stages such that the scaling factor is closest to e . Practically, a scaling factor $> e$ results in the minimum propagation delay. The propagation delay is reduced by sharing the capacitive load (i.e. distributing the capacitive load) such that the ratio of capacitance to drive is reduced while constraining the number of gate delays introduced into the circuit.

- 4a.
- increased capacitance due to extra contacts.
 - extra area taken up in layout.
 - asymmetric operation $\left\{ \begin{array}{l} \text{faster fall time} \\ \text{slower rise time.} \end{array} \right.$
 - extra resistance



$$C_{\text{drain}} = \frac{1}{2} C_G + C_j A_D + C_{jsw} P_D$$

$$A_D = W(L_{s,D} + X_D)$$

$$P_D = 2(W + L_{s,D} + X_D)$$

$$C_G = C_{ox} W L_{\text{drawn}}$$

$$C_{\text{drainP}} = \frac{1}{2} C_{ox} W_p L_{\text{drawn}}$$

$$+ C_{jp} W_p (L_{s,p} + X_{Dp})$$

$$+ C_{jswp} \cdot 2(W_p + L_{s,p} + X_{Dp})$$

$$C_{\text{drainN}} = \frac{1}{2} (6.7 \times 10^{-3} \text{ pF}/\mu\text{m}^2) (10 \mu\text{m}) (0.35 \mu\text{m}) \quad C_{\text{drainP}} = \frac{1}{2} (6.7 \times 10^{-3} \text{ pF}/\mu\text{m}^2) (10 \mu\text{m}) (0.35 \mu\text{m})$$

$$+ 1.3 \times 10^{-3} \text{ F}/\text{m}^2 (10 \mu\text{m} \cdot (0.85 \mu\text{m} + 0.055 \mu\text{m})) \quad + 1.51 \times 10^{-3} \text{ F}/\text{m}^2 (10 \mu\text{m} \cdot (0.85 \mu\text{m} + 0.015 \mu\text{m}))$$

$$+ 3.8 \times 10^{-10} \text{ F}/\text{m} \cdot 2 \cdot (10 \mu\text{m} + 0.85 \mu\text{m} + 0.055 \mu\text{m}) \quad + 4.6 \times 10^{-10} \text{ F}/\text{m} \cdot 2 \cdot (10 \mu\text{m} + 0.85 \mu\text{m} + 0.015 \mu\text{m})$$

$$w/x_0 = 11.73 \text{ fF} + 11.05 \text{ fF} + 8.25 \text{ fF} \quad w/o x_0 = 11.73 \text{ fF} + 12.84 \text{ fF} + 9.98 \text{ fF}$$

$$w/x_0 = 11.73 \text{ fF} + 11.77 \text{ fF} + 8.29 \text{ fF} \quad w/x_0 = 11.73 \text{ fF} + 13.1 \text{ fF} + 10 \text{ fF}$$

$$C_{DN} = 31.79 \text{ fF}$$

$$C_{DP} = 34.83 \text{ fF}$$

$$w/o x_0 = 31.03 \text{ fF}$$

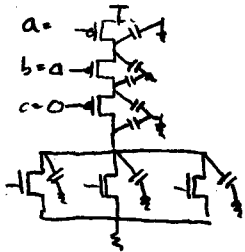
$$w/o x_0 = 34.55 \text{ fF}$$

Most Capacitance

Least Capacitance.

initial $c=0, b=0, a=d$, final $c=0, b=0, a=0$

initial $c=1, b=0, a=0$, final $c=0, b=0, a=0$

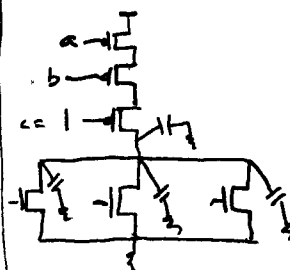


$$C_{\text{most}} = C_{\text{DN}} + C_{\text{DPN}} + 2C_{\text{Dp}} + 2C_{\text{DpP}} + C_{\text{DAP}}$$

$$= 3C_{\text{DN}} + 5C_{\text{DP}}$$

$$C_{\text{most}} = 269.52 \text{ fF}$$

$$\text{or } 265.84 \text{ fF}$$



$$C_{\text{least}} = C_{\text{DN}} + C_{\text{DPN}} + C_{\text{CN}} + C_{\text{CP}}$$

$$= 3C_{\text{DN}} + C_{\text{DP}}$$

$$C_{\text{least}} = 130.2 \text{ fF}$$

$$\text{or } 127.64 \text{ fF}$$

When NMOS/PMOS is on capacitance from other nodes is brought to the output.

when NMOS/PMOS is off no extra capacitance is brought to the output.

Question 5

$$V_{DD} = 3.3V$$

$$V_{SGP} = 3.3 - 2 = 1.3V$$

$$V_{TP} = -0.8V$$

$$V_{SDP} = 3.3 - 1.65 = 1.65V$$

Current through the resistor

$$I_r = \frac{V_{out}}{R} = \frac{1.65V}{200\Omega} = 8.25 \times 10^{-3} A$$

Check to see if the pMOS is in saturation

$$\begin{aligned} \text{saturation} \quad V_{SDP} &\geq V_{SGP} - |V_{TP}| \\ 1.65 &\geq 1.3 - 0.8 \\ 1.65 &\geq 0.5 \quad \checkmark \end{aligned}$$

$$L = L_{drawn} - \Delta L$$

$$= 0.35 \mu m - 2 \times 0.015 \mu m$$

$$= 0.32 \mu m$$

Equate the currents and solve for W

$$I_r = I_{dp}$$

$$I_r = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L} \right) (V_{SGP} - |V_{TP}|)^2$$

$$8.25 \times 10^{-3} A = \frac{(1.7 \times 10^{10} \mu m^2/V/s) (6.7 \times 10^{-15} F/\mu m^2) W}{(2)(0.32 \times 10^{-6} m)} (1.3 - 0.8)^2$$

$$W = 185 \mu m$$