FPGA Pin #	16	17	18	20	21	22	23	24	27	29	30	31	33	34	35	36	37	41	42	43	44	45	46	47	48	49	58	59	60	61	62	63	67	69	* **(XC2S200)**
D2(A/E)	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	13	12	11	10	9	8	7	5	* **(A/E)**
																																			* **(Fconn)**
																																			* **(Mconn)**
D2IO (J2)	2	1	4	3	6	5	8	7	10	9	12	11	14	13	16	15	18	17	20	19	22	21	24	23	26	25	27	30	29	32	31	34	33	35	* **(J2)**
CPLD pin Description	B1	B0	B2	G0	G1	G2	R0	R1	HS	VS	KDAT	KCLK	LCD_RS	LCD_RW	NC	LCD_E	D1	D0	D3	D2	D5	D4	D7	D6	WE	CS	OE	A0	CLK	A2	A1	A4	A3	A5	* **(XC95108)**
	VGA										PS2		LCD																						* **USAGE**
																	LED, SW, PB, 7-seg dispay																	

HOW TO READ THIS SUMMARY - (top to bottom)

Row	Description
FPGA PIN	Represents the pin number of the **XC2S200** FPGA on the **D2** board.
D2	FPGA pin # is routed to the **D2** headers **A** and **E** on the edges of the **D2** board.
	When connected to the male header (**J2**) on the **D2IO** board, the pins are connected as shown in the above chart (vertically).
D2IO	The pins of the **J2** connector on the **D2IO** board ar ethen routed to the **CPLD** (bus controller) in the fasion described above.
CPLD	The **CPLD** pins are static and cannot be changed (as far as you are concerned) so the pin descriptions are listed rather that the pin numbers.

*LEGEND

XC2S200	Spartan II FPGA - Main programmable device, located on the Digilab D2 development board.
A/E	I/O Ports A and E on the D2 board are mirrored to allow connection to 2 daughter boards. In EE480 we will use port E for I/O connectivity.
Fconn	Female Connector
Mconn	Male Connector
J2	PCB label found on the Digilab D2IO trainer daughter board. This connector mates with port E of the D2 board.
XC95108	Non-Volitile CPLD programmed to act as a bus controller for the D2IO hardware.
USAGE	Illustrates the target I/O device for associated pin description.

EXAMPLE: To map a **logical port** in your VHDL design to **CS** on the **D2IO** you would assign that **logical port** to pin # **49** using the **constraints editor.**