**FEATURES**

- **SO-8 Package**
- **12-Bit Resolution**
- **Buffered True Rail-to-Rail Voltage Output**
- **External Reference Input Can Be Tied to VCC**
- **Output Swings from 0V to VREF**
- **3V and 5V Supply Operation**
- **Schmitt Trigger on Clock Input Allows Direct Optocoupler Interface**
- **Power-On Reset Clears DACs to 0V**
- **3-Wire Serial Interface**
- **Maximum DNL Error: 0.5LSB**
- **Low Cost**

**APPLICATIONS**

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

**DESCRIPTION**

The LTC®1448 is a dual rail-to-rail voltage output, 12-bit digital-to-analog converter (DAC). It includes rail-to-rail output buffer amplifiers and an easy-to-use 3-wire serial interface. It is available in 8-pin SO and PDIP packages and provides the smallest footprint of any dual 12-bit DAC.

The LTC1448 has an external reference input pin (REF) and its outputs swing from 0V to REF. The REF input can be tied to VCC providing rail-to-rail operation from supplies of 2.7V to 5.5V. (For devices with internal reference see the LTC1446 data sheet.) The LTC1448 dissipates 2.5mW from a 5V supply.

The low power supply current and the small SO-8 package make the LTC1448 ideal for battery-powered applications.

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LTC1448

**Absolute Maximum Ratings**

- $V_{CC}$ to GND: $-0.5V$ to 7.5V
- Logic Inputs to GND: $-0.5V$ to 7.5V
- $V_{OUT_A}$, $V_{OUT_B}$, REF to GND: $-0.5V$ to $V_{CC} + 0.5V$
- Maximum Junction Temperature: 125°C

**Operating Temperature Range**

- LTC1448C: 0°C to 70°C
- LTC1448I: -40°C to 85°C

**Storage Temperature Range**

- -65°C to 150°C

**Lead Temperature (Soldering, 10 sec)**

- 300°C

**Electrical Characteristics**

$V_{CC} = 2.7V$ to 5.5V, $V_{OUT_A}$ and $V_{OUT_B}$ unloaded, REF $\leq V_{CC}$, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC</td>
<td>Resolution</td>
<td>●</td>
<td>12</td>
<td></td>
<td>Bits</td>
<td></td>
</tr>
<tr>
<td>Monotonicity</td>
<td>●</td>
<td>12</td>
<td></td>
<td>Bits</td>
<td></td>
<td></td>
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<tr>
<td>DNL</td>
<td>Differential Nonlinearity</td>
<td>$V_{REF} \leq V_{CC} - 0.1V$ (Note 1)</td>
<td>●</td>
<td>±0.2</td>
<td>±0.5</td>
<td>LSB</td>
</tr>
<tr>
<td>INL</td>
<td>Integral Nonlinearity</td>
<td>$V_{REF} \leq V_{CC} - 0.1V$ (Note 1), $T_A = 25°C$</td>
<td>●</td>
<td>±5.0</td>
<td></td>
<td>LSB</td>
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<tr>
<td>$V_{OS}$</td>
<td>Offset Error</td>
<td>Measured at Code 20, $T_A = 25°C$</td>
<td>●</td>
<td>±10</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Measured at Code 20</td>
<td></td>
<td>●</td>
<td>±15</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$V_{OS_TC}$</td>
<td>Offset Error Temperature Coefficient</td>
<td></td>
<td></td>
<td>±15</td>
<td></td>
<td>µV/°C</td>
</tr>
<tr>
<td>$V_{FS}$</td>
<td>Full-Scale Voltage</td>
<td>$V_{REF} = 4.096V$, $T_A = 25°C$</td>
<td>●</td>
<td>4.070</td>
<td>4.095</td>
<td>4.120</td>
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<tr>
<td>$V_{REF} = 4.096V$</td>
<td></td>
<td>4.060</td>
<td>4.095</td>
<td>4.130</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{FS_TC}$</td>
<td>Full-Scale Voltage Temperature Coefficient</td>
<td></td>
<td>10</td>
<td></td>
<td>ppm/°C</td>
<td></td>
</tr>
</tbody>
</table>

**Power Supply**

- $V_{CC}$ Positive Supply Voltage: For Specified Performance | ● | 2.7 | 5.5 | V |

**Op Amp DC Performance**

- Short-Circuit Current Low: $V_{OUT}$ Shorted to GND | ● | 55 | 120 | mA |
- Short-Circuit Current High: $V_{OUT}$ Shorted to $V_{CC}$ | ● | 65 | 120 | mA |
- Output Impedance to GND: Input Code = 0 | ● | 30 | 120 | Ω |
- Output Line Regulation: Input Code = 4095, $V_{CC} = 4.5V$ to 5.5V, $V_{REF} = 4.096V$ | ● | 0.2 | 1.5 | LSB/V |

Consult factory for Military grade parts.
## ELECTRICAL CHARACTERISTICS

$V_{CC} = 2.7V$ to $5.5V$, $V_{OUTA}$ and $V_{OUTB}$ unloaded, $REF \leq V_{CC}$, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td></td>
<td>AC Performance</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Voltage Output Slew Rate</td>
<td></td>
<td>0.5</td>
<td>1.0</td>
<td>V/µs</td>
<td></td>
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<tr>
<td></td>
<td>Voltage Output Settling Time</td>
<td>(Notes 2, 3) to ±0.5LSB</td>
<td>14</td>
<td></td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Digital Feedthrough</td>
<td></td>
<td>0.3</td>
<td></td>
<td>nV•s</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Reference Input</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>$R_{IN}$</td>
<td>REF Input Resistance</td>
<td></td>
<td>7.5</td>
<td>12.5</td>
<td>18</td>
<td>kΩ</td>
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<td>REF</td>
<td>REF Input Range</td>
<td>(Notes 5, 6)</td>
<td>0</td>
<td></td>
<td>$V_{CC}$</td>
<td>V</td>
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<tr>
<td></td>
<td>Digital I/O</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Digital Input High Voltage</td>
<td>$V_{CC} = 5V$</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Digital Input High Voltage</td>
<td>$V_{CC} = 3V$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Digital Input Low Voltage</td>
<td>$V_{CC} = 5V$</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Digital Input Low Voltage</td>
<td>$V_{CC} = 3V$</td>
<td>0.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{LEAK}$</td>
<td>Digital Input Leakage</td>
<td>$V_{IN} = GND$ to $V_{CC}$</td>
<td></td>
<td>±10</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Digital Input Capacitance</td>
<td>(Note 6)</td>
<td></td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Switching ($V_{CC} = 4.5V$ to $5.5V$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_1$</td>
<td>$D_{IN}$ Valid to CLK Setup</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_2$</td>
<td>$D_{IN}$ Valid to CLK Hold</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_3$</td>
<td>CLK High Time</td>
<td>(Note 6)</td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_4$</td>
<td>CLK Low Time</td>
<td>(Note 6)</td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
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<tr>
<td>$t_5$</td>
<td>$CS/LD$ Pulse Width</td>
<td>(Note 6)</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
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<tr>
<td>$t_6$</td>
<td>LSB CLK to $CS/LD$</td>
<td>(Note 6)</td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_7$</td>
<td>$CS/LD$ Low to CLK</td>
<td>(Note 6)</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_8$</td>
<td>CLK Low to $CS/LD$ Low</td>
<td>(Note 6)</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Switching ($V_{CC} = 2.7V$ to $5.5V$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_1$</td>
<td>$D_{IN}$ Valid to CLK Setup</td>
<td></td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_2$</td>
<td>$D_{IN}$ Valid to CLK Hold</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_3$</td>
<td>CLK High Time</td>
<td>(Note 6)</td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_4$</td>
<td>CLK Low Time</td>
<td>(Note 6)</td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_5$</td>
<td>$CS/LD$ Pulse Width</td>
<td>(Note 6)</td>
<td>80</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_6$</td>
<td>LSB CLK to $CS/LD$</td>
<td>(Note 6)</td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_7$</td>
<td>$CS/LD$ Low to CLK</td>
<td>(Note 6)</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_8$</td>
<td>CLK Low to $CS/LD$ Low</td>
<td>(Note 6)</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:** Nonlinearity is defined from code 20 to code 4095 (full scale). See Applications Information.

**Note 2:** Load is 5kΩ in parallel with 100pF.

**Note 3:** DAC switched between all 1s and the code corresponding to $V_{OS}$ for the part.

**Note 4:** Digital inputs at 0V or $V_{CC}$.

**Note 5:** $V_{OUT}$ can only swing from $(GND + |V_{OS}|)$ to $(V_{CC} - |V_{OS}|)$ when output is unloaded.

**Note 6:** Guaranteed by design, not subject to test.
**PIN FUNCTIONS**

**CLK (Pin 1):** Serial Interface Clock. Internal Schmitt trigger on this input allows direct optocoupler interface.

**DIN (Pin 2):** Serial Interface Data. Data on the DIN pin is latched into the shift register on the rising edge of the serial clock.

**CS/LD (Pin 3):** Serial Interface Enable and Load Control. When CS/LD is low the CLK signal is enabled, so the data can be clocked in. When CS/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output and the CLK is disabled internally.

**REF (Pin 4):** Reference Input for Both DACs. This pin can be tied to VCC. The output will swing from 0V to REF. The typical input resistance is 12.5k.

**VOUT A, VOUT B (Pins 5, 8):** Buffered DAC Outputs.

**GND (Pin 6):** Ground.

**VCC (Pin 7):** Positive Supply Input. 2.7V ≤ VCC ≤ 5.5V. Requires a bypass capacitor to ground.
**DEFINITIONS**

**Differential Nonlinearity (DNL):** The difference between the measured change and the ideal 1 LSB change for any two adjacent codes. The DNL error between any two codes is calculated as follows:

\[
\text{DNL} = \frac{\Delta V_{\text{OUT}} - \text{LSB}}{\text{LSB}}
\]

where \(\Delta V_{\text{OUT}}\) is the measured voltage difference between two adjacent codes.

**Digital Feedthrough:** The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

**Full-Scale Error (FSE):** The deviation of the actual full-scale voltage from ideal. FSE includes the effects of offset and gain errors (see Applications Information).

**Integral Nonlinearity (INL):** The deviation from a straight line passing through the endpoints of the DAC transfer curve (Endpoint INL). Because the output cannot go below zero, the linearity is measured between full scale and the lowest code which guarantees the output will be greater than zero. The INL error at a given input code is calculated as follows:

\[
\text{INL} = \frac{V_{\text{OUT}} - V_{\text{OS}} - (V_{\text{FS}} - V_{\text{OS}})(\text{code}/4095)}{\text{LSB}}
\]

where \(V_{\text{OUT}}\) is the output voltage of the DAC measured at the given input code.

**Least Significant Bit (LSB):** The ideal voltage difference between two successive codes.

\[
\text{LSB} = \frac{V_{\text{REF}}}{4096}
\]

**Resolution (n):** Defines the number of DAC output states \(2^n\) that divide the full-scale range. Resolution does not imply linearity.

**Voltage Offset Error (VOS):** Nominally, the voltage at the output when the DAC is loaded with all zeros. A single supply DAC can have a true negative offset, but the output cannot go below zero (see Applications Information).

For this reason, single supply DAC offset is measured at the lowest code that guarantees the output will be greater than zero.

**OPERATION**

**Serial Interface**

The data on the DIN input is loaded into the shift register on the rising edge of the clock. Data is loaded as one 24-bit word where the first 12 bits are for DAC A and the second 12 are for DAC B. For each 12-bit segment the MSB is loaded first. Data from the shift register is loaded into the DAC register when CS/LD is pulled high. The clock is disabled internally when CS/LD is high. Note: CLK must be low before CS/LD is pulled low to avoid an extra internal clock pulse.

**Voltage Output**

The LTC1448’s rail-to-rail buffered outputs can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 30Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

The output swings from 0V to the voltage at the REF pin, i.e., there is a gain of 1 from the REF to \(V_{\text{OUT}}\). Please note if REF is tied to \(V_{\text{CC}}\) the output can only swing to \((V_{\text{CC}} - V_{\text{OS}})\). See Applications Information.
**APPLICATIONS INFORMATION**

**Rail-to-Rail Output Considerations**

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 1b. Similarly, limiting can occur near full scale when the REF pin is tied to Vcc. If Vref = Vcc and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at Vcc as shown in Figure 1c. No full-scale limiting can occur if Vref is less than Vcc – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

Figure 1. Effects of Rail-to-Rail Operation on a DAC Transfer Curve: (a) Overall Transfer Function, (b) Effect of Negative Offset for Codes Near Zero Scale, (c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When Vref = Vcc
This circuit shows how to use one LTC1448 to make an autoranging ADC. The microprocessor sets the reference span and the Common pin for the analog input by loading the appropriate digital code into the LTC1448. $V_{OUT_A}$ controls the Common pin for the analog inputs to the LTC1296 and $V_{OUT_B}$ controls the reference span by setting the $REF^+$ pin on the LTC1296. The LTC1296 has a Shutdown pin that goes low in shutdown mode. This will turn off the PNP transistor supplying power to the LTC1448. The resistor and capacitor on the LTC1448 outputs act as a lowpass filter for noise.

An Autoranging 8-Channel ADC with Shutdown
TYPICAL APPLICATIONS

Digitally Programmable Current Source

\[ I_{OUT} = \frac{D_{IN} \times 5}{4096 \times R_A} \text{ mA TO 10 mA} \]

\( V_{CC} \) + 6V TO 100V FOR \( RL \leq 50 \Omega \)

\( V_{OUT} \) B PIN NOT SHOWN FOR CLARITY
**PACKAGE DESCRIPTION**

Dimensions in inches (millimeters) unless otherwise noted.

**N8 Package**

8-Lead PDIP (Narrow 0.300)

(LTC DWG # 05-08-1510)

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE
12-Bit, 3V to 5V Supply, Dual Voltage Output DAC

**TYPICAL APPLICATION**

**RELATED PARTS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC1257</td>
<td>Single 12-Bit V\text{OUT} DAC, Full Scale: 2.048V, V\text{CC}: 4.75V to 15.75V, Reference Can Be Overdriven Up to 12V, i.e., F_{\text{SMAX}} = 12V</td>
<td>5V to 15V Single Supply, Complete V\text{OUT} DAC in SO-8 Package</td>
</tr>
<tr>
<td>LTC1446/LTC1446L</td>
<td>Dual 12-Bit V\text{OUT} DACs in SO-8 Package with Internal Reference</td>
<td>LTC1446: V\text{CC} = 4.5V to 5.5V, V\text{OUT} = 0V to 4.095V LTC1446L: V\text{CC} = 2.7V to 5.5V, V\text{OUT} = 0V to 2.5V</td>
</tr>
<tr>
<td>LTC1450/LTC1450L</td>
<td>Single 12-Bit V\text{OUT} DACs with Parallel Interface</td>
<td>LTC1450: V\text{CC} = 4.5V to 5.5V, V\text{OUT} = 0V to 4.095V LTC1450L: V\text{CC} = 2.7V to 5.5V, V\text{OUT} = 0V to 2.5V</td>
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<tr>
<td>LTC1451</td>
<td>Single Rail-to-Rail 12-Bit DAC, Full Scale: 4.095V, V\text{CC}: 4.5V to 5.5V, Internal 2.048V Reference Brought Out to Pin</td>
<td>5V Low Power, Complete V\text{OUT} DAC in SO-8 Package</td>
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<tr>
<td>LTC1452</td>
<td>Single Rail-to-Rail 12-Bit V\text{OUT} Multiplying DAC, V\text{CC}: 2.7V to 5.5V</td>
<td>Low Power, Multiplying V\text{OUT} DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package</td>
</tr>
<tr>
<td>LTC1453</td>
<td>Single Rail-to-Rail 12-Bit V\text{OUT} DAC, Full Scale: 2.5V, V\text{CC}: 2.7V to 5.5V</td>
<td>3V, Low Power, Complete V\text{OUT} DAC in SO-8 Package</td>
</tr>
<tr>
<td>LTC1454/LTC1454L</td>
<td>Dual 12-Bit V\text{OUT} DACs in SO-16 Package with Added Functionality</td>
<td>LTC1454: V\text{CC} = 4.5V to 5.5V, V\text{OUT} = 0V to 4.095V LTC1454L: V\text{CC} = 2.7V to 5.5V, V\text{OUT} = 0V to 2.5V</td>
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<tr>
<td>LTC1456</td>
<td>Single Rail-to-Rail Output 12-Bit DAC with Clear Pin, Full Scale: 4.095V, V\text{CC}: 4.5V to 5.5V</td>
<td>Low Power, Complete V\text{OUT} DAC in SO-8 Package with Clear Pin</td>
</tr>
<tr>
<td>LTC1458/LTC1458L</td>
<td>Quad 12 Bit Rail-to-Rail Output DACs with Added Functionality</td>
<td>LTC1458: V\text{CC} = 4.5V to 5.5V, V\text{OUT} = 0V to 4.095V LTC1458L: V\text{CC} = 2.7V to 5.5V, V\text{OUT} = 0V to 2.5V</td>
</tr>
<tr>
<td>LTC1659</td>
<td>Single Rail-to-Rail 12-Bit V\text{OUT} DAC in MSOP-8 Package, V\text{CC}: 2.7V to 5.5V</td>
<td>Low Power Multiplying V\text{OUT} DAC in MSOP-8 Package. Output Swings from GND to REF. REF Input Can Be Tied to V\text{CC}</td>
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