Small-area decimators for delta-sigma video sensors

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ABSTRACT

A delta-sigma, or sigma-delta, analog-to-digital converter (ADC) comprises both a modulator, which implements oversampling and noise shaping, and a decimator, which implements low-pass filtering and downsampling. Whereas these ADCs are ubiquitous in audio applications, their usage in video applications is emerging. Because of oversampling, it is preferable to integrate delta-sigma ADCs at the pixel level of megapixel video sensors. Moreover, with pixel-level applications, area usage per ADC is much more important than with chip-level applications, where there is only one or a few ADCs per chip. Recently, a small-area decimator was presented that is suitable for pixel-level applications. However, though the pixel-level design is small enough for invisible-band video sensors, it is too large for visible-band ones. As shown here, nanoscale CMOS processes offer a solution to this problem. Given constant specifications, small-area decimators are designed, simulated, and laid out, full custom, for 180, 130, and 65 nm standard CMOS processes. Area usage of the whole decimator is analyzed to establish a roadmap for the design and demonstrate that it could be competitive compared to other digital pixel sensors, based on Nyquist-rate ADCs, that are being commercialized.

Keywords: CMOS image sensors, video technology, integrated circuits, digital pixel sensors, analog-to-digital converters, decimation, scalability, nanotechnology.

1. INTRODUCTION

Pixel-level analog-to-digital converters (ADCs) solve a major problem of nonlinear complementary metal-oxide-semiconductor (CMOS) image sensors, which is their low signal-to-noise-and-distortion ratio (SNDR) relative to linear CMOS image sensors. Using a logarithmic digital pixel sensor (DPS) array, where logarithmic sensors are integrated with in-pixel delta-sigma (ΔΣ) ADCs, Mahmoodi and Joseph demonstrated a peak SNDR (PSNDR) competitive with the human eye and linear active pixel sensor (APS) arrays. The advantage of logarithmic sensors over linear ones is that they easily achieve wide dynamic range (DR) at video rates.

A ΔΣ ADC is composed of two parts: a modulator and a decimator. Although a ΔΣ modulator is an ADC of sorts, it is not a ΔΣ ADC without a decimator. Early work on pixel-level “ΔΣ ADCs”, led by a Stanford lab, left the decimator outside the pixel. Classical decimators, intended for one or a few ADCs per chip, are too large to put inside pixels of useful size. However, performing decimation outside pixels limits the frame rate and/or the oversampling ratio, where the latter limits the SNDR. As a result, the Stanford lab abandoned the ΔΣ approach, which was their initial choice, to investigate alternative DPS architectures.

Though not obvious, decimators small enough to make useful pixel-level ΔΣ ADCs are indeed possible, as disclosed by Joseph and Mahmoodi in a pending patent. Using the patented technology, Mahmoodi et al. also presented a DPS-based image sensor. While it achieves wide DR and high SNDR at video rates, the pixel area is still too large for visible-band applications. Developed in a 180 nm process, the decimator that was used is purely digital and represents a significant part of the DPS layout area. Digital circuits, unlike analog ones, benefit directly from scaling, in compliance with Moore’s Law. So, it is expected that the decimator, through scaling, will eventually be small enough for visible-band image sensors.

In general, ΔΣ ADCs behave really well for low sampling rate and high bit resolution applications, which is the case of pixel-level ADCs for image sensors. So ΔΣ ADCs are a good choice provided they can be made small enough. Fortunately, there is a minimum pixel size due to optical considerations of image sensors, so the large-area drawback will become less of an issue as CMOS technology scales down.
In this work, full-custom decimator designs for 180, 130, and 65 nm standard CMOS processes are presented in order to create a roadmap for area usage of the corresponding ∆Σ ADC and DPS. By determining a trendline for the decimator circuit, projections for pixel pitch can be made assuming the decimator width determines the pixel pitch.

This paper is organized in the following manner. Section 2 presents the schematic of the decimator and summarizes the innovative aspects of its circuit. Section 3 explains the procedure followed here for producing the three decimator designs and gives the results, including an analysis of area usage and pixel pitch. Section 4 compares the decimator and associated DPS with the state of the art, especially a commercial DPS. Finally, Section 5 summarizes the main points made by this paper.

2. BACKGROUND

The main tasks of a ∆Σ decimator are to filter out-of-band components and quantization noise, shaped by the ∆Σ modulator, and to down-sample the filtered signal to the Nyquist rate. Several decimation methods have been developed. However, they are either meant for stand-alone ∆Σ ADCs or for sharing among many ∆Σ modulators. In the first case, area usage is not a concern so it is not applicable to this work, given that this work concerns a ∆Σ ADC that will be included in each pixel of an array of pixels. In the second case, sharing the decimator across many pixels, e.g., a column of pixels, has a negative effect on the SNDR of said ADCs because it limits the sampling and/or oversampling rates.

Candy has concluded that, given a modulator of order \( l \), a decimator based on a comb filter of order \( l + 1 \) offers a near-optimal response in terms of noise filtering. A decimator based on a second-order comb filter, with triangular impulse response, is typically used with a first-order modulator. However, an approach based on the decimator by Mahmoodi and Joseph has been chosen because it is a simpler way, i.e., using less area per ADC, to implement an array of decimators for an array of in-pixel ∆Σ modulators. These parallel decimators are based on a parabolic filter, which offers optimal noise filtering for a first-order modulator.

In the rest of this section, the decimator circuit is described. As shown in Fig. 1, it includes a one-bit full adder, a one-bit register (i.e., a flip flop), an \( N \)-bit shift register, two NOR gates, and three inverters. Table 1 breaks down the transistor count for the decimator circuit.

The decimator receives the modulator output, which is a one-bit signal at the oversampling rate. This rate determines the frequency at which the digital circuits in the decimator must work to guarantee proper operation of the ADC. Each value at the output of the modulator must be multiplied to a serial coefficient of the parabolic filter, which is generated at chip level, and then accumulated. The process occurs for \( M \) coefficient values, \( M \) being the oversampling ratio (OSR) of the modulator. Since both the output of the modulator and the coefficients are serial, the multiplication function can be easily implemented by an AND gate. In order to use the minimum number of transistors, a NOR gate is used instead. In this case, the inputs of the decimator will be inverted versions of the modulator output and serial coefficients.

The one-bit full adder performs the arithmetic sum of the bit serial accumulator. Fig. 2(a) shows the schematic used to implement the one-bit full adder. Since timing constraints are not the limiting parameter.

Table 1. Blocks and transistor counts of the decimator. Here, \( N \) is assumed to be a multiple of 4, i.e., an integer number of nibbles. Assuming \( N \geq 8 \), the shift register dominates the transistor count of the decimator.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Block(s)</th>
<th>Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Inverters</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>NORs</td>
<td>8</td>
</tr>
<tr>
<td>1</td>
<td>1-bit register</td>
<td>10</td>
</tr>
<tr>
<td>1</td>
<td>1-bit full adder</td>
<td>24</td>
</tr>
<tr>
<td>1</td>
<td>N-bit shift register</td>
<td>10N</td>
</tr>
<tr>
<td></td>
<td>Total</td>
<td>48 + 10N</td>
</tr>
</tbody>
</table>
for the decimator, skewed gates are used to minimize the width of the PMOS transistors, i.e., the PMOS and NMOS transistors have a 1 : 1 ratio even though the respective carrier mobilities do not have a 1 : 1 ratio.

The one-bit register, i.e., a flip flop, is used to store and feed back the carry out of the one-bit full adder. Flip flops, being part of the $N$-bit shift register, are also used to store the accumulator data. As described in Mahmoodi and Joseph’s pending patent application,\textsuperscript{10} and in Mahmoodi’s PhD thesis,\textsuperscript{5} two pulsed latches were chosen to implement each flip flop, which utilizes only eight transistors. Though this approach works in a 180 nm process, it does not do so in 130 and 65 nm processes. As a result, one extra transistor is required per latch to ensure correct behavior for all processes. The circuit is shown in Fig. 2(b).

Among the technology nodes considered, the 65 nm one presents a higher leakage current that considerably affects the behavior of the flip flop. Switches in the two pulsed latches are leaky and cause undesirable behavior in the flip flop, shift register, and the entire decimator. In order to avoid this, low threshold-voltage transistors are needed with the 130 and 65 nm processes. Even though the amount of leakage current does not significantly affect overall behavior in the 180 nm process, we could use low threshold-voltage transistors in this process as well. However, this kind of transistor was not available in the chosen 180 nm process so regular transistors were used for the switches. Also, because the flip flops might be sensitive to the clock slope, an inverter per decimator per clock is included in order to sharpen the clock signal coming from the chip level.

The total number of transistors in the decimator circuit is $48 + 10N$. Assuming the number of bits of the $N$-bit register is 16, 208 transistors per decimator are needed. Because the accumulator needs to be reset after the accumulation is done, a second NOR gate is listed in Table 1 to implement this function.

3. SCALING

Previous work related to the scaling of digital circuits\textsuperscript{15–17} has shown the problems to overcome when migrating to newer processes. It also predicts further complications specific to nanoscale processes. Moreover, options
Figure 2. Schematics of the full adder and the flip flop. (a) This one-bit full adder, along with a shift register, implements bit serially the accumulator of the ΔΣ decimator. Inverted outputs, $\bar{S}$ and $\bar{C}_{\text{out}}$, suffice. (b) This flip flop, using two pulsed latches, is the building block of the shift register. Asterisks indicate low-voltage transistors (130 and 65 nm processes).

for metallization (number of metal layers), pitch of metal interconnections, and available devices vary from one process to another, making the process of scaling down circuits even more complex. To show the transition of the DPS circuit from the 180 nm process, the next technology node, i.e., 130 nm, was selected. Also, in order to explore the limitations when designing in the nanoscale regime, a 65 nm process was selected.

This section systematically presents three designs made in the aforementioned technologies. Also, the decision-making process used to adapt the decimator circuit, made previously by Mahmoodi in a 180 nm process, for these new designs is presented.

### 3.1 Layout Design

A full-custom layout is desirable because it can be optimized for area as much as possible, which is not the case for automatically-generated layouts or even semi-custom layouts made from standard cells. Also, a hierarchical layout creation was preferred over a flat one because it is easier to debug and, most importantly, because it enables reuse of sub-blocks to form major blocks and facilitates scaling. In order to plan and create the layout of the decimator, a mix between top-down and bottom-up organization was used.

The top-down organization was necessary to appropriately place the different cells and determine the way they will interact, spatially and functionally, between each other in the layout. For this, the floorplanning of the entire decimator (highest hierarchy), prior to the completion of the layout of each sub-block (lowest hierarchy), and tentative placements of the inputs and outputs of sub-blocks were required, as shown in Fig. 3.
From Fig. 3(a), the area of the decimator, $A_D$, can be calculated as

$$A_D = H_D (W_{SR} + W_{MB}),$$

where $W_{SR}$ and $W_{MB}$ are the widths of the shift register and a “macro” block, respectively. The macro block is formed from the other sub-blocks together. Finally, $H_D$ represents the height of the decimator.

The height of the decimator, $H_D$, is given by the height of the shift register, which stacks four rows of flip flops. It is expected that the shift register will have a number of bits, e.g., 12, 16, or 20, that is a multiple of four. With microelectronics, it is common and therefore convenient to represent binary numbers as an integer multiple of nibbles, i.e., four bits. The width of the shift register, as shown in Fig. 3(b), depends directly on its number of bits. For efficient use of area, the height of the macro block should also be $H_D$.

Bottom-up organization, in addition to the top-down organization, was necessary to complete the layout of the sub-blocks, treated as “black boxes” in the top-down approach. For each cell, a custom layout was created taking into account the desirable placement of inputs and outputs, given by the top-down approach. It is important to consider the overlapping area of the cells so they fit perfectly when putting them together.

For the particular case of the $N$-bit shift register, which is a repetitive block composed of one flip flop per bit, knowing the overlapping area between flip flops is required to compute the area usage of the $N$-bit shift register. The area of the $N$-bit shift register, $A_{SR}$, is $H_D W_{SR}$, where $H_D$ and $W_{SR}$ are calculated as follows:

$$H_D = 4W_{FF} - 2\Delta H_1 - \Delta H_2,$$

$$W_{SR} = \left(\frac{N}{4}\right) W_{FF} - \left(\frac{N}{4} - 1\right) \Delta W + L_1 + L_2.$$  

As shown in Fig. 3(b): $W_{FF}$ and $H_{FF}$ are the width and height of a flip flop; $\Delta W$ is the overlapped section for $W_{FF}$; $\Delta H_1$ and $\Delta H_2$ are the overlapped sections for $H_{FF}$ due to VSS/VDD sharing in mirrored flip flops; and $L_1$ and $L_2$ are the additional sections used for local interconnects. Table 2 gives the designed values for the 180, 130, and 65 nm CMOS processes.

Considering $N = 16$, we can conclude that 77% of the transistors of the decimator are concentrated in the shift register. Since its basic building block is the flip flop, efforts should focus on optimizing this sub-block. Furthermore, preliminary results for the decimator, in terms of area usage, can be obtained by observing the area trend of a flip flop. Fig. 4 shows the layouts of the flip flop made in the three processes.

Shown in Fig. 5, the layout of the decimator made in the three processes follows the floorplan shown in Fig. 3. Also, since the objective is reducing the pitch of the pixel, and because the shift register has a “fixed” width given by (3), the width of the macro block has been made as small as possible.
Figure 4. Layouts of the flip flop in three processes. Chosen processes are available through CMC Microsystems. As all layouts are shown at the same scale, area reduction is plain to see. This component dominates the decimator layout.

Table 3 gives the dimensions of the decimator that was designed in the three processes, as depicted in Fig. 5. It is plain to see that the area reduction from 180 to 130 and 65 nm is considerable.

3.2 Analysis

In the previous subsection, results for decimator layouts in three processes, i.e., technology nodes, were shown. These results may be used to develop a roadmap for pixel pitch, assuming that the ADC determines the pixel size, which would be true if the detector and other circuits are vertically integrated.

From Fig. 3(a), the $\Delta\Sigma$ modulator, which is shown with dotted lines, is to be laid out to have the same width as the decimator, while its height, $H_M$, is determined by the layout needs. Since the pixel pitch is determined

Table 2. Layout parameters of the decimator in three processes. Parameters, in $\mu$m, are defined in Fig. 3.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>180 nm</th>
<th>130 nm</th>
<th>65 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$H_{FF}$</td>
<td>3.92</td>
<td>2.58</td>
<td>1.75</td>
</tr>
<tr>
<td>$\Delta H_1$</td>
<td>0.70</td>
<td>0.50</td>
<td>0.23</td>
</tr>
<tr>
<td>$\Delta H_2$</td>
<td>0.82</td>
<td>0.32</td>
<td>0.23</td>
</tr>
<tr>
<td>$W_{FF}$</td>
<td>8.90</td>
<td>7.02</td>
<td>3.67</td>
</tr>
<tr>
<td>$\Delta W$</td>
<td>0.79</td>
<td>0.56</td>
<td>0.43</td>
</tr>
<tr>
<td>$L_1$</td>
<td>0.61</td>
<td>0.34</td>
<td>0.08</td>
</tr>
<tr>
<td>$L_2$</td>
<td>0.61</td>
<td>0.34</td>
<td>0.08</td>
</tr>
<tr>
<td>$H_D$</td>
<td>13.46</td>
<td>9.00</td>
<td>6.31</td>
</tr>
<tr>
<td>$W_{SR}$</td>
<td>34.47</td>
<td>27.08</td>
<td>13.55</td>
</tr>
<tr>
<td>$W_{MB}$</td>
<td>8.71</td>
<td>6.86</td>
<td>3.48</td>
</tr>
</tbody>
</table>

Table 3. Layout area of the decimator in three processes. Reduction relative to the 180 nm design is indicated.

<table>
<thead>
<tr>
<th>Node (nm)</th>
<th>Area ($\mu$m$^2$)</th>
<th>Reduction (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>$43.17 \times 13.46$</td>
<td>-</td>
</tr>
<tr>
<td>130</td>
<td>$33.94 \times 9.00$</td>
<td>47</td>
</tr>
<tr>
<td>65</td>
<td>$17.03 \times 6.31$</td>
<td>82</td>
</tr>
</tbody>
</table>
Figure 5. Layouts of the decimator in three processes. In each layout, the macro block and shift register are on the left and right, respectively. The layouts show the degree to which process scaling can shrink the decimator.

by the maximum of \( H_D + H_M \) and \( W_{MB} + W_{SR} \), and because the latter is much greater than \( H_D \) according to Table 2, the pitch of the pixel will be given by the width of the decimator, provided the height of the modulator is small enough for this to be valid.

As shown in Fig. 6, the pitch of the pixel would go from 43.2 to 17.0 \( \mu \text{m} \) with the three technology nodes used in this paper, relying on scaling only. The area reduction obtained at the 65 nm node, relative to the 180 nm one, is 82%. With further optimization at the circuit and system (CAS) level, an even greater reduction is expected. The figure also shows that the pixel pitch trend is approximately linear.

4. DISCUSSION

This section puts the decimator, as part of a \( \Delta \Sigma \) ADC, in the context of the DPS technology. Furthermore, it discusses the selection of the \( \Delta \Sigma \) ADC, for inclusion at pixel level, over alternative ADC architectures.

Major attempts to make DPS technology a viable option for image sensors have come from the Information Systems Laboratory at Stanford University.\(^2\)\(^,\)\(^4\)\(^,\)\(^7\)\(^,\)\(^8\) They have developed three DPS generations,\(^12\) where the first involved a pixel-level \( \Delta \Sigma \) modulator and the second and third involved Nyquist-rate ADCs. A summary of this work is given in Table 4.

In-pixel \( \Delta \Sigma \) ADCs offer several advantages over their Nyquist-rate counterparts. First of all, temporal noise filtering is possible in an oversampled ADC without using a low-pass filter at the input of the ADC.\(^13\) Also, trading of bit resolution with frame rate and the fact that \( \Delta \Sigma \) ADCs are more robust to analog imperfections, which facilitates scaling to newer technology nodes, are other important advantages.
Figure 6. Pixel pitch versus technology node. Assuming the decimator width determines the DPS pitch, the pixel pitch is approximately a linear function of technology node. Extrapolating from the 180, 130, and 65 nm layouts, by the 14 nm technology node a 7 µm pixel pitch is expected, which is a benchmark for visible-band applications.

According to Fowler et al.,\textsuperscript{20} the main disadvantages of the ΔΣ modulator approach, and certainly the reasons why the Stanford lab migrated to other in-pixel ADC architectures, was its large pixel area and high output data rate due to oversampling. The latter is because the decimation was performed externally in software, not in the pixel, which places severe requirements on the input/output bandwidth.

Mahmoodi et al. presented a true ΔΣ ADC, i.e., where the decimator was integrated at pixel level,\textsuperscript{2} achieving high values for both DR and SNDR. Although high output data rate is no longer a problem, area usage was still too large for visible-band applications. Showing how to overcome this problem has been the focus of this paper.

### 4.1 Exploiting Scaling

Because optical requirements do not scale with technology, i.e., there is a fixed lower bound for pixel pitch, the large area of in-pixel ΔΣ ADCs can benefit from scaling, so area usage will eventually cease to be a limiting factor. A commercial DPS design, by Pixim, which was originally developed by the Stanford lab,\textsuperscript{9,21} is used as a benchmark here to assess the competitiveness of the in-pixel ΔΣ ADC approach.

By using the decimator design presented here, which is simple and uses basic digital circuits, it could be possible to reduce the pixel size to make it suitable for the visible band. Hence, if the main drawbacks that caused other researchers to move from ΔΣ architectures to Nyquist-rate ones are overcome, through innovations and scaling, in-pixel ΔΣ ADCs are worth reconsidering.

### Table 4. Specifications of competing DPS designs.

Work of the Information Systems Laboratory at Stanford University is presented chronologically. Three of these designs integrate one ADC per $2 \times 2$ pixels, i.e., one colour pixel.

<table>
<thead>
<tr>
<th>CMOS DPS</th>
<th>Node (µm)</th>
<th>Area (µm$^2$)</th>
<th>ADC Type</th>
<th>Transistors (per pixel)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fowler et al.\textsuperscript{3}</td>
<td>1.2</td>
<td>60 × 60</td>
<td>ΔΣ modulator</td>
<td>22</td>
</tr>
<tr>
<td>Yang et al.\textsuperscript{4}</td>
<td>0.8</td>
<td>20.8 × 20.8</td>
<td>ΔΣ modulator</td>
<td>17/4</td>
</tr>
<tr>
<td>Yang et al.\textsuperscript{7}</td>
<td>0.35</td>
<td>10.5 × 10.5</td>
<td>MCBS</td>
<td>18/4</td>
</tr>
<tr>
<td>Kleinfeldler et al.\textsuperscript{8}</td>
<td>0.18</td>
<td>9.4 × 9.4</td>
<td>Ramp-compare</td>
<td>37</td>
</tr>
<tr>
<td>Bidermann et al.\textsuperscript{9}</td>
<td>0.18</td>
<td>7 × 7</td>
<td>MCBS</td>
<td>22/4</td>
</tr>
</tbody>
</table>
Because a DPS is a mixed-signal circuit, it is expected that, while the digital part benefits from process scaling, the analog part does not necessarily do so. The DPS developed by Pixim uses a multi-channel bit-serial (MCBS) ADC. This kind of ADC presents mostly analog components, which makes the scaling of this DPS to newer technology nodes more complex and less beneficial. The DPS architecture based on the \( \Delta \Sigma \) ADC does not have this problem.

Considering the transistor counts of both the modulator and the decimator, as reported by Mahmoodi and Joseph,\(^2\) and keeping in mind that the folded cascode operational transconductance amplifier (OTA) is the only analog block (23 transistors) in the modulator, 92% of the \( \Delta \Sigma \) ADC is digital. This enables substantial area reduction through scaling. Such a perspective is borne out by the actual scaling results shown in this paper for the decimator alone.

Another relevant point to take into account is that while the pitch of Pixim’s pixels is 7\( \mu \)m, the Pixim image sensors actually share one ADC per 2\( \times \)2 pixels. Thus, because this work focused on one ADC per pixel, a first-order estimate of the benchmark pitch without sharing is 14\( \mu \)m. As shown in Fig. 6, we expect a 17\( \mu \)m pixel pitch, which is close, with the \( \Delta \Sigma \) ADC architecture at the 65 nm node.

By following a trendline established by linear regression on actual data, the same figure indicates that the pixel pitch with the \( \Delta \Sigma \) ADC could reach even the 7\( \mu \)m benchmark by scaling to the 14 nm technology node. For simplicity, this projection assumes the pixel pitch is determined by decimator width. In practice, modulator scaling needs to be investigated. Moreover, sensor and readout circuits need to be considered, although these can be vertically integrated\(^22\) to minimize their impact on DPS area.

### 4.2 Circuit Sharing

As shown in Table 4, several designs by the Stanford lab, including the one commercialized via Pixim, shared one ADC per 2\( \times \)2 pixels. This is reasonable given that one colour pixel may be formed by putting together 2\( \times \)2 pixels with an overlaid pattern of colour filters. The same idea could be applied to the \( \Delta \Sigma \) ADC approach investigated here.

If we were to share one ADC, the blocks that could not be shared would be the integrating capacitors, in the modulator, and the shift register, in the decimator. These are the parts that store state information, either in analog or digital form, specific to each pixel.

Sharing one \( \Delta \Sigma \) modulator across 2\( \times \)2 pixels could reduce pixel pitch greatly. Although integrating capacitors cannot be shared, they can be placed in metal layers above other circuitry, which means they can be discounted in terms of layout area. As shown in Section 3, because the macro block constitutes 23% of the decimator transistors, approximately three quarters of it, or about 17% of decimator transistors, could be saved per pixel through sharing.

### 5. CONCLUSION

DPS technology offers a way to achieve image sensors with wide DR and high PSNDR simultaneously at video rates. Though DPS research initially concerned oversampled ADCs, Nyquist-rate ADCs were used in a recent commercial application. Early attempts for using \( \Delta \Sigma \) “ADCs”, which are the main type of oversampled ADCs, did not include the decimator at pixel level, which caused a high output data rate. As this problem was solved recently, the oversampled approach has reemerged.

This work focuses on the decimator invented by Mahmoodi and Joseph.\(^10\) The circuit is interesting because it is much smaller than previous decimators, includes really simple logic gates, and enables a true in-pixel \( \Delta \Sigma \) ADC. Although the circuit has been included in a DPS-based image sensor, pixels were still too large for visible-band imaging. This issue is less of a problem with newer technologies, as the digital parts of the \( \Delta \Sigma \) ADC, a mixed-signal circuit, may be naturally reduced through scaling. This paper, in particular, analyzes the area usage of the innovative decimator to produce a roadmap for the corresponding DPS technology.

The roadmap is determined by designing and laying out the decimator in 180, 130, and 65 nm standard CMOS processes, i.e., in three technology nodes. Each layout was started using a top-down approach to set the floorplanning of the blocks, the sub-blocks, and the way inputs and outputs interact (to avoid future problems
when assembling the entire decimator). A bottom-up approach was then used to complete the layout of the blocks and sub-blocks, which were treated as “black boxes” in the top-down approach. Full-custom design of every block was done so the area usage would be as small as possible.

For simplicity, we assume that decimator width determines pixel pitch. Because pixel pitch does not need to scale with technology node, scaling is a feasible way to eventually realize an in-pixel ΔΣ ADC that is sufficiently small for visible-band applications. A suitable benchmark for pixel pitch is 7 µm, which has been established by a recent DPS technology, based on Nyquist-rate ADCs, that was commercialized by Pixim.

Compared to the 180 nm design, the decimator layout area was reduced by 82% with the 65 nm technology node, obtaining a 17 µm pixel pitch. The three data points that were realized, one for each CMOS process, form approximately a straight trendline. Extrapolating, we predict that, relying on scaling only, the target 7 µm pitch would be reached by the 14 nm technology node. Considering what was done with the Nyquist-rate ADC in the benchmark DPS technology, the target pitch could be achieved at an earlier technology node by sharing one ΔΣ ADC per 2 × 2 pixels.

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