Application Note: Design and Fabrication of a VI-CMOS Image Sensor

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Design and Fabrication of a VI-CMOS Image Sensor

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1. SCOPE

This application note starts with a motivation for vertical stacking of integrated circuits, focusing on the benefits for electronic image sensors. Next, it considers general principles in the design of vertically-integrated (VI) CMOS image sensors that are fabricated by flip-chip bonding. These sensors are composed of a silicon die with CMOS circuits and a transparent die with photodetectors. As a specific example, the note presents a VI-CMOS image sensor that was designed at the University of Alberta, and fabricated with the help of CMC Microsystems and Micralyne Inc. Finally, recommendations are made for future projects of a similar nature.

2. BACKGROUND

Vertical stacking of integrated circuits (ICs), where one die is placed above another, is a growing trend in IC design. The approach offers several advantages over planar technologies. First, only one package is required for several dies, which makes it possible to build lighter and more compact systems. Second, because the long traces on a printed circuit board (PCB) are replaced by much shorter connections between dies, the resistance (R) and capacitance (C) of interconnects are significantly lowered. This results in a notable reduction in transmission power loss. Moreover, RC delays become smaller and, therefore, the interconnect bandwidth increases. In addition, the information flow between dies may be raised substantially with vertical integration because the number of connections between dies is area-limited, not perimeter-limited as with planar technologies.

3. DESCRIPTION OF APPLICATION

The capabilities of vertically-integrated (VI) image sensors are likely to surpass those of planar image sensors. Vertical integration enables multi-tier image sensors, where each tier is fabricated in a technology optimized for the type of devices it contains. Image sensors require several types of devices: photodetectors for sensing; analog circuits for amplification and pre-processing; and digital circuits for control and post-processing. While digital circuits may exploit the advantages of a nanoscale CMOS process, photodetectors may be fabricated in a larger scale process. Analog circuits may be fabricated in an intermediate scale process or, with robust design methods, in the same process as the digital ones. Furthermore, in some fabrication methods, the photodetector tier need not use crystalline silicon, which makes it easier to target invisible bands of the electromagnetic spectrum.

For vision applications, image sensors should have features such as high spatial and temporal resolution, high signal-to-noise ratio, high dynamic range, and low dark limit. Advanced pixel-level circuitry, such as digital pixel sensors (DPS), may be used to address these competing requirements. With CCD technology, however, standard CMOS circuits may not be integrated either in the pixel or elsewhere on the chip. Although DPS is possible with CMOS technology, in-pixel circuits and photodetectors must be laterally integrated. Thus, it is impossible to use advanced circuitry without either having impractical pixel dimensions or using a nanoscale CMOS process, which is less suitable for photodetection. VI-CMOS technology aims to overcome this dilemma by distributing semiconductor devices across overlapping tiers. In theory, it enables small pixels for high spatial resolution and also advanced pixel-level circuitry to address other important measures of imaging performance.

Fig. 1 shows a VI-CMOS image sensor, made by flip-chip bonding, next to a CMOS image sensor. Both were designed at the University of Alberta (UofA). Although VI-CMOS image sensors have been demonstrated in the United States, Belgium, and Germany, no such sensor has previously been prototyped via CMC Microsystems. The closest known Canadian work was done by Hosseini, who integrated a microfluidic chip with a CMOS image sensor by flip-chip bonding. In Hosseini’s work, vertical integration was not used to construct the pixels themselves. Bond pads in the vertical integration were on the perimeter of the image sensor only.
Figure 1. CMOS and VI-CMOS image sensors designed at the University of Alberta and fabricated via CMC Microsystems. (a) The CMOS sensor was fabricated in a 0.35 μm TSMC process. Each pixel contains a photodetector integrated laterally with CMOS transistors. (b) The VI-CMOS sensor comprises a silicon die with CMOS circuits (bottom) and a glass die with photodetectors (top) that were assembled by flip-chip bonding. Whereas the CMOS die was fabricated in a standard 0.8 μm DALSA process, the photodetector die was fabricated in a custom process via Micralyne Inc and the UofA Nanofab. Each pixel contains a photodetector integrated vertically with CMOS transistors.

4. PRINCIPLES OF DESIGN AND FABRICATION

VI-CMOS image sensors may be designed for different fabrication methods, as shown in Fig. 2. With thinned substrate\(^8\) and thin-film-on-ASIC (TFA)\(^9\) technologies, semiconductor devices may be vertically integrated on one die, enabling monolithic VI-CMOS image sensors. With flip-chip technology,\(^10\) VI-CMOS image sensors are composed of two dies that are assembled face-to-face using metallic interconnects after separate fabrication. Through-substrate-via (TSV) technologies may be used to vertically integrate two or more dies. Front-to-back electrical connections between dies are possible by etching holes through substrates and metalizing them. Burns \textit{et al.}\(^11\) demonstrated a TSV image sensor with three tiers using stacked silicon-on-insulator (SOI) technology. Top, middle, and bottom tiers were dedicated to photodetectors, analog circuits, and digital circuits, respectively. While all tiers were fabricated using SOI substrates, each tier had its own process scale.

Our first efforts towards a prototype concerned TFA technology. However, TFA requires extensive post-processing of finished CMOS substrates, including surface planarization and film deposition. Despite our access to the UofA Nanofab, a state-of-the-art nanofabrication facility, process development was very difficult without whole CMOS wafers. Using a multi-project wafer service, we could obtain only tens of CMOS dies at a relatively low cost. Furthermore, because the CMOS dies were fabricated in a commercial process, the exact materials and dimensions involved were trade secrets, which made it more difficult to develop compatible post-processing.

In 2007, we switched to flip-chip technology because it was the only way to make a VI-CMOS image sensor with the support of CMC, the umbrella organization for Canadian microsystems. At the time, TSV technologies were still in development – there were no TSV services available through CMC. Flip-chip technology required the design and fabrication of a CMOS die (Section 4.1) and a photodetector die (Section 4.2), as shown in Fig. 3. These dies are assembled by flip-chip bonding (Section 4.3) to make a VI-CMOS image sensor.

4.1 CMOS Die

The CMOS die in Fig. 3(a) was designed for a standard CMOS process. Design of a CMOS die for a VI-CMOS image sensor is similar to the design of a CMOS image sensor, but there are some important differences.
Typical CMOS image sensors are composed of: active pixels, which amplify photodetector signals; row and column address decoders, which select pixel signals for readout; column and output buffers, which route selected signals to output buses; and analog-to-digital converters (ADC), which transform the output signals. In addition to the photodetectors, these readout circuits define how photogenerated charge carriers are interpreted. In general, the digital response is a linear or logarithmic function of the light stimulus. Usually, a few ADCs are included for all pixels. However, designs that include one or two ADCs per column, or column-level ADCs, are increasingly common. Further details on CMOS image sensor design may be found in the literature.\textsuperscript{12–14}

As with a CMOS image sensor, the floor plan of a CMOS die designed for a VI-CMOS image sensor also requires active pixels, address decoders, buffers, and one or more ADCs. However, unlike CMOS image sensors, there is no photodetector in the pixel layout. Instead, each pixel has a bond pad to form an electrical contact with a vertically-integrated photodetector after flip-chip bonding. Like typical CMOS chips, a VI-CMOS image sensor also requires peripheral bond pads for wire bonding to a package that can be soldered onto a PCB.

For visible-band image sensors, the motivation for VI-CMOS over CMOS technology is to facilitate one ADC per pixel. With conventional CMOS image sensors, analog signals must travel outside the pixel array for conversion to digital signals. While traveling, they accumulate noise. Because digital signals are far more immune to noise than analog ones, the signal-to-noise ratio is expected to improve with pixel-level ADCs. However, as ADCs require complex circuits, building them in a CMOS technology suitable for visible-band imaging implies a relatively low spatial resolution. Further details on pixel-level ADCs may be found in the literature.\textsuperscript{15,16}

In CMOS image sensors, the pixel layout usually defines borders between adjacent photodetectors. In VI-CMOS image sensors, however, there are good reasons to avoid physical borders between adjacent photodetectors. The manufacturing cost of the photodetector die may be reduced significantly by avoiding the lithography
Figure 3. The VI-CMOS prototype in Fig. 1(b) is composed of a CMOS die and a photodetector die. (a) The central area of the CMOS die contains a circuit array for readout purposes, which mates to back contacts on the photodetectors. Surrounding bond pads mate to a transparent conductive oxide (TCO), which defines a front contact on the photodetectors. Peripheral bond pads are required to wire the image sensor to a package. (b) The central area of the photodetector die has an array of bond pads on a light-sensitive semiconductor. Surrounding bond pads are on the TCO.

steps required to pattern the borders. Moreover, edges of patterned devices introduce defect states and other imperfections that degrade performance, for example, by increasing the dark currents of photodetectors.

Without physical borders between adjacent photodetectors, lateral currents may flow due to drift and diffusion. This would cause photogenerated charge carriers to enter the “wrong” pixels of the CMOS die, a condition known as “crosstalk”. The crosstalk may be made negligible if a vertical electric field of sufficient uniformity and magnitude is applied on all photodetectors by the CMOS circuits. Schneider et al.\textsuperscript{17} used a feedback active pixel to introduce this approach in a VI-CMOS image sensor made by TFA technology. Skorka and Joseph\textsuperscript{18} elaborated on the design of such pixels, especially in terms of stability and compensation.

4.2 Photodetector Die

The photodetector die in Fig. 3(b) was fabricated in a custom process. Unlike with the CMOS die, the challenge with designing this die has to do with its cross-section, and not its floor plan. One must specify the material layers, their ordering, and their thicknesses. Usually, the electric field in the photodetectors is oriented parallel to the incident light flux, i.e., parallel to $\Phi$ in Fig. 2(c). Otherwise, each pixel requires two bond pads.

4.2.1 Substrate Materials

The handle substrate of the photodetector die must be transparent for the electromagnetic band targeted by the application. For better imaging performance, a large percentage of photons must reach the light-sensitive devices. There is always some loss of photons due to reflections at interfaces between photodetector layers. However, loss of photons due to absorption in the handle substrate should be minimized.

Handle substrates of the photodetector and CMOS dies should have similar coefficients of thermal expansion (CTEs). Large CTE differences cause mechanical stress when the temperature of the assembled device varies from the temperature of assembly. Temperature changes are expected when the device is powered up or down. Mechanical stress results in distortion of features, which may affect functionality, especially with nanoscale CMOS. Table 1 gives three CTEs of silicon, which is the handle substrate of standard CMOS dies, and of substrates suitable for visible-band applications. Borosilicate glass has CTEs closest to those of silicon.

When selecting a handle substrate, properties of other substrate materials in the photodetector die should be considered. Amorphous materials may, in general, be deposited on any handle substrate. However, crystalline materials require handle substrates with matching lattice constants. Moreover, the handle substrate must withstand all process steps required to make the photodetector die. For example, polysilicon films, which are suitable
Borosilicate glass, which is sold commercially as Pyrex or Borofloat, has CTEs that are closest to those of silicon.

<table>
<thead>
<tr>
<th>Material</th>
<th>CTE (10^{-6} K^{-1}) @ 200 K</th>
<th>CTE (10^{-6} K^{-1}) @ 293 K</th>
<th>CTE (10^{-6} K^{-1}) @ 500 K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>1.5</td>
<td>2.6</td>
<td>3.5</td>
</tr>
<tr>
<td>Glass, borosilicate</td>
<td>2.7</td>
<td>2.8</td>
<td>3.3</td>
</tr>
<tr>
<td>Glass, fused-silica</td>
<td>0.1</td>
<td>0.5</td>
<td>0.6</td>
</tr>
<tr>
<td>Glass, soda-lime</td>
<td>-</td>
<td>7.5</td>
<td>-</td>
</tr>
<tr>
<td>Quartz, single crystal,</td>
<td></td>
<td>c-axis</td>
<td>5.2</td>
</tr>
<tr>
<td>Quartz, single crystal, ⊥ c-axis</td>
<td>10.3</td>
<td>12.2</td>
<td>19.5</td>
</tr>
<tr>
<td>Sapphire, single crystal,</td>
<td></td>
<td>c-axis</td>
<td>4.1</td>
</tr>
<tr>
<td>Sapphire, single crystal, ⊥ c-axis</td>
<td>6.6</td>
<td>7.4</td>
<td>8.3</td>
</tr>
</tbody>
</table>

for photodetection, may be deposited using low-pressure chemical vapour deposition (LPCVD) at over 600°C. If the films are doped, they require annealing at 900–1000°C for dopant activation. Borosilicate glass, although transparent and with CTEs close to those of silicon, cannot be used with polysilicon photodetectors because it cannot withstand these temperatures. Fused silica, quartz, or sapphire should be used in this case.

4.2.2 Transparent Electrode

The first layer on the handle substrate must be a transparent conductor. It forms the front contact of all photodetectors, and is an essential electrode to realize a vertical electric field. In some cases, it is possible use a heavily-doped section of the handle substrate or the light-sensitive devices (subsequent layers) for this purpose. In other cases, one deposits a film based on thin metals, transparent conductive oxides (TCOs), transparent conductive polymers (TCPs), or carbon nanotubes (CNTs). These materials are described below.

**Thin metals:** Metals are very good conductors but are opaque to visible light. Metal films, however, transmit some visible light if they are very thin. Aluminum (Al), silver (Ag), and gold (Au), are attractive choices because they have a relatively high transmittance in the visible band. These metals must be less than 20 nm thick to have at least 10% transmission. Unfortunately, thin films are much less conductive than thick ones, and their conductivity is much more sensitive to thickness variation. Hence, it may be difficult to achieve a satisfactory combination of transparency, conductivity, and uniformity with thin metals.

**Transparent conductive oxides:** TCOs are semiconductors, usually polycrystalline or amorphous, that have high optical transparency and high electrical conductivity, properties normally considered mutually exclusive. To be used as a TCO, a semiconductor needs a high band gap (≥ 3.1 eV), a high concentration of free carriers (≥ 10^{19} cm^{-3}) – i.e., it needs to be a degenerated semiconductor – and a good mobility (≥ 1 cm²V^{-1}s^{-1}). Popular TCOs are indium oxide (In_2O_3), tin oxide (SnO_2), and zinc oxide (ZnO), which are all n-type semiconductors. Table 2 presents their optoelectronic properties. Although TCOs are more conductive than typical semiconductors, they are much less conductive than metals.

Often, TCOs are doped with impurities. Widely used examples are tin-doped indium oxide (In_2O_3:Sn or ITO) and aluminum-doped zinc oxide (ZnO:Al or AZO). ITO has been used for many years in applications where transparent electrodes were needed. However, because indium and tin are expensive metals, while zinc is cheap and non-toxic, AZO films have been getting more attention in recent years.

**Transparent conductive polymers:** Organic electronic devices are based on polymers such as those listed in Table 3. Mass production of organic devices is expected to be cheaper than that of inorganic devices.
Table 2. Optoelectronic properties of the three TCOs that are most commonly used.\textsuperscript{23}

<table>
<thead>
<tr>
<th>Material</th>
<th>Band Gap (eV)</th>
<th>Conductivity ($\Omega^{-1}\text{cm}^{-1}$)</th>
<th>Carrier Concentration ($\text{cm}^{-3}$)</th>
<th>Mobility ($\text{cm}^{2}\text{V}^{-1}\text{s}^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>In$_2$O$_3$</td>
<td>3.75</td>
<td>$10^4$</td>
<td>$&gt;10^{21}$</td>
<td>35</td>
</tr>
<tr>
<td>ZnO</td>
<td>3.35</td>
<td>$8 \cdot 10^3$</td>
<td>$&gt;10^{21}$</td>
<td>20</td>
</tr>
<tr>
<td>SnO$_2$</td>
<td>3.60</td>
<td>$5 \cdot 10^3$</td>
<td>$&gt;10^{20}$</td>
<td>15</td>
</tr>
</tbody>
</table>

Table 3. Abbreviations and full names of polymers commonly used in organic electronic devices.

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>CuPc</td>
<td>copper(II) phthalocyanine</td>
</tr>
<tr>
<td>PC60BM</td>
<td>(6,6)-phenyl-C61-butyric acid methyl ester</td>
</tr>
<tr>
<td>PDDTT</td>
<td>poly(5,7-bis(4-decanyl-2-thienyl)-thieno (3,4-b)diathiazole-thiophene-2,5)</td>
</tr>
<tr>
<td>PEDOT</td>
<td>poly(3,4-ethylenedioxythiophene)</td>
</tr>
<tr>
<td>PSS</td>
<td>poly(styrenesulfonate)</td>
</tr>
<tr>
<td>P3HT</td>
<td>poly(3-hexylthiophene)</td>
</tr>
</tbody>
</table>

Moreover, polymers are ideal for realizing flexible devices. Currently, ITO is widely used as a transparent electrode in organic optoelectronic devices.\textsuperscript{26} However, ITO is brittle, which makes it unsuitable for flexible devices. PEDOT:PSS is a flexible TCP that has been touted as a suitable replacement.\textsuperscript{27}

At present, the conductivity of TCPs is about an order of magnitude lower than that of ITO.\textsuperscript{28} and TCPs are less transparent to visible light than ITO.\textsuperscript{27} Moreover, when a device includes polymers, the maximum temperature that it can withstand during fabrication and operation is more limited. Therefore, the advantages of working with TCPs are relevant mainly when the whole device is organic.

Carbon nanotubes: Researchers have shown recently that thin films of CNTs, mainly single-walled CNTs (SWCNTs), may be used as transparent electrodes.\textsuperscript{29,30} SWCNTs are attractive because they can be deposited on almost any substrate,\textsuperscript{31} and because their mechanical properties make them suitable for use in flexible devices. Whereas indium prices are rising due to the increasing depletion of indium sources worldwide, carbon remains an abundant element. Hence, SWCNTs have a promising future.

Similar to the difficulties faced with polymers, the transparency and conductivity of SWCNTs are inferior to those of ITO. Sangeeth \textit{et al.}\textsuperscript{27} compared experimentally the performance of ITO, PEDOT:PSS, and SWCNTs. When SWCNT films have a transparency comparable to that of ITO films, for light at 550 nm (i.e., the middle of the visible band), their conductivity is almost two orders of magnitude lower. Nonetheless, researchers are working on methods to improve the conductivity of CNT films.\textsuperscript{31,32}

4.2.3 Light-Sensitive Devices

Electronic photodetectors are mainly constructed from a light-sensitive semiconductor, which must have high absorption coefficients for the targeted wavelengths. Hence, for visible-band imaging, the semiconductor band gap must be smaller than the energy of red photons. In addition, absorbed photons must change the electrical properties of the semiconductor sufficiently so that the change is detectable by a CMOS circuit.

With VI-CMOS image sensors, there may be more degrees of freedom in photodetector design than with CMOS image sensors. For example, the depth of lateral photodetectors in a CMOS image sensor is largely fixed by the doping profiles of the CMOS process. However, the depth of vertical photodetectors in a flip-chip image
sensor is largely variable. On the photodetector die, the thickness of the light-sensitive semiconductor may be chosen to optimize a performance measure, such as the ratio between photocurrent and dark current.\textsuperscript{33}

In addition to layer thicknesses, a photodetector design must specify the device type and the layer materials. In general, light-sensitive devices may be categorized as photoconductors, photodiodes, or phototransistors.\textsuperscript{34} Traditionally, photodetector layers were based on inorganic semiconductors, either crystalline or amorphous ones, but organic semiconductors may also be used. Further details are given below.

**Photoconductors:** A photoconductor (or photoresistor) consists of a uniformly-doped semiconductor sandwiched between ohmic contacts, i.e., heavily-doped layers of the same semiconductor. Device conductivity increases with increasing illumination. With an applied electric field, photogenerated electrons and holes are collected by opposite contacts. For good performance, the charge carriers should have long lifetimes and high mobilities. Otherwise, most of the excess electron-hole pairs recombine on their way to the contacts, and do not contribute to the photocurrent. The semiconductor should have a low dark current, with respect to photocurrent, for the device to have an acceptable response in dim illumination.

**Photodiodes:** Photodiodes are commonly used in CMOS image sensors. They incorporate either p-n junctions between p-doped and n-doped semiconductors or Schottky junctions between semiconductors and metals. Under reverse bias, photodiodes usually have lower dark currents than comparable photoconductors because of a depletion layer. An electric field accelerates photogenerated charge carriers towards the contacts, where they contribute to photocurrent. To increase the thickness of the depletion layer, an intrinsic layer (undoped or lightly doped) may be inserted between the p and n regions. This makes a p-i-n photodiode. Avalanche photodiodes permit the detection of single photons. These devices realize high gains by accelerating photogenerated charge carriers, using a high electric field, so as to generate secondary electron-hole pairs in the depletion layer. Lately, there has been an increased interest in avalanche photodiodes,\textsuperscript{35} which have applications not only in image sensors but also in microfluidics (lab on a chip).

**Phototransistors:** The term phototransistor is normally used for two back-to-back p-n junctions, i.e., light-sensitive devices that resemble bipolar transistors. When two Schottky junctions are used, the device is often called a metal-semiconductor-metal (MSM) photodetector. In either case, one junction is reversed biased while the other is forward biased when a voltage is applied. Photogenerated charge carriers perform the role of the base current in a bipolar transistor. A high photocurrent is possible.

**Crystalline semiconductors:** Crystalline silicon is the material used to make photodetectors in standard CMOS and CCD image sensors. Other crystalline semiconductors that are suitable for photodetection in the visible band are alloys like gallium arsenide\textsuperscript{36} (GaAs) and indium gallium nitride\textsuperscript{37} (InGaN). Common deposition methods for these materials are molecular beam epitaxy (MBE) and metal-organic chemical vapour deposition (MOCVD). Mercury cadmium telluride (HgCdTe or MCT) has long been used for infrared photodetection. The band gap of this alloy may be varied by changing the element proportions.\textsuperscript{38} The main drawback with crystalline materials is that they can be deposited only on substrates with similar lattice constants. Moreover, the deposition needs to be done at relatively high temperatures.

**Amorphous semiconductors:** Hydrogenated amorphous silicon (a-Si:H) is an amorphous semiconductor commonly used for photodetection in the visible band. It is a relatively cheap material, has a high absorption coefficient for visible light, and can be deposited on various substrates. Popular deposition methods for a-Si:H optoelectronic devices are sputtering and plasma-enhanced chemical vapour deposition (PECVD). The deposition is done at relatively low temperatures, i.e., at 200–250°C. Amorphous selenium (a-Se) is another amorphous semiconductor that is used for photodetection. Its properties make it ideal for detecting x-rays.\textsuperscript{39} However, a-Se photodetectors for the visible band have also been demonstrated.\textsuperscript{40}

**Organic semiconductors:** Although organic semiconductors have been studied for 60 years, their use in optoelectronic devices, e.g., LCD displays, is quite recent. The breakthrough was the discovery that some organic semiconductors are photoconductive under visible light.\textsuperscript{41} Initially, organic semiconductors were unstable and had a low carrier mobility. However, their properties have improved in recent years thanks
to extensive research. They are attractive for use in optoelectronic devices, as an alternative to inorganic semiconductors, because of their low cost, low deposition temperature, and flexibility. Organic photodetectors for the visible band have been demonstrated using materials such as penctane, a blend of PDDTT and PC60BM, and a structure composed of P3HT and CuPc thin films. Deposition methods for organic semiconductors include thermal evaporation, organic molecular beam deposition (OMBD), and spin coating. In some cases, deposition may be done at or just above room temperature.

4.3 Flip-Chip Bonding
CMOS dies and photodetector dies need to undergo a few more process steps before they can be flip-chip bonded. The process performed on the CMOS dies includes etching of the native oxide layer from the aluminum bond pads and deposition of a metal stack that has a good wettability to the solder material used in the flip-chip bonding. Photodetector dies are processed to form two sets of bond pads, which are also metal stacks. These bond pads form back contacts on the photodetectors, and also connect to the transparent electrode, which forms a front contact on the photodetectors. Such contacts must have a good adhesion to non-metallic materials, such as semiconductors and conductive oxides, and must have good wettability to the solder material.

The design and fabrication of bond pads for flip-chip bonding has been considered in a previous application note. One detail needs correcting. As illustrated in Fig. 4, the bond pads on the photodetector dies serve as under-bump metalization (UBM), and those on the CMOS dies serve as top surface metallurgy (TSM). Unlike what was expected, the flip-chip bonding contractor preferred to form the solder bumps on the photodetector dies, not on the CMOS dies. Having the solder bumps on the smaller die facilitated the assembly process.

5. DESIGN AND FABRICATION OF A PROTOTYPE
The previous section focused on general principles in the design and fabrication of a VI-CMOS image sensor. This section focuses on the design and fabrication of a specific prototype.

CMOS dies were fabricated in a standard CMOS process. Therefore, the challenging part with these dies was the circuit design, mainly the pixel layout, and not the fabrication. Photodetector dies, however, were fabricated in a custom process. In terms of manufacturability and performance, these dies are not the best that could be designed for the visible band, which was targeted for simplicity. However, they are the best that could be made with the available materials and equipment. A new process was developed at the UofA Nanofab to realize the photodetector dies. Process development requires that all materials used, e.g., etching gases and solutions, and all conditions reached, e.g., maximum temperature, work without any undesirable side effects.
Figure 5. Floor plan and pixel layout of the designed CMOS die. (a) As with a CMOS image sensor, the CMOS die of a VI-CMOS image sensor requires active pixels (AP), row and column address decoders (AD), and buffers (BF). Extra circuits (EC) and alignment marks (AM) are included for test purposes and flip-chip bonding. (b) The active pixel has a bond pad (BP) for the vertical photodetector and a feedback logarithmic-response circuit (FL), as well as a lateral photodiode (LP) and a standard logarithmic-response circuit (SL). A switch (SW) configures the output.

5.1 CMOS Die

The CMOS die was designed for a 0.8\textmu m Dalsa process, which has three metal layers. Fig. 5 gives the floor plan, which includes a 20 × 24 array of active pixels, and the pixel layout, which includes a bond pad for the vertical photodetector. ADCs were not included for simplicity. Although electrostatic discharge protection is recommended for all bond pads, such circuits were only included in wire bond pads. Interior bond pads are inaccessible after flip-chip bonding. Schematic and layout designs were done with Cadence. The schematic was verified using DC, AC, and transient simulations. The layout was verified using design rule check (DRC) and layout versus schematic (LVS) tests. Dies were fabricated through CMC.

Pixels are 110 × 110\textmu m², which is quite large for visible-band applications. When the project was at the design stage, CMC could guarantee flip-chip bonding only for bond pads of at least 55\textmu m pitch and 110\textmu m spacing from centre to centre. However, American researchers have demonstrated VI-CMOS image sensors, using flip-chip technology, with 10 × 10\textmu m² pixels. Improved access to fine-pitch flip-chip bonding will make it possible for Canadian researchers to realize VI-CMOS image sensors with high spatial resolution.

In general, design rules of CMOS processes do not allow placement of devices underneath bond pads, and require bond pads to connect to all metal layers. However, researchers are working to change this. For example, Ker et al. designed and tested NMOS transistors underneath wire bond pads. Their bond pads used all metal layers except the lowest, which was used for the transistors. Even after wire bonding, there was little difference between the characteristics of these transistors and standard ones, located far from the bond pads.

Because the light-sensitive semiconductor in the photodetector die is unpatterned, active pixels in the CMOS die employ feedback circuits to reduce crosstalk. A logarithmic response to light stimulus was chosen over a linear one because it can capture a higher dynamic range. The feedback logarithmic-response circuit maintains a constant voltage at the photodetector back contacts and, therefore, uses current as its input signal.

Each pixel also includes a lateral photodiode and a standard logarithmic-response circuit. Because space was available in the layout, these were added so that the functionality of the CMOS die could be tested independently of flip-chip bonding. In addition, the pixel contains a switch, which is configured externally. In one configuration, the lateral photodiode is connected to the standard logarithmic circuit, and the vertical photodetector is connected to the feedback logarithmic circuit. Connections are swapped in the second configuration.
To verify the functionality of the CMOS circuits, several CMOS dies were packaged without undergoing flip-chip bonding. A PCB was designed to test packaged CMOS dies, as well as the final prototypes. Data conversion is done on the PCB with a commercial ADC. Control of the CMOS die and ADC is accomplished with an Altera Cyclone II FPGA board, which communicates with a PC through a QuickUSB board from Bitwise Systems. The FPGA reads video data from the image sensor via the ADC and sends it to a PC, where it is processed for real time display. All boards are powered by the PC’s universal serial bus (USB).

5.2 Photodetector Die

The design of the photodetector die was mainly determined by the light-sensitive semiconductor that we could use. There was no equipment for GaAs deposition in the Nanofab. Moreover, GaAs films must be deposited on GaAs substrates, which are opaque to visible light. Some options, such as HgCdTe (MCT), were ruled out because of their toxicity. Other options, such as organic films, did not have good enough performance at the time. After a careful review, the only semiconductor we could work with productively was a-Si:H.

In general, a-Si:H can be deposited either by sputtering or by PECVD. The latter method tends to yield higher quality films than the former method. Sputtering must be done at 200–250°C as a reactive process using hydrogen. Although the Nanofab has sputtering machines, none of them had a hydrogen supply. Fortunately, Micralyne Inc, an Edmonton company, agreed to deposit a-Si:H films with their PECVD machine. Micralyne’s process, however, did not support dopant gases. Therefore, our devices had to be based on intrinsic films, and so photodiodes could not be implemented. To create ohmic contacts, shallow heavily-doped diffusion layers are required, but we did not have equipment that could be used for this purpose. Consequently, we designed an MSM device, in which an intrinsic a-Si:H layer is sandwiched between two conductive layers.

5.2.1 Substrate Materials

We used borosilicate glass (Borofloat) as the handle substrate for the photodetectors. Although thinner substrates were available, we used 1 mm thick ones because they were in stock at the Nanofab. Substrates were cleaned using a Piranha solution (sulfuric acid and hydrogen peroxide). Using the VASE ellipsometer in the Nanofab, we measured the optical transmission of a naked substrate. Results are presented in Fig. 6.

Fig. 7 illustrates the fabrication process of the photodetectors. ITO and a-Si:H were deposited on the handle substrate by sputtering and PECVD, respectively. The purpose of the first lithography step was to selectively
Figure 7. Fabrication process of the designed photodetector die. (a) ITO is sputtered at room temperature on a clean borosilicate glass substrate. The ITO is annealed to improve its conductivity. Using PECVD, a-Si:H is deposited on the ITO. (b) The first lithography step uses reactive ion etching to expose ITO at the periphery of a-Si:H rectangles. (c) An array of UBM bond pads is formed on the a-Si:H rectangles, with further UBM bond pads on the surrounding ITO. A metal grid is deposited with the bond pads to mark dicing lines on the coated glass substrate.

etch the a-Si:H layer. One needs to expose the ITO layer because, in the VI-CMOS image sensor, an electric potential must be applied to it. The a-Si:H was dry etched using the Plasma Lab µEtch machine in the Nanofab. The chamber was pumped down prior to the process. Etching was done in an atmosphere composed of 40 sccm of carbon tetrafluoride (CF₄) and 10 sccm of oxygen (O₂). The CF₄/O₂ plasma also serves as surface treatment to improve performance of the ITO film. An RF power of 100 W was applied, and the chamber pressure was 63 mTorr. A chrome mask was used for the dry etch because earlier trials with a photoresist mask showed that the etchant gases consumed the photoresist at a higher rate than the a-Si:H.

The final photodetector design was a Cr/a-Si:H/ITO stack on glass. Chrome was used as the back contact because it has a good adhesion to non-metal substrates, including a-Si:H. To get a higher photocurrent to dark current ratio with this MSM device, the CMOS die connects the ITO electrode to a higher voltage than the chrome electrode due to the relative size of potential barriers at the two Schottky junctions.

5.2.2 Transparent Electrode

Equipment and materials available in the Nanofab meant we could use either a thin metal or TCO film as the transparent electrode. The layer could be realized by physical vapour deposition (PVD), i.e., either sputtering or e-beam evaporation. We preferred the TCO option because our first sputtering trials of ITO were successful, despite a brittle ITO target. Moreover, if a metal film is used, it must be less than 20 nm thick. Although the substrate is rotated during the deposition, there are still non-uniformities in film thickness. With thin metals, small variations in thickness result in large variations in transparency and conductivity.

For photodetectors based on a-Si:H, in which an a-Si:H film is deposited on a TCO substrate, ZnO is preferable to ITO as the TCO material. The a-Si:H is normally deposited using a PECVD process, during which the TCO surface is exposed to hydrogen plasma. When ITO is exposed to hydrogen plasma, hydrogen radicals react with the oxygen in the ITO, and reduce some of the oxide into metals, i.e., indium and tin. This decreases the
transparency of the ITO to visible light, and also changes the electrical properties of the a-Si:H/ITO contact. ZnO, on the contrary, is non-reactive under these conditions.\textsuperscript{51}

Although ZnO (and AZO) targets are available commercially, we were not allowed to work with zinc in the multi-user machines of the Nanofab because zinc has a high vapour pressure at low temperatures. Usage of zinc in the vacuum chambers would mean that, for a long time, future users of the machine would have zinc contamination in their depositions. Therefore, we had to work with ITO.

The ITO films were deposited in a Lesker magnetron sputtering machine with a Lesker ITO target. Prior to deposition, the chamber was pumped down to a pressure of 2\,\mu\text{Torr}. The deposition was done in a pure argon environment with a gas flow of 50\,sccm, and under pressure of 5.3\,mTorr. Each deposition lasted for 50 min. An RF power of 80\,W was used during the process. Under these conditions, the mean deposition rate of the ITO was 5.5\,nm/min. Film resistivity was measured immediately after deposition using a four-point probe. The average value was 5.83\,\times\,10^{-4}\,\Omega\,cm. Deposition of ITO films in a reactive process, where the chamber atmosphere was 1\% oxygen, resulted in films that were about twice as resistive (or half as conductive).

After deposition, the ITO films were annealed for two hours in air at 150–175\,°C. The average resistivity after annealing was 5.45\,\times\,10^{-4}\,\Omega\,cm. Annealing trials that were performed at 250–325\,°C resulted in increased resistivity. Finally, the annealing had negligible impact on film transparency, as shown in Fig. 6.

5.2.3 Light-Sensitive Devices
Micralyne deposited two sets of a-Si:H films for us by PECVD. Both depositions were done at 200\,°C. In the first set, a-Si:H was deposited on two thermal-oxide silicon wafers. One film was 50\,nm thick, and the other was 1000\,nm thick. The purpose was to characterize the films, and to determine their suitability for our application. In the second set, a-Si:H was deposited on four ITO-coated Borofloat wafers. Film thicknesses were 250, 500, 750, and 1000\,nm. These depositions were used to fabricate the photodetector dies. We asked for multiple thicknesses to experimentally determine the optimal photodetector thickness in the VI-CMOS image sensor. The 1000\,nm film in this second set, however, was not uniform over the substrate. “Bald” areas could be seen.

The thick Micralyne film on the thermal oxide substrate was used to measure optical properties in the visible band. Extraction of the absorption coefficient, $\alpha$, was done using the VASE ellipsometer in the Nanofab. A thin film is needed to ensure that not all the light passing through the a-Si:H is absorbed. Monochromatic light reflected from the sample at various interfaces contains information that is used to extract $\alpha$. Fig. 8(a) gives the absorption coefficient of the Micralyne film versus wavelength, $\lambda$. Results are compared to reported values for crystalline silicon,\textsuperscript{52} as well as hydrogenated and non-hydrogenated amorphous silicon.\textsuperscript{53} In most of the visible band, the Micralyne film absorbs about ten times as much light as does crystalline silicon.

Absorption coefficients of the Micralyne film and crystalline silicon were used to calculate the power, per wavelength, that would be absorbed by a 500\,nm film, per unit area, given a blackbody light source of 300\,lux power density with a 3050\,K colour temperature. These illumination conditions approximate a real laboratory light source. Results are given in Fig. 8(b). They are compared to the photopic sensitivity of the human eye, which is a measure of relative light power perceived by human colour vision. The Micralyne film absorbs light in a manner more similar to human photopic sensitivity than does crystalline silicon.

The thick Micralyne film on the second thermal oxide substrate was used for optoelectronic characterization. Because the thermal oxide substrate is an insulator, electrical properties of the film could only be tested with surface contacts. Aluminum was deposited on the a-Si:H to form contacts. After lithography, a pattern of long and narrow contact lines was made, as shown in Fig. 8(c), to implement the transmission line model (TLM) method.\textsuperscript{54} With $W = 5$\,mm and $d = 80\,\mu$m, $\ell$ was varied from 5 to 320\,\mu m. The TLM method extracts sheet resistance. Given film thickness, the material conductivity may also be extracted.

Sheet resistance and material conductivity versus illuminance were extracted by illuminating the patterned Micralyne film and repeating the TLM method. We used a halogen light source with a 3050\,K correlated colour temperature and a cold fibre waveguide. Results are shown in Fig. 8(d). Conductivity of the Micralyne film changes by about four orders of magnitude in response to a similar change in the illuminance. A second y-axis gives the estimated current for a $10 \times 10\,\mu$m$^2$ pixel, i.e., for pixel dimensions more suitable for imaging than the ones actually used ($110 \times 110\,\mu$m$^2$). Currents in this range may be easily sensed by CMOS circuits.
Figure 8. Optoelectronic properties of Micralyne a-Si:H films. (a) Measured absorption coefficients are compared to reported values for crystalline\(^5\)\(^2\) and amorphous\(^5\)\(^3\) silicon (hydrogenated and non-hydrogenated). (b) Power absorbed by a 500 nm film is calculated for 300 lux illumination with a 3050 K blackbody spectrum, and is compared to human photopic sensitivity. (c) Sheet resistance is measured using the TLM method,\(^5\)\(^4\) which required long contacts to be patterned with variable spacing. (d) Conductivity is calculated from sheet resistance – both vary with applied illuminance (3050 K colour temperature). Current in a 10 × 10 \(\mu\)m\(^2\) pixel is also calculated, assuming 1V is applied across a 500 nm film.

Human vision has three different modes of operation, which vary in accordance to illuminance level. Scotopic vision, or dark vision, occurs for illuminances lower than 0.05 lux, and photopic vision, or color vision, occurs for illuminances higher than 50 lux.\(^5\)\(^5\) For illuminances between these thresholds, the human eye operates in a transition mode called mesopic vision. Fig. 8(d) shows that the Micralyne film is sensitive to light even at levels below the photopic vision threshold. It is therefore suitable for imaging in the visible band.

There is one more factor to note. Steabler and Wronski\(^5\)\(^6\) found that when exposed to light, there is a gradual decrease in the photocurrent and dark current of a-Si:H films. This change can be reversed by annealing the films in a temperature that is slightly lower than their deposition temperature. Extensive research has been done on the Steabler-Wronski effect (SWE) by various groups around the world.\(^5\)\(^7\) We are not certain to what extent our VI-CMOS image sensor is affected by the SWE. However, our main purpose is to advance Canadian state-of-the-art with a prototype. Different light-sensitive devices may be used in future.
5.3 Flip-Chip Bonding

Figs. 3(a) and (b) show finished CMOS and photodetector dies. UBM bond pads were fabricated on the photodetector dies, both on the a-Si:H surface, where they are arranged in a 20×24 array, and on the exposed ITO at the array periphery. Design and fabrication of these bond pads are discussed in a previous application note. The finished dies were sent to a flip-chip contractor for assembly. TSM was deposited on the interior bond pads of the CMOS dies by the contractor. The contractor also had to form solder bumps on the UBM bond pads. However, at this point he encountered several difficulties with the photodetector dies.

First, the UBM bond pads did not show good wettability to the indium-based solder material. Repeating the process after surface cleaning with methanol improved the results. Therefore, we assume that it was caused by surface contamination with organic material. In addition, there was a problem with adhesion of the bond pads to the a-Si:H surface when a high temperature was applied in order to form the solder bumps. This problem was even more evident on the ITO surface. These problems arose partly because we had expected solder bumps to be formed on the CMOS dies and did not design the photodetector dies for that purpose.

The flip-chip contractor told us he had a process for UBM formation. His process works successfully on crystalline silicon and glass substrates. It includes deposition of a titanium adhesion layer and a thick aluminum layer. This is followed by electroless nickel and immersion gold plating. Although this process has never been tried on glass substrates coated with a-Si:H and ITO, we believe that it is likely to work. If the deposition of the UBM is done by the contractor, he must be provided with the glass substrates after the first lithography step, when the a-Si:H is etched to expose the ITO. He also requires a positive mask for the bond pads.

The flip-chip contractor recommended sending undiced glass substrates next time. Some photodetector dies were damaged as they were too small to handle. After formation of the solder bumps, the flip-chip contractor can dice the substrates into dies at his facility. Moreover, in future work on similar prototypes, one should include process steps to cover the surface of the light-sensitive devices and the transparent electrode with a dielectric layer. This should be done everywhere except over the bond pads. A dielectric layer would prevent mechanical and chemical damage to the photodetectors before, during, and after flip-chip bonding.

These difficulties resulted in a low yield after flip-chip bonding. We intended to get twelve prototypes. However, this number was reduced to eight because of the difficulties encountered by the contractor. During the return shipment, five of the eight prototypes disassembled into two dies. Thus, we received three prototypes of the VI-CMOS image sensor, all of which were functional. One of them is shown in Fig. 1(b).

6. CONCLUSION

Image sensors include photodetectors and mixed-signal circuits, which involve devices with different requirements. Vertical integration of these devices in a VI-CMOS image sensor means each tier may be fabricated in a different process. This enables advanced circuits in each pixel without sacrificing spatial resolution. Advanced pixel-level circuitry is essential for improving the overall performance of image sensors. Although there are other options, this application note focuses on VI-CMOS image sensors made by flip-chip bonding. They are composed of two dies: a silicon die with CMOS circuits, and a transparent die with photodetectors.

The main difference between a CMOS die of a VI-CMOS image sensor and a CMOS image sensor is that, with the former, each pixel needs a bond pad for a vertical photodetector and does not need a lateral photodetector. It is desirable to leave the light-sensitive semiconductor unpatterned in the photodetector die of a VI-CMOS image sensor. This results in a preference for feedback active pixels in the CMOS die, whereby potential differences between adjacent photodetector contacts are attenuated to reduce pixel crosstalk.

The design of photodetectors for VI-CMOS image sensors, especially those fabricated by flip-chip bonding, has many more degrees of freedom than the design of photodetectors for CMOS image sensors. Choices need to be made regarding materials used for the handle substrate, the transparent electrode, and the light-sensitive devices. One must also choose the light-sensitive device type, which may be a photoconductor, photodiode, or phototransistor. With all this freedom, photodetectors may be optimized for various applications.

In addition to general design and fabrication principles, supported by extensive references, this work presents a specific VI-CMOS image sensor prototype. To make the prototype, a CMOS die was designed for a commercial
process, and a photodetector die was designed for a custom process. The CMOS die was fabricated by Dalsa through CMC Microsystems, and the photodetector die was fabricated at the University of Alberta Nanofab and Micralyne Inc. Finally, the two dies were assembled by a flip-chip contractor through CMC.

The VI-CMOS prototype includes two sets of CMOS circuits in each pixel. The first is a feedback logarithmic-response circuit, and the second is a standard logarithmic-response circuit. Each pixel also includes both a vertical MSM photodetector, which uses an unpatterned a-Si:H film, and a lateral CMOS photodiode. Test results of the prototypes will be reported elsewhere, but the prototypes are functional. Nonetheless, optoelectronic properties of the Micralyne a-Si:H films were reported. The films proved excellent for visible-band imaging.

The main outcome of this work is a process flow for what is, to our knowledge, the first Canadian VI-CMOS image sensor. The main drawback is a low spatial resolution due to large pixels. Even if fine-pitch flip-chip bonding cannot be accessed by Canadian researchers in the near future, there are applications where large pixels are desirable, e.g., in sensors for x-ray imaging. An advantage of flip-chip bonding is its robustness. As long as contact dimensions and electrical interfaces are preserved, the same CMOS die may be bonded to various sensor dies, which are not limited to photodetector dies.

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